THE PENNSYLVANIA STATE UNIVERSITY
SCHREYER HONORS COLLEGE

DEPARTMENT OF ELECTRICAL ENGINEERING

ANALYSIS, DESIGN, AND SYNTHESIS OF A NEGATIVE RESISTANCE CONVERTER FOR A MARGINAL OSCILLATOR

BRANDON TRICOU
Spring 2011

A thesis
submitted in partial fulfillment
of the requirements
for a baccalaureate degree
in Electrical Engineering
with honors in Electrical Engineering

Reviewed and approved* by the following:

Jeffrey L. Schiano
Associate Professor of Electrical Engineering
Thesis Supervisor

John D. Mitchell
Professor of Electrical Engineering
Honors Adviser

* Signatures are on file in the Schreyer Honors College.

Abstract

A negative resistance converter (NRC) is a two-terminal active circuit whose terminal current/voltage (i/v) relationship is that of a negative resistor. NRCs with a nonlinear i/v relationship are especially useful for creating marginal oscillators (MO) by canceling the losses in a tuned circuit. Though NRCs have been implemented in earlier MO designs, few authors have fully understood what the shape of an NRC's i/v characteristic should be, and none have presented simulated or experimental verification of their NRC's i/v characteristic. This thesis examines three previous NRC implementations both analytically and through the use of simulation software. This thesis goes on to design and synthesize an analog nonlinear NRC using high-frequency operational amplifiers and Schottky diodes. The NRC is designed such that its i/v characteristic can be tuned with potentiometers. Finally, this thesis experimentally confirms that the NRC's i/v characteristic matches that of a desired characteristic characteristic.

Table of Contents

List of Figures

List of Tables

Chapter 1

Negative Resistance Converter

1.1 Figures of Merit

A negative resistance converter (NRC) is an active circuit with a single terminal pair whose current/voltage (i/v) relationship is that of a negative resistance. In other words, a positive voltage applied to the terminals of an NRC will result in a negative current, and vice versa. This configuration is shown in Figure 1.1(a), and the resultant i/v characteristic is shown in Figure 1.1(b). The slope of the i/v characteristic shown in Figure 1.1(b) is $-g$, where g has units of Siemens.

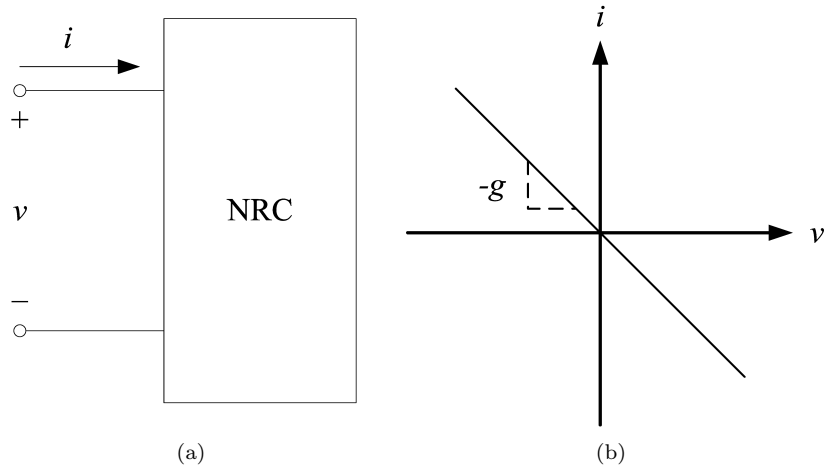


Figure 1.1. (a) Two-Terminal NRC, (b) i/v Characteristic of a Simple Linear NRC

In most applications, it is necessary to decrease the slope of the i/v characteristic with in-

creasing voltage magnitude to avoid dynamic instability. As an example, the piecewise-linear NRC i/v characteristic in Figure 1.2 is characterized by the parameters g_A, g_B, and v_T. When the magnitude of the NRC terminal voltage is less than v_T, the slope of the i/v characteristic is $-g_A$. When the input voltage magnitude exceeds v_T, the slope of the i/v characteristic is reduced from $-g_A$ to $-g_B$, where $g_B < g_A$.

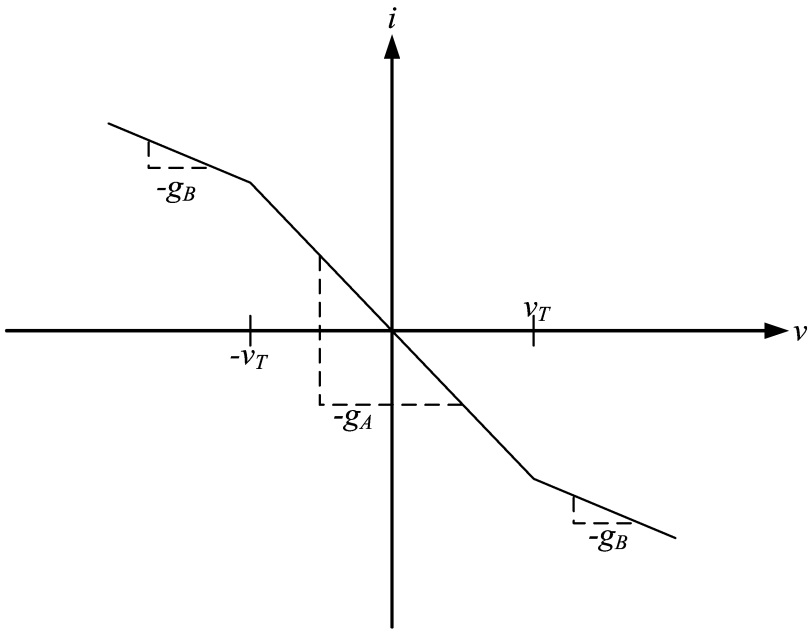


Figure 1.2. Ideal NRC i/v Characteristic

The NRC whose i/v characteristic is shown in Figure 1.2 is a memoryless nonlinear system. However, the practical implementation utilizes amplifiers with finite bandwidth, which introduces an undesirable phase shift between the input voltage and current at the terminals of the NRC. For a sinusoidal driving voltage, the effect of this phase shift is to open an "eye" in the i/v characteristic. Figure 1.3 shows an i/v characteristic for an NRC whose finite amplifier results in a phase shift.

1.2 Applications

When an NRC with terminal resistance $-R$ is placed in parallel with a positive resistance R, the two resistances will effectively appear as an open circuit. In this way, NRCs can be used

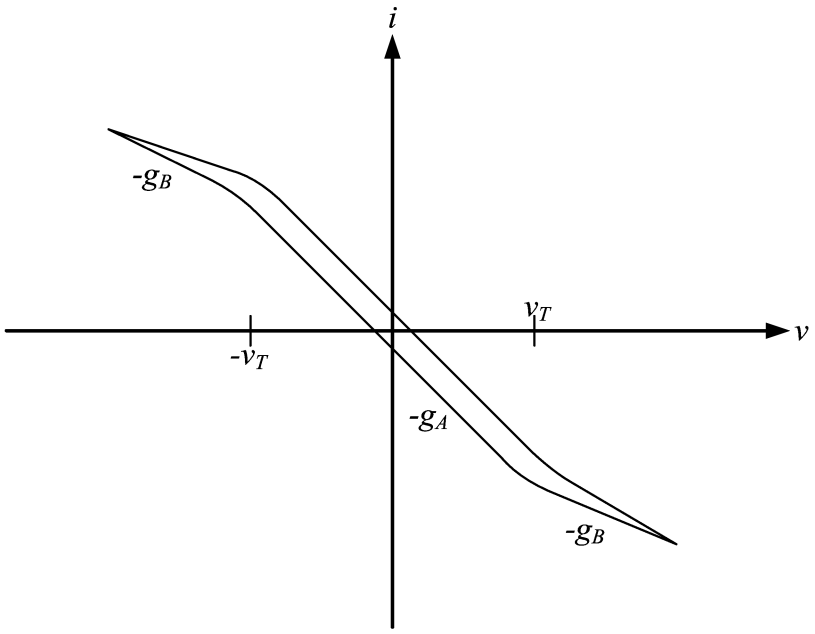


Figure 1.3. i/v Characteristic of an NRC with a Phase Shift

to create lossless circuits. The intended application for the NRC studied in this report is the synthesis of a marginal oscillator for observing the absorption of energy in quadrupole resonance (QR) experiments [1]. NRCs have also been used in the design of autonomous chaotic circuits like Chua's Circuit. These applications are now discussed in sections 1.2.1 and 1.2.2, respectively.

1.2.1 Marginal Oscillators

Marginal oscillators are used to sense small changes in the losses of a tuned circuit. Pound is credited with developing the first marginal oscillator in the 1940s for detecting the absorption of radio frequency energy in nuclear magnetic resonance spectroscopy experiments [2, 3]. In the following decades, marginal oscillators would find practical applications in the fields of ion cyclotron resonance spectroscopy [4] and the monitoring of the mechanical properties of thin-films [5], the characterization of defects in silicon [6], and the measurement of penetration depth in super-conductors [7].

Marginals oscillators are comprised of a linear tuned circuit and a nonlinear feedback element. Figure 1.4 shows the conceptual model of a marginal oscillator. It consists of a tuned RLC circuit driven by a dependent current source whose i/v characteristic is shown in Figure 1.2. The

resistance R represents the losses in the tuned circuit, while A represents the amplitude of the oscillations. Many of the authors who studied marginal oscillator behavior recognized that the nonlinear feedback element needed to both appear as a negative resistance to the tuned circuit, and also provide gain to sustain oscillation. However, up until the mid-1970s, it was not well-understood how the shape of the i/v characteristic of the NRC affected the sensitivity of the amplitude of oscillation with respect to changes in the losses of the tuned circuit.

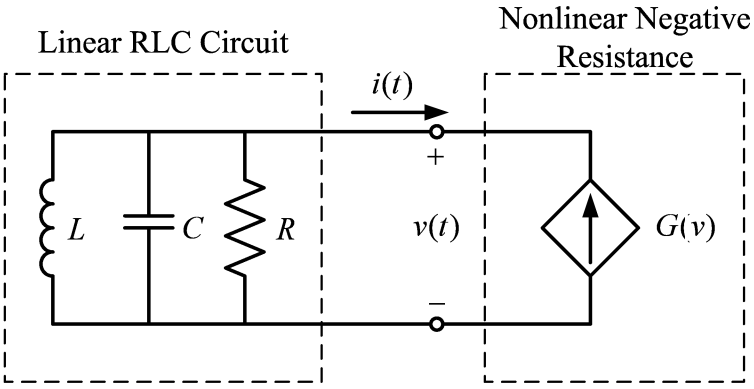


Figure 1.4. Conceptual Model of a Marginal Oscillator

In her 1975 thesis, Viswanathan recognized that the *shape* of the i/v characteristic of the nonlinear feedback element directly affects how losses in the tuned circuit affect the amplitude of oscillation. Viswanathan modeled the i/v characteristic of the nonlinear feedback element using the piecewise-linear curve in Figure 1.2 because it is a reasonable representation for NRCs constructed from nonlinear circuit elements such as vacuum tubes and field effect transistors (FETs). Her other contribution was to formally define conversion gain and to derive it in terms of the NRC's parameters [1].

Viswanathan defined conversion gain,

$$G_C = S_R^A = \frac{\Delta A}{\Delta R}\frac{R}{A} = \frac{\%\text{ change in A}}{\%\text{ change in R}}, \tag{1.1}$$

as the sensitivity of the oscillation amplitude to small changes in resistance. For a parallel RLC circuit driven by an independent current source at its natural frequency, it can be shown that the conversion gain is unity. This means that a $1\mu\Omega$ change in resistance would result in a 1 μV

change in oscillation amplitude. Viswanathan noted that it is possible to achieve a conversion gain much greater than unity by using a piecewise linear feedback element [1]. She showed that the conversion gain G_C is related to the NRC parameters g_A and g_B defined in Figure 1.2 by

$$G_C = \frac{\pi}{2(1 - g_B/g_A)g_A \sin(2\theta)}, \tag{1.2}$$

where $\theta \in \left[0, \frac{\pi}{2}\right]$ is a solution to

$$\sin(2\theta) + 2\theta = \frac{\pi}{(1 - g_B/g_A)} \left[\frac{1}{g_A R} - \frac{g_B}{g_A}\right]. \tag{1.3}$$

Furthermore, she showed that the amplitude of oscillation satisfies

$$v_T = A \sin(\theta), \tag{1.4}$$

where the threshold voltage v_T is defined in Figure 1.2.

In marginal oscillator designs, the conversion gain is the primary figure of merit. A high conversion gain is desirable as it increases the signal-to-noise ratio when detecting small changes in the resistance of the tuned circuit [1].

1.2.2 Autonomous Chaotic Circuits

NRCs also have applications in the synthesis of autonomous chaotic circuits. An autonomous chaotic circuit is a circuit that experiences large changes in its output due to small changes in its initial conditions. The first functional autonomous chaotic circuit was designed in 1983 by Leon Chua while visiting Waseda University in Tokyo. There, Professor T. Matsumoto was attempting to build a circuit realization of the Lorenz equations, which is one of only two autonomous systems generally accepted as being chaotic. Matsumoto's circuit utilized more than a dozen integrated circuits (ICs) and took over a year to design and build. Unfortunately, it failed to demonstrate chaotic behavior [8].

It did, however, inspire Leon Chua to design a simpler, more robust chaotic circuit. Chua realized that in order for a circuit to be chaotic, it must have at least three linear passive energy storage elements and exactly one 2-terminal nonlinear resistor characterized by a piecewise-linear, voltage-controlled v-i characteristic. In order to sustain an oscillation, the nonlinear resistor must

be capable of sourcing energy to the circuit to overcome losses. However, as the amplitude of the voltage across the nonlinear resistor increases, it must eventually resemble a passive resistor in order to sustain a steady-state oscillation. For these reasons, the nonlinear resistor is said to be eventually passive [9]. Chua's experience with nonlinear circuit design led to the choice of a negative, piecewise-linear v-i characteristic because it is both easier to both analyze and synthesize [8].

Chua's nonlinear resistor is directly analogous to the NRC being studied at Penn State. The three inner slopes of its i/v characteristic have the exact same shape as the i/v characteristic shown in Figure 1.2. Chua's circuit was of initial interest to the lab at Penn State because, unlike other NRC designs, Chua implemented his nonlinear resistor by capitalizing on the nonlinear characteristics of operational amplifiers. Using only two operational amplifiers, a handful of resistors, and three energy storage elements, Chua created a circuit that exhibited chaos [8].

1.3 Thesis Contributions

Though many authors have implemented NRCs for use in marginal oscillators, none have verified the i/v characteristics of their NRC circuits. This thesis will examine the i/v characteristics of previous designs using simulation tools. By analyzing past designs and comparing them to a predicted functional model, this thesis will provide insight into the most desirable NRC characteristics. In addition, this thesis aims to design an analog NRC that will exhibit the i/v characteristic from Figure 1.2. The relationships between analog components and i/v parameters will be explored and utilized to design a circuit whose passive components can be used to adjust g_A, g_B, and v_T. This circuit will be simulated, synthesized, and tested experimentally.

1.3.1 Assessment of Earlier NRC Designs

This thesis will explore NRC designs by Lee and Choh, Viswanathan, and Chua. The first two implemented NRCs using FETs as part of their marginal oscillator designs. Their circuits will be assessed based on both component choice and the shape of the i/v characteristic obtained using simulation software. Chua's NRC design is also of interest because his implementation utilizes operational amplifiers. His design will be assessed mathematically to demonstrate the strengths and weaknesses of his approach.

1.3.2 NRC Design Specifications

The proposed NRC design should produce a piecewise linear i/v characteristic like that shown in Figure 1.2. The circuit should function with a phase shift of 12 degrees or less from DC to 5 MHz. It is desired that the phase shift be zero because all of Viswanathan's analysis is based on that assumption, and it is her analysis that allows for an evaluation of conversion gain. Given a resistance R looking into the circuit of -60 kΩ, the parameters g_A and g_B should be tunable such that

$$1 < g_A R < 1.2 \tag{1.5}$$

and

$$0.8 < g_B R < 0.95. \tag{1.6}$$

The threshold voltage v_T must also be adjustable.

1.3.3 Thesis Organization

Chapter 2 is a detailed analysis of previous NRC designs using both qualitative techniques and simulation results. Chapter 3 is a more detailed explanation of the design and analysis of an NRC. Chapter 4 discusses the synthesis and experimental verification of the NRC presented in Chapter 3. Chapter 5 is a summary of this thesis and a discussion of future work.

Chapter 2

Previous Work

2.1 Generalized NRC

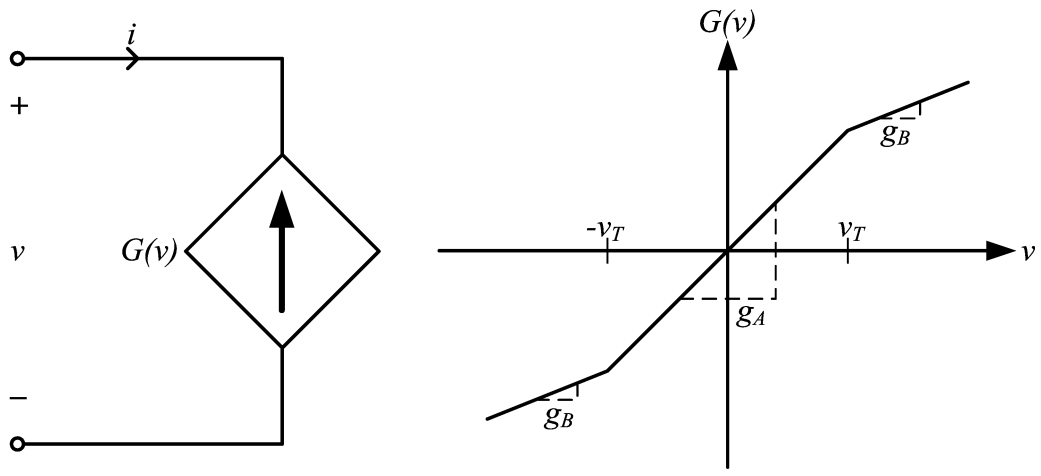
In order to understand how previous authors implemented their NRCs, it is first necessary to show how to realize a general NRC using a nonlinear amplifier contained within a feedback loop. As a starting point, consider from Chapter 1 the two-terminal NRC shown in Figure 1.1(a) with the i/v characteristic shown in Figure 1.2. This NRC can be represented by the voltage-controlled current source shown in Figure 2.1(a). To maintain the NRC's i/v characteristic, the dependent current source must have the i/v characteristic shown in Figure 2.1(b).

Given that $i = -G(v)$, the slope of the i/v characteristic of the dependent current source can be expressed by taking the derivative of the current with respect to voltage. Let $g(v)$ be the derivative of $G(V)$ such that

$$\frac{di}{dv} = -\frac{dG(v)}{dv} = -g(v). \tag{2.1}$$

$g(v)$, which is the slope of $G(v)$, is shown graphically in Figure 2.2. The function $g(v)$ represents the gain of the dependent current source, while $-g(v)$ represents the conductance looking into the NRC's terminals at an input voltage v.

In practice, it is much easier to implement a voltage-controlled voltage source than it is to implement a voltage-controlled current source. For this reason, it is convenient to substitute the circuit model shown in Figure 2.1(a) with the circuit model shown in Figure 2.3(a). This new model is composed of a resistor R and a voltage-dependent voltage source whose gain with



(a) (b)

Figure 2.1. (a) Voltage-Controlled Current Source NRC Representation, (b) i/v Characteristic of Dependent Current Source

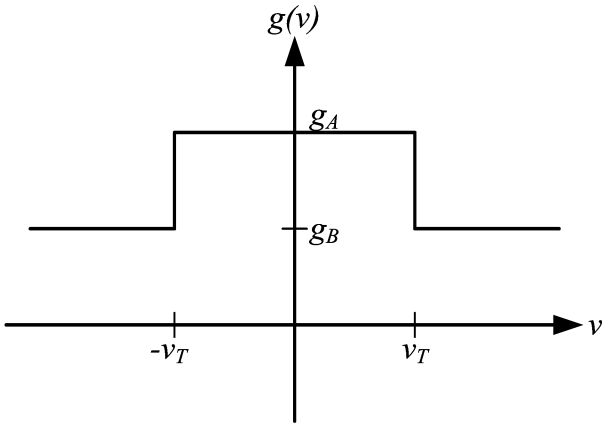


Figure 2.2. Slope of the Dependent Current Source

respect to the input voltage v is given by the function $\bar{G}(v)$. Equivalently, the layout in Figure 2.3(a) can be modeled as an ideal amplifier with a resistor connected between its input and its output. This representation is shown in Figure 2.3(b).

From Figure 2.3(a), the current i can be expressed as

$$i = \frac{v - \bar{G}(v)}{R}. \tag{2.2}$$

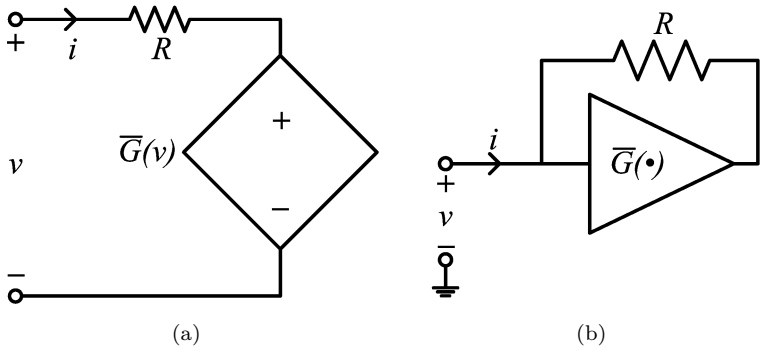


Figure 2.3. (a) Voltage-Dependent Voltage Source NRC Representation, (b) Ideal Amplifier NRC Representation

The derivative of i with respect to v is then

$$\frac{di}{dv} = \frac{1 - \bar{g}(v)}{R}, \tag{2.3}$$

where $\bar{g}(v)$ is the derivative, or slope, of $\bar{G}(v)$.

In order for the electrical networks in Figure 2.1(a) and 2.3(a) to have identical i/v characteristics, the derivative di/dv must be the same for both networks. Equating equations 2.1 and 2.3, it follows that

$$\frac{1 - \bar{g}(v)}{R} = -g(v). \tag{2.4}$$

For the network s to be identical, $\bar{g}(v)$ must be chosen as

$$\bar{g}(v) = Rg(v) + 1. \tag{2.5}$$

Using Figure 2.2, a plot of $\bar{g}(v)$ is constructed in Figure 2.4.

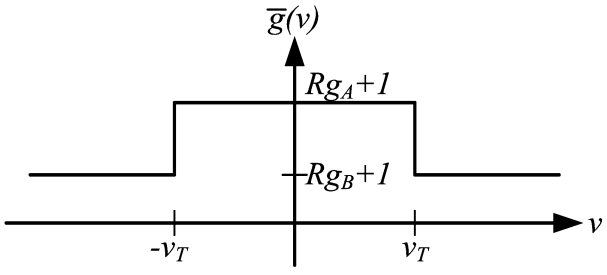


Figure 2.4. Slope of the Dependent Voltage Source

The required voltage-controlled voltage characteristic $\bar{G}(v)$ can be determined by integrating $\bar{g}(v)$, and is shown in Figure 2.5. Note that, when the input voltage reaches v_T, the gain $\bar{g}(v)$ of $\bar{G}(v)$ changes from $Rg_A + 1$ to $Rg_B + 1$.

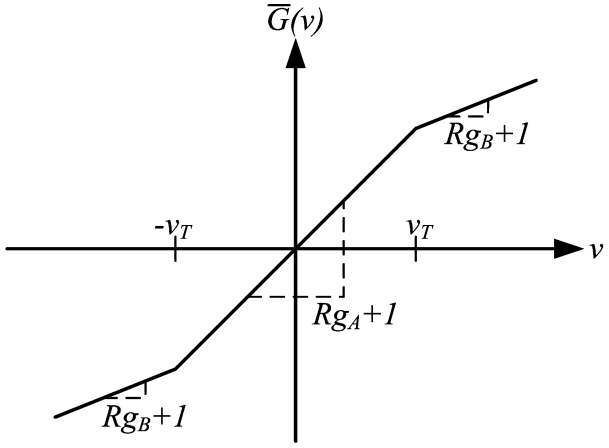


Figure 2.5. v/v Gain of Dependent Voltage Source

This chapter considers several NRCs whose active amplifying component is a FET. In these realizations, because the FET will not conduct for signals that cause their p-n junction to be reverse-biased, the characteristic $\bar{G}(v)$ only limits for one polarity of the input voltage. This means that the i/v characteristics in this chapter can not match the i/v characteristic shown in Figure 1.2, and should not be compared to it. Instead, their i/v characteristics will have two slopes and one nonlinearity. An example of this i/v characteristic shape is shown in Figure 2.6.

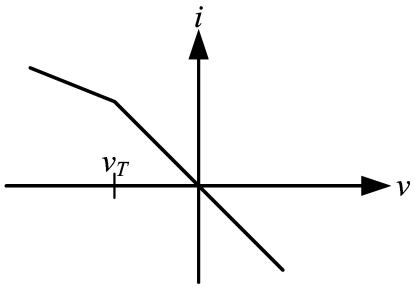


Figure 2.6. i/v Characteristic for an NRC Implemented with FETs

2.2 Lee and Choh's Marginal Oscillator Design

In Lee and Choh's marginal oscillator design, the authors never state how their circuit works, in particular, the nature of the nonlinear feedback mechanism required to sustain a steady-state oscillation. However, despite their failure to analyze their NRC's i/v characteristic or how it is affected by the values of the passive circuit components, they were able to achieve oscillation [10]. Even though it is not obvious how to adjust the potentiometers in Lee and Choh's circuit, their marginal oscillator is of interest as it yields the absorption spectra of a quadrapole interaction [11].

2.2.1 Circuit Model

In their marginal oscillator design, Lee and Choh employ the two N-Channel JFET circuit shown in Figure 2.7. The JFET Q_1 serves as a high input impedance amplifier that measures the voltage across the tuned circuit in the marginal oscillator. The second JFET, Q_2, serves as a limiter that reduces the overall gain of the two stage amplifier as the input voltage decreases. The output of Q_2 is fed back through a the series combination of C_2 and R to the input of the NRC. C_1 acts as a coupling capacitor at the circuit's input and C_2 acts a DC blocking capacitor at the two stage amplifier's output.

In order to obtain the i/v characteristic of Lee and Choh's NRC, their circuit is simulated using Multisim 11.0. The input v to the circuit is a sinusoidal signal with an amplitude of 0.25 V_{rms} and a frequency of 3 MHz. The Tektronix oscilloscope labeled XSC1 is configured to capture the input voltage v on channel 1 and the input current i using a current probe on channel 2. As the circuit is implemented using one FET for amplification and one FET for controlling the threshold voltage, the expected i/v characteristic should have two distinct slopes. Also, note that there are three potentiometers within the circuit labeled Key=A, Key=B, and Key=C. For convenience, they will henceforth be referred to by their letter only.

Lee and Choh describe the functionality of potentiometers B and C very briefly as a means for controlling the amplitude of the oscillation. They do not explain the function of potentiometer A, nor do they predict how the potentiometers will affect the characteristics of the NRC. However, because they were able to achieve stable oscillations with their oscillator, the effects of the potentiometers on the i/v characteristic is worthy of investigation [10].

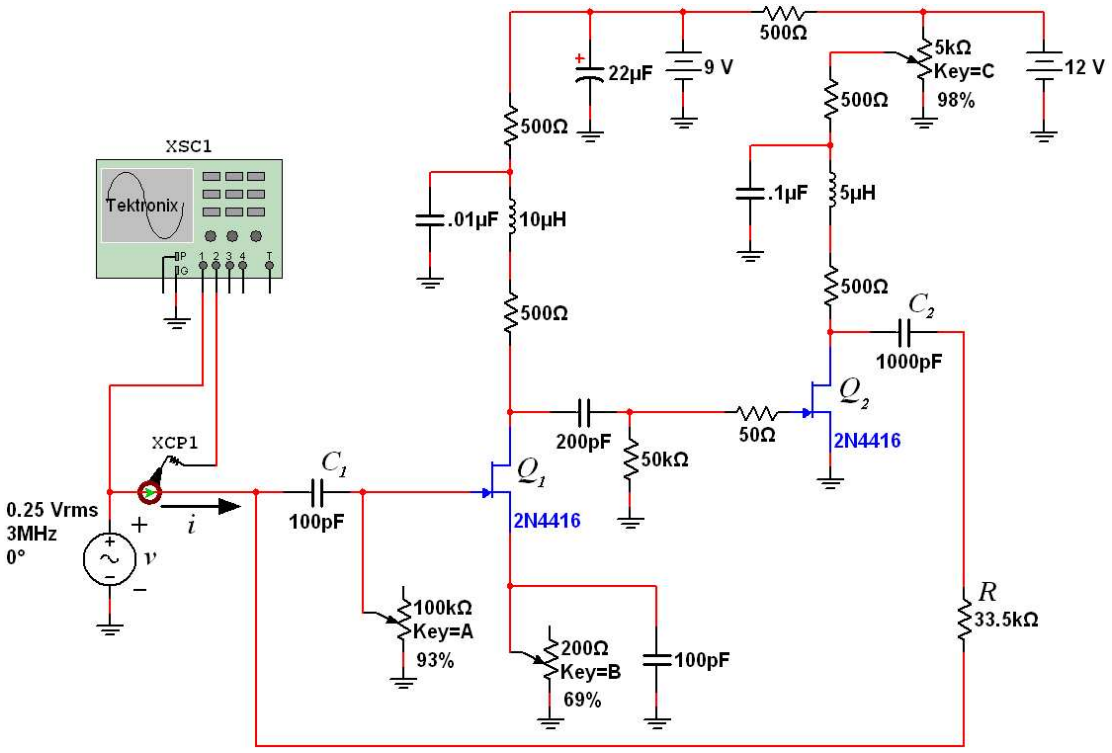


Figure 2.7. Multisim Schematic of Lee and Choh's NRC

2.2.2 Simulation Results

The i/v characteristic for Lee and Chohs NRC is shown in Figure 2.8. Although the i/v characteristic has opened, the slopes shown by tangent lines A and B are negative, indicating a negative resistance. In addition, these two slopes describe the generalized i/v characteristic predicted for FET NRCs. Further investigation reveals that each potentiometer appears to directly control these two slopes. However, they do not control the slopes independently, as adjustment of either potentiometer tends to affect the entire i/v characteristic. Lastly, potentiometer C controls the threshold voltage at which the slopes change.

2.2.3 Discussion

It is clear from Lee and Choh's writing that they did not study the shape of their NRC's i/v characteristic. This may be because they were redesigning a vacuum-tube oscillator using FETs, and since the previous circuit worked without a thorough knowledge of the NRC's i/v characteristic, they felt that it was not necessary to investigate. While the i/v characteristic shown in Figure 2.8

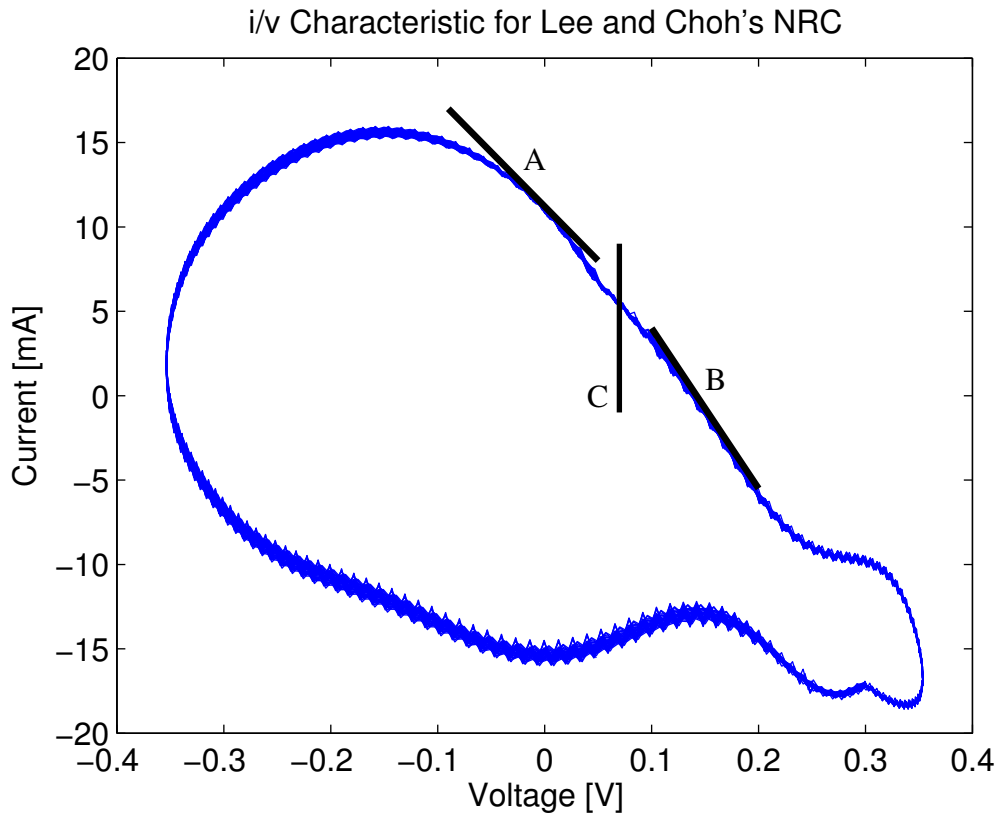


Figure 2.8. Simulated i/v Characteristic of Lee and Choh's NRC

exhibits a large phase shift, this does not preclude the use of the NRC in a marginal oscillator. Indeed, the circuit can be used to obtain the absorption spectra of a quadrapole interaction at 3.312 MHz. However, because of the extreme phase shift revealed by the i/v characteristic in Figure 2.8, the results of Viswanathan's analysis are unlikely to predict the conversion gain of Lee and Choh's marginal oscillator.

2.3 Viswanathan's Low Frequency Marginal Oscillator Design

Similar to Lee and Choh, Viswanathan also uses transistors to implement NRCs in two marginal oscillator circuits designed in her 1970 thesis. Unlike Lee and Choh, Viswanathan understood that the shape of the NRC's i/v characteristic was directly related to conversion gain. Further, Viswanathan was the first to analyze the effects of a two-segment i/v characteristic on conversion

gain [12].

To study the effects of a two-segment piecewise-linear NRC i/v characteristic on a marginal oscillator, Viswanathan designed a low-frequency circuit. This circuit also allowed her to demonstrate the ease of synthesis of a two-segment NRC. Unfortunately, she was never able to directly verify the i/v characteristic of the NRC component. She was, however, able to measure the sensitivity and effective bandwidth of the oscillator as a whole, and those values agreed with her predicted values within 5% [12].

2.3.1 Circuit Model

The Multisim schematic of Viswanathan's low-frequency NRC is shown in Figure 2.9. In Viswanathan's design, the input voltage v is sensed by the transistors T_2 and T_3, which are connected in a Darlington pair configuration. The 18 kΩ resistor connected to T_3's emitter results in a collector current that is proportional to the input voltage v. The transistor T_1 acts as a current source which can be controlled by potentiometer A. The difference between the current flowing through T_1 and the Darlington pair flows into the diodes, which will conduct alternately depending on the magnitude of v. As a result, Viswanathan posits that potentiometers B and C can be used to control the slope of each segment in $G(v)$ independently, and that potentiometer A will adjust the threshold voltage. Transistors T_6 and T_7 form a voltage-dependent current source that determines the input current i at the input of the NRC [12].

Viswanathan's NRC is simulated with a sinusoidal input signal v with an amplitude of 0.5 V_{rms} and a frequency of 1 kHz. Though low, this frequency is still significantly higher than the frequency at which Viswanathan studied the circuit [12]. The Tektronix oscilloscope labeled XSC1 is configured to capture the input voltage v on channel 1 and the input current i using a current probe on channel 2.

2.3.2 Simulation Results

The i/v characteristic of Viswanathan's low-frequency NRC is shown below in Figure 2.10. Only a cursory glance is required to verify that the i/v characteristic is two-segment piecewise-linear, that it has a negative slope, and that it has virtually no phase shift. Further investigation reveals that potentiometer B independently controls the lower slope while potentiometer C independently

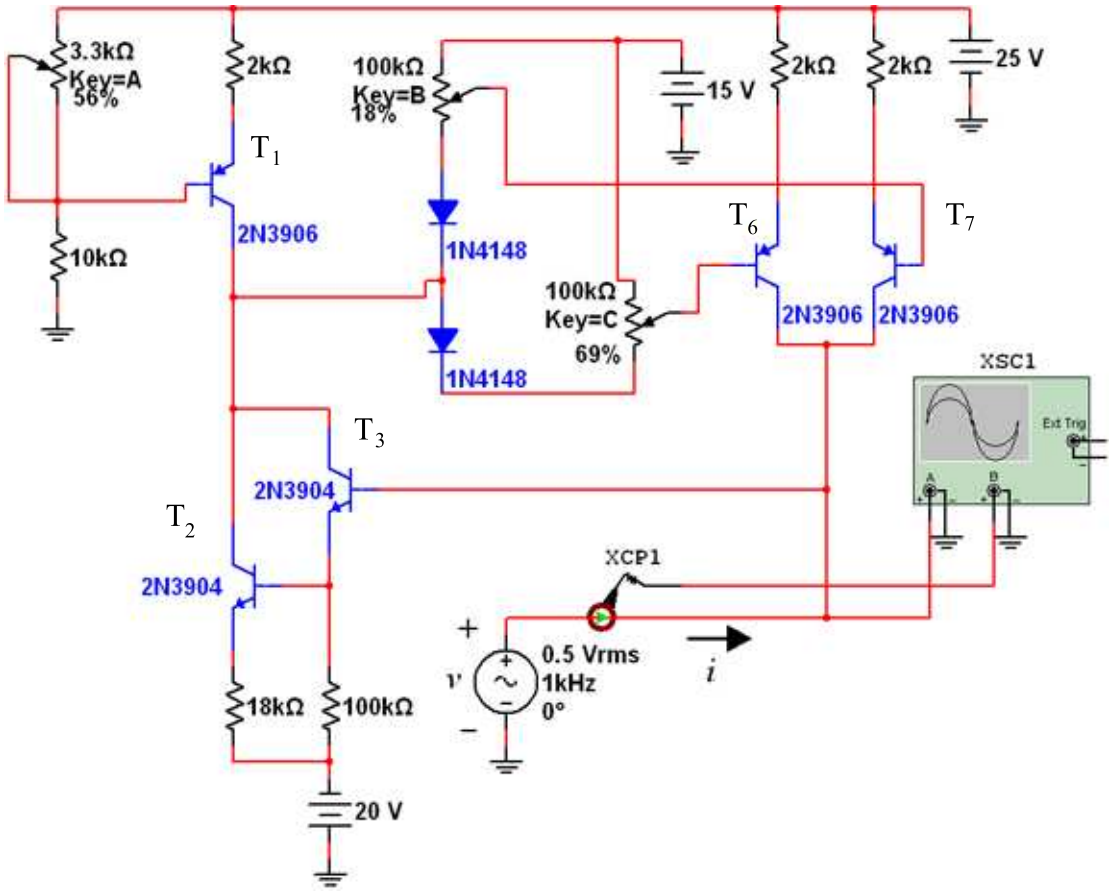


Figure 2.9. Multisim Schematic of Viswanathan's Low-Frequency NRC

adjusts the upper slope without affecting the threshold voltage. Increasing potentiometer A decrease the threshold voltage, though the effective range is very narrow. A small change in potentiometer A has a large effect on the threshold voltage.

2.3.3 Discussion

It is undeniable that Viswanathan's low-frequency NRC behaves exactly as she intended. It is piecewise-linear with two slopes g_A and g_B separated by a nonlinearity at v_T. The two slopes and the threshold voltage are independently adjustable by the potentiometers designed for that purpose. Though well-designed, Viswanathan's low-frequency NRC has the drawback that a phase shift becomes evident at frequencies as low as 20 kHz.

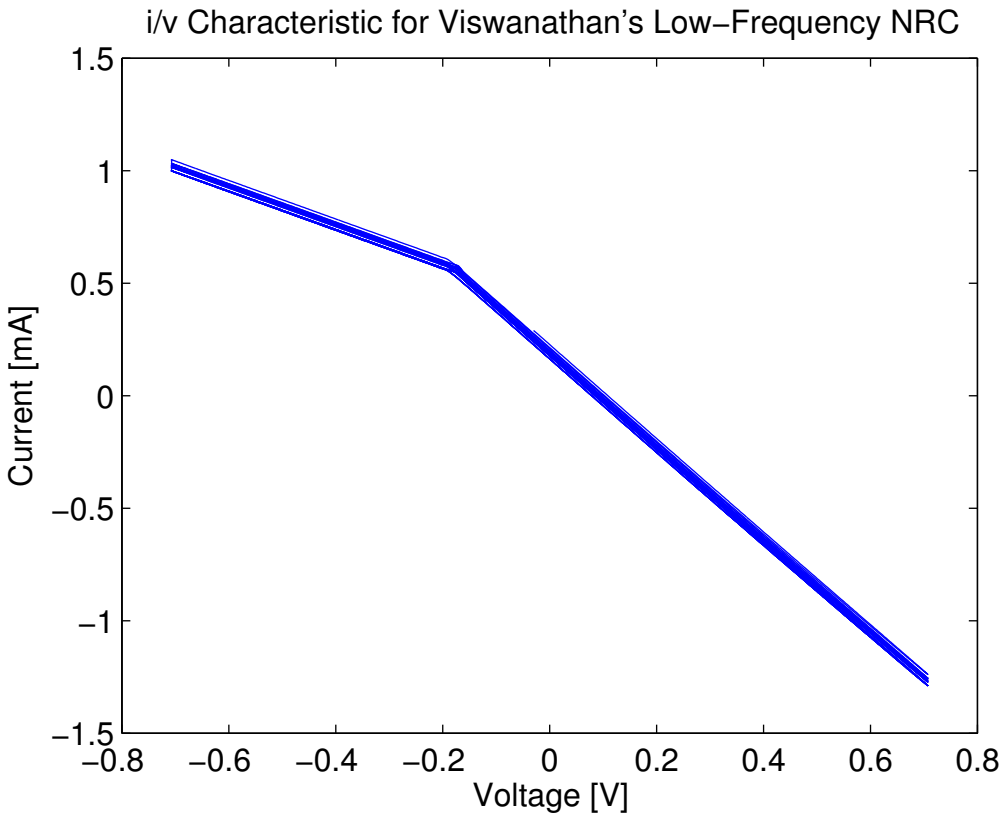


Figure 2.10. Simulated i/v Characteristic of Viswanathan's Low-Frequency NRC

2.4 Viswanathan's High Frequency Marginal Oscillator Design

The second NRC design presented in Viswanathan's 1970 thesis is a high-frequency configuration that is part of a 3 MHz oscillator-detector circuit. Like her low-frequency NRC, Viswanathan's high-frequency NRC is designed to have an i/v characteristic that has two distinct slopes. However, Viswanathan's high-frequency design differs from her low-frequency design in two ways. First, its active components are FETs rather than bipolar junction transistors (BJTs). Furthermore, Viswanathan states that the i/v characteristic will have a smooth nonlinearity as opposed to the piecewise-linear nonlinearity exhibited by her low-frequency NRC [12].

2.4.1 Circuit Model

The Multisim schematic of Viswanathan's high-frequency NRC is shown below in Figure 2.11. The circuit shown in Figure 2.11 differs from Viswanathan's original circuit in a small way. The transistors used for T_3 and T_4 are not the same part as that utilized by Viswanathan, because Multisim did not have the original parts in its database. However, the simulated transistors are both P-Channel switches with device parameters very close to the actual part used by Viswanathan.

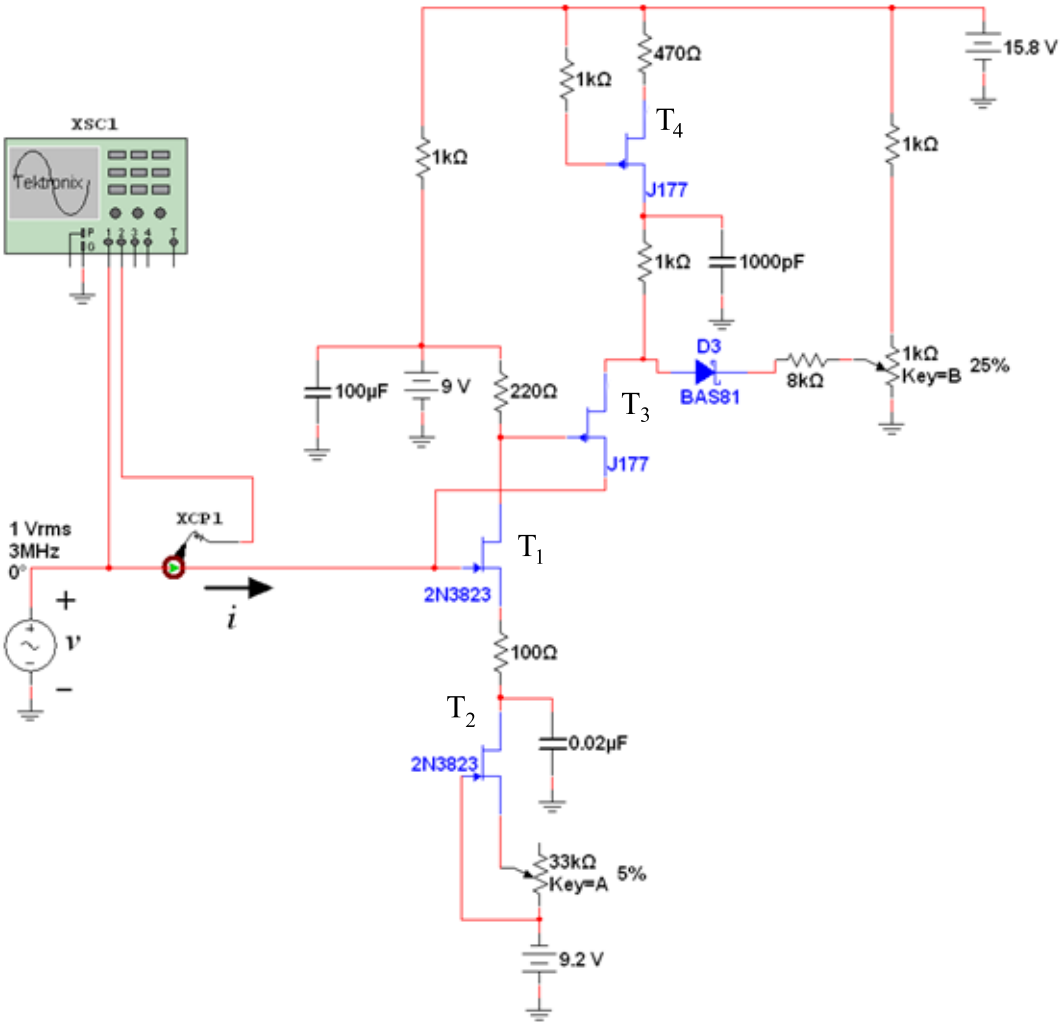


Figure 2.11. Multisim Schematic of Viswanathan's High-Frequency NRC

Viswanathan's high-frequency NRC operates by sensing the input voltage v on the gate of T_1. Potentiometer A and T_2 control T_1's bias current, while the 100 Ω resistor in T_1's source results in a linear relationship between the drain current of T_1 and the input voltage v. This drain current

establishes a voltage across the 220 Ω resistor which is sensed by the gate of T_3. Again, the 1 kΩ resistor in T_3's source establishes a linear relationship between the gate voltage and drain current while T_4 is used for biasing. To achieve positive feedback, T_3 inverts the signal at the drain of T_1. When the voltage at T_3's source goes above the voltage established by potentiometer B, the diode conducts and forms a shunt path across the 1 kΩ resistor. This shunt causes a slight reduction in loop gain, which results in a nonlinearity [12].

Viswanathan's high-frequency NRC is simulated with a sinusoidal input signal v with an amplitude of 1 V_{rms} and a frequency of 3 MHz. The Tektronix oscilloscope labeled XSC1 is configured to capture the input voltage v on channel 1 and the input current i using a current probe on channel 2.

2.4.2 Simulation Results

Viswanathan's high-frequency NRC i/v characteristic is shown in Figure 2.12. Despite a phase shift between input voltage and input current, the i/v characteristic clearly has two distinct slopes and a smooth nonlinearity.

Viswanathan's high-frequency NRC contains two potentiometers. Increasing potentiometer A has two effects. First, it appears to increase the threshold voltage, although it is difficult to tell due to the smoothness of the nonlinearity. Second, the entire i/v characteristic rotates counter-clockwise, making both the upper and the lower slope less negative. Increasing potentiometer A to its maximum value results in an i/v characteristic that is essentially a horizontal line. Potentiometer B appears to exclusively alter the lower slope, and hence the value of g_A. However, this effect is minimal, as large changes in potentiometer B seem to have a small effect on the slope.

2.4.3 Discussion

As with her low-frequency NRC, the i/v characteristic of Viswanathan's high-frequency NRC looks exactly as she predicted. It has two distinct negative slopes separated by a smooth nonlinearity. Again, one can only assume that Viswanathan did not simulate her NRC due to the lack of simulation tools at the time.

The drawbacks of the circuit are two-fold. First, there is a significant phase shift present at

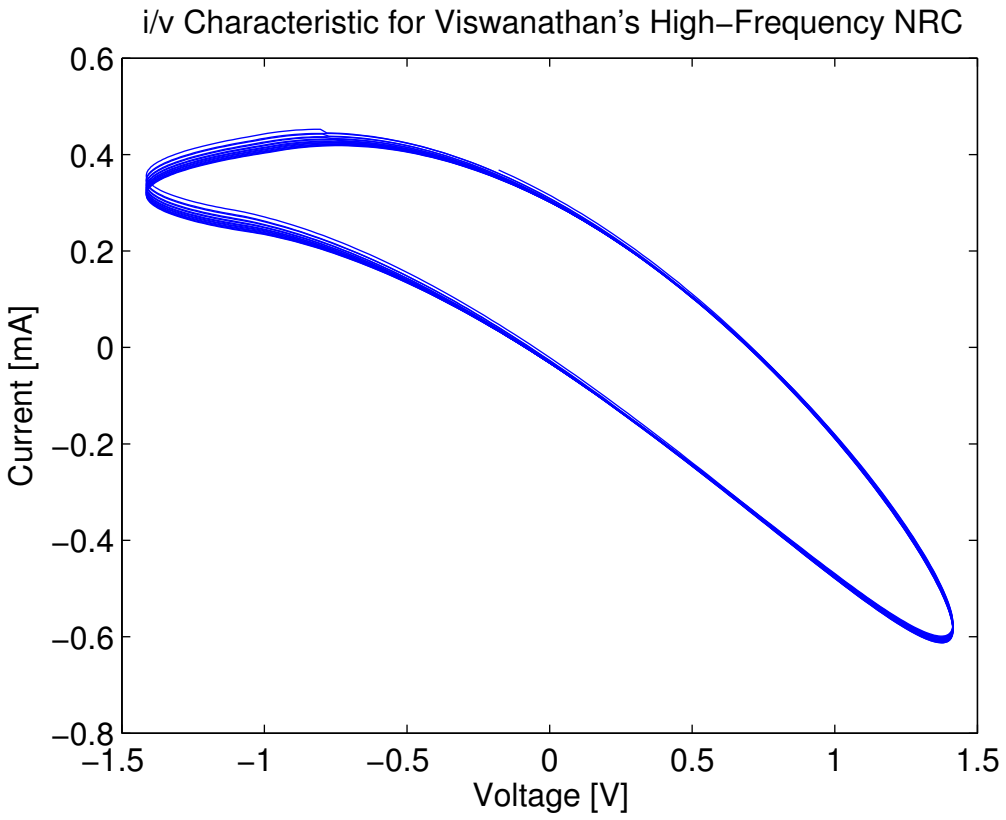


Figure 2.12. Simulated i/v Characteristic of Viswanathan's High-Frequency NRC

3 MHz which only becomes larger as the input signal frequency is increased. Second, it does not appear that Viswanathan intended for the parameters of her NRC's i/v characteristic to be adjustable. While it is possible to alter the shape of the i/v characteristic, potentiometer A controls all three parameters at once, while potentiometer B seems to alter very little at all. Instead, it seems that Viswanathan designed this oscillator for a specific application, and potentiometers A and B are simply present for fine-tuning.

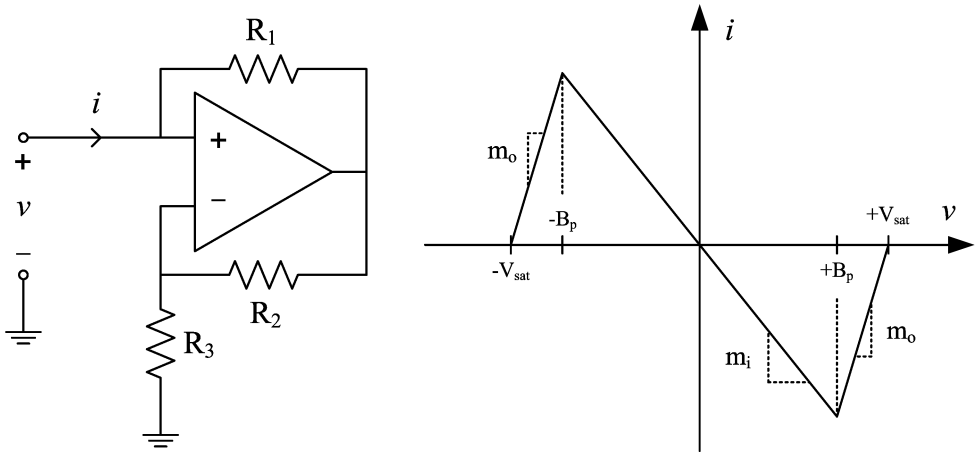
2.5 Chua's Negative Resistance Converter

Chua created a nonlinear negative resistor as part of an autonomous chaotic circuit [8]. His design is simple and elegant, as it uses only two operational amplifiers and six resistors. This is possible because Chua achieves the nonlinearity in his NRC by taking advantage of the inherent nonlinear characteristics already present in operational amplifiers. By combining two single operational

amplifier NRCs in parallel, Chua realized a symmetrical nonlinear i/v characteristic with one inner amplifying region and two outer limiting regions. What's more, Chua demonstrated that the parameters of the i/v characteristic are dependent directly on the values of the six resistors [13].

2.5.1 Circuit Model

The building block of Chua's nonlinear negative resistor is the single operational amplifier circuit shown in Figure 2.13(a). For the derivation of the i/v characteristic, the operational amplifier is assumed to be ideal, to have zero offset voltage, and to have saturation levels that are equal in magnitude. The resulting i/v characteristic is shown in Figure 2.13(b). The middle segment of the i/v characteristic represents the linear region of operation for the operational amplifier, while the two outer segments represent the positive and negative saturation regions of operation.



(a) (b)

Figure 2.13. (a) Chua's Single Operational Amplifier NRC, (b) i/v Characteristic of Chua's Single Operational Amplifier NRC

The slopes and breakpoints on the i/v characteristic shown in Figure 2.13(b) can be derived easily using Ohm's Law. The input current to the NRC is

$$i = \frac{v - v_o}{R_1}, \tag{2.6}$$

where v_o is the voltage at the operational amplifier's output terminal. In the linear operating

region, the gain equation for a non-inverting operational amplifier is

$$v_o = \left(1 + \frac{R_2}{R_3}\right) v. \tag{2.7}$$

Combining equations 2.6 and 2.7 to eliminate v_o yields

$$i = -\frac{R_2}{R_1 R_3} v. \tag{2.8}$$

In the positive saturation region, $v_o = +V_{sat}$. Substituting this into equation 2.6 results in

$$i = \frac{v}{R_1} - \frac{V_{sat}}{R_1}. \tag{2.9}$$

Similarly, in the negative saturation region, $v_o = -V_{sat}$, and equation 2.6 becomes

$$i = \frac{v}{R_1} + \frac{V_{sat}}{R_1}. \tag{2.10}$$

The breakpoints can be obtained by equating the current in the linear operating region to the current in the saturation operating region. This results in

$$\pm B_p = \pm \frac{R_3}{R_2 + R_3} V_{sat}. \tag{2.11}$$

From the above equations, the characteristics of Figure 2.13(b) are

$$m_i = -\frac{R_2}{R_1 R_3}, \tag{2.12}$$

$$m_o = \frac{1}{R_1}, \tag{2.13}$$

$$\pm B_p = \pm \frac{R_3}{R_2 + R_3} V_{sat}. \tag{2.14}$$

In order to use Chua's approach to obtain the i/v characteristic in Figure 1.2, it is necessary to use an additional operational amplifier to set the slope of the outer segments of $G(v)$.

Figure 2.14 shows two single operational amplifier NRCs connected in parallel to form Chua's NRC. All of the operational amplifier assumptions made in the preceding analysis are made here. Further, assume that both operational amplifiers are identical, and therefore have the

same saturation voltages. When an input voltage v is applied to the parallel combination, the input current i is the sum of the current drawn by each individual operational amplifier. In other words, $i = i_1 + i_2$. In this way, the overall i/v characteristic of Chua's NRC is obtained by summing the i/v characteristics of each operational amplifier. This is shown graphically in Figure 2.15. The top two graphs represent the i/v characteristics of each operational amplifier individually, while the bottom graph represents the overall i/v characteristic of Chua's NRC.

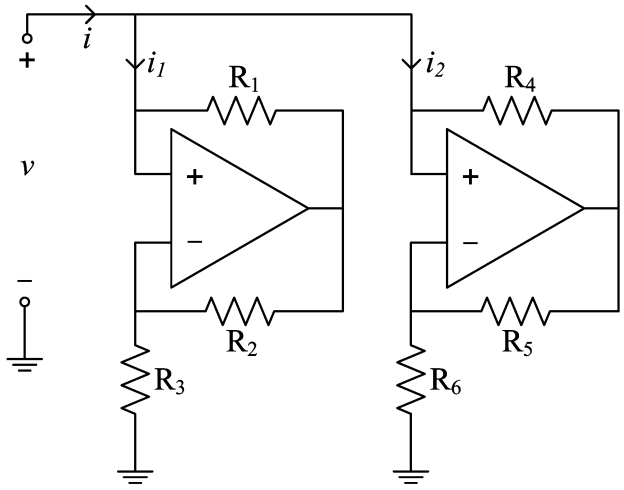


Figure 2.14. Chua's Dual Operational Amplifier NRC

Since the overall i/v characteristic in Figure 2.15 is the sum of the individual NRC's i/v characteristics, it follows that the overall slope is simply the sum of the individual slopes. Therefore,

$$g_A = m_{i1} + m_{i2} = -\frac{R_2}{R_1 R_3} - \frac{R_5}{R_4 R_6}, \tag{2.15}$$

$$g_B = m_{i1} + m_{o2} = -\frac{R_2}{R_1 R_3} + \frac{1}{R_4}, \tag{2.16}$$

and the threshold voltage occurs at

$$v_T = B_{p2} = \frac{R_6}{R_5 + R_6}. \tag{2.17}$$

As long as the magnitude of the input voltage remains less than B_{p1}, the i/v characteristic for Chua's NRC has exactly the same shape as the ideal i/v characteristic presented in Figure 1.2.

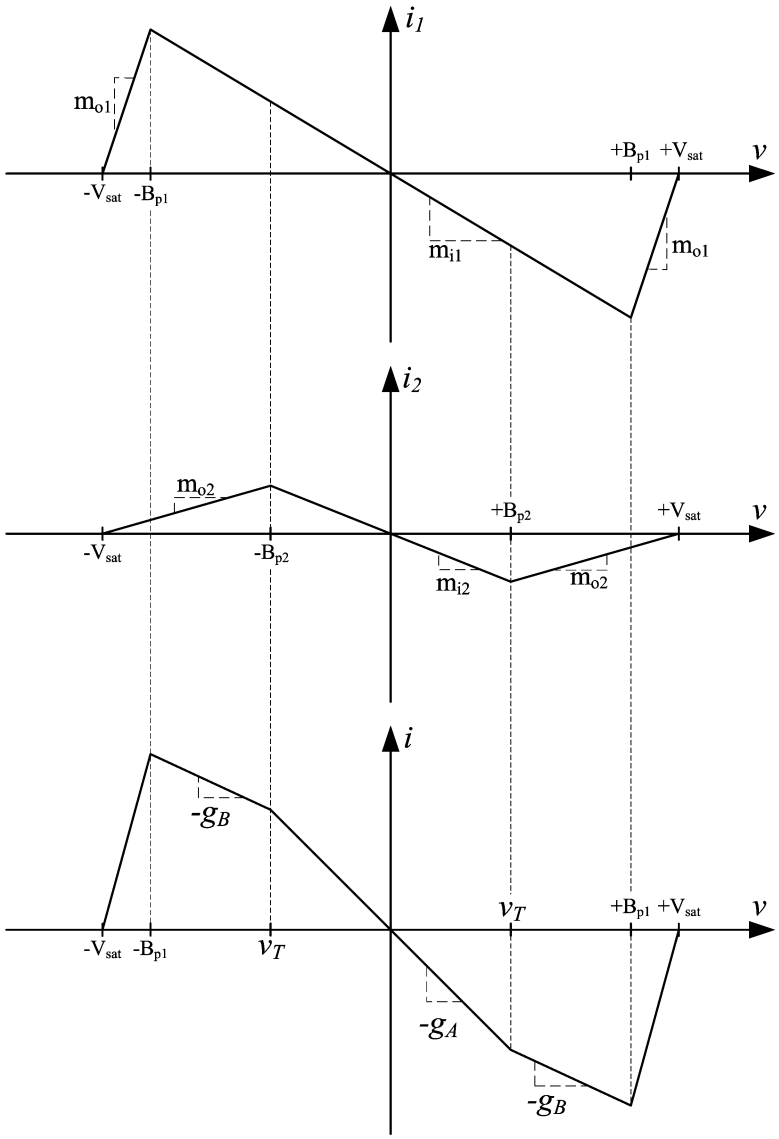


Figure 2.15. Combination of Two Single Operational Amplifier NRC i/v Characteristics to Produce Desired Nonlinear NRC i/v Characteristic

2.5.2 Discussion

Chua's NRC has several positive attributes. Its simple topology affords a nonlinear i/v characteristic with a minimum of components. This makes implementation trivial. Even the single operational amplifier NRC circuit configuration is useful, and can be used in conjunction with another topology to obtain a nonlinear NRC.

However, Chua's NRC is impractical for a couple of reasons. First, the i/v characteristic

parameters depend on several resistors. For example, the slope g_A depends on resistors R_1 through R_6, the slope g_B depends on resistors R_1 through R_4, and the threshold voltage v_T depends on resistors R_5 and R_6. As a result, any change in g_A will affect both g_B and v_T, making it impossible to adjust the parameters independently. Second, to obtain values of g_A and g_B on the order of μS using Chua's NRC, many of the resistors would have to be in the range of hundreds of kΩ. At the frequency of interest in this study, large resistors are undesirable as they form low-pass filters with stray capacitance.

2.6 Summary

This chapter shows how to implement an NRC using either a voltage-controlled current source or a voltage-dependent voltage source. Using this understanding, the i/v characteristics of three NRC designs were considered.

Lee and Choh implemented an NRC using FETs as part of a marginal oscillator design. Though they did not explicitly design for or investigate their NRC's i/v characteristic, they were able to create a marginal oscillator. A simulation of their NRC revealed that its i/v characteristic is negatively sloped, nonlinear, and has a significant widening of the eye. The slopes appear to be adjustable using passive circuit components.

Viswanathan designed two FET NRCs in her 1970 thesis. Though she did not simulate or experimentally observe the i/v characteristic of either of her NRCs, her analysis of her NRC accurately predicts what it should be. Simulation of her low-frequency NRC revealed that it has exactly the shape predicted by her analysis, and that the parameters of the curve were independently adjustable using passive circuit components. Its main drawback was that it only works at very low frequencies. Above 20 kHz, the eye opens up completely. The issue of the widening eye is also present in her high-frequency NRC. Also, her high-frequency NRC was not nearly as tunable as its low-frequency counterpart. It appears that it was designed to have a specific set of parameters, and is only slightly tunable in that narrow range.

Chua's NRC is the most recent and by far the most relevant to this thesis. Its simple operational amplifier design lends itself easily to synthesis and analysis. Using only two operational amplifier and six resistors, Chua was able to generate an i/v characteristic that is piecewise-linear, that has an inner amplifying region, and an outer limiting region. Unfortunately, Chua's dual

operational amplifier design is not useful for the QR lab at Penn State for two reasons. First, its i/v characteristic parameters are related to the values of the passive circuit components in a complex way which makes it difficult to tune or experiment on. Second, the resistors necessary to achieve typical g_A and g_B values are much too large for use at high frequencies. However, though Chua's dual operational amplifier NRC is not directly helpful, the single operational amplifier NRC building block is a good start towards creating the desired NRC.

Chapter 3

Design and Analysis of an NRC

3.1 Circuit Topology

As discussed in Section 2.1, an NRC with a single slope can be achieved using an ideal amplifier and a feedback resistor as shown in Figure 2.3(b). The operational amplifier is an excellent practical amplifier choice, as it has near-infinite input impedance and near-zero output impedance. In the non-inverting configuration, the operational amplifier's gain is positive and greater than unity, making it an ideal starting point for an NRC design. Figure 3.1 is a simple NRC realized using an operational amplifier in the non-inverting configuration. Resistor R_1 provides the feedback between the input and output of the operational amplifier. Resistors αR_2 and R_2 control

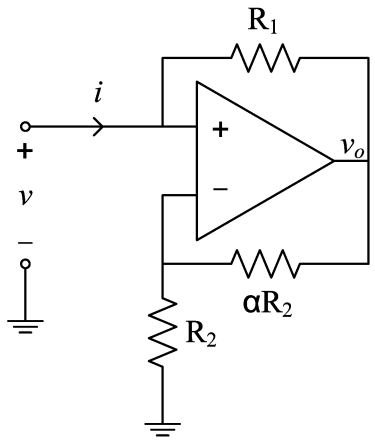


Figure 3.1. Simple NRC Realized Using an Operational Amplifier in the Non-Inverting Configuration

the operational amplifier's gain, which can be expressed as

$$v_o = \left(1 + \frac{\alpha R_2}{R_2}\right) v = (1 + \alpha)v. \tag{3.1}$$

Using Ohm's Law and some algebra, the current can be expressed as

$$i = -\frac{\alpha R_2}{R_2}\frac{1}{R_1}v = -\frac{\alpha}{R_1}v. \tag{3.2}$$

This makes the operational amplifier's gain an important design feature, since the value of α can be used to make the conductance of the circuit smaller without having to use large resistors in the feedback path. Note that the circuit configuration shown in Figure 3.1 and the i/v relationship derived in equation 3.2 exactly match the configuration and i/v relationship of the single operational amplifier NRC designed by Chua [13].

Though the starting point of the operational amplifier designed in this thesis is the same as Chua's, the final NRC cannot have the same configuration as the dual operational amplifier NRC explored in Chapter 2. Recall that, although the shape of the i/v characteristic was negative and piecewise-nonlinear, the attainable values of g_A and g_B were limited by resistor size. So, this thesis utilizes a different method of implementing a nonlinearity.

Consider the circuit shown in Figure 3.2. Assuming the two diodes are ideal, the left-most diode will conduct when the output voltage v_o is less than $-v_B$ and the right-most diode will conduct when $v_o > v_B$. When either of the diodes is conducting, current can flow through R_4. The combination of R_3 at the output of the operational amplifier and the pull-down resistor R_4 creates a voltage divider. This voltage divider effectively decreases the amount of current in R_1, causing a reduction in the slope of the NRC's i/v characteristic. When the output voltage magnitude is less than $|v_B|$, the circuit will behave like the circuit shown in Figure 3.1, with the series combination of R_1 and R_3 providing the feedback between the output and input of the operational amplifier.

The batteries from Figure 3.2 can be implemented with analog circuit components as shown in Figure 3.3. Resistors R_5 and R_7, and potentiometer R_6 create a simple voltage divider between the operational amplifier's supply rails, which allows the user to adjust the threshold voltage v_T. The threshold voltage is connected to operational amplifier U_2, which is configured as a voltage

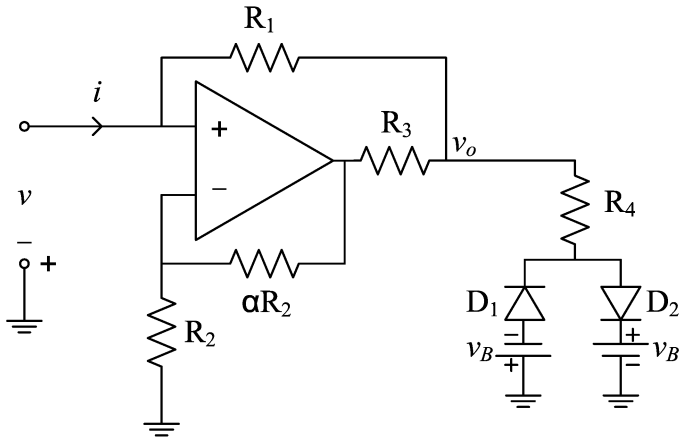


Figure 3.2. Simple NRC with a Nonlinear i/v Characteristic

follower. The output of U_2 is connected to D_1 through a low-valued resistor and also to the input of U_3. Op-amp U_3 is configured as an inverting amplifier. Choosing $R_8 = R_9$ will result in a gain of -1, so the output of U_3 will be equal in magnitude and opposite in sign to the output of U_2. Again, the output of U_3 is connected to D_2 through a low-valued resistor. The capacitors C_1 and C_2 provide a low-impedance path to ground for AC signals when the either of the diodes are conducting.

3.2 Analysis

In order to experimentally verify the designed NRC's i/v characteristic, it is necessary to determine how the parameters g_A, g_B, and v_T depend on the passive circuit components. The analysis of the proposed NRC is explored in this section in two parts. First, this section examines the exact relationship between the i/v characteristic parameters and the resistors in the circuit. Second, this section will explore what approximations can be made to simplify the expressions with the goal of controlling g_A, g_B, and v_T independently with three separate potentiometers.

3.2.1 Exact Analysis

The analysis of the NRC must consider two distinct regions of operation. The first region occurs when $|v_o| < |v_T|$. In this case, neither diode conducts, and the input current i is given by the

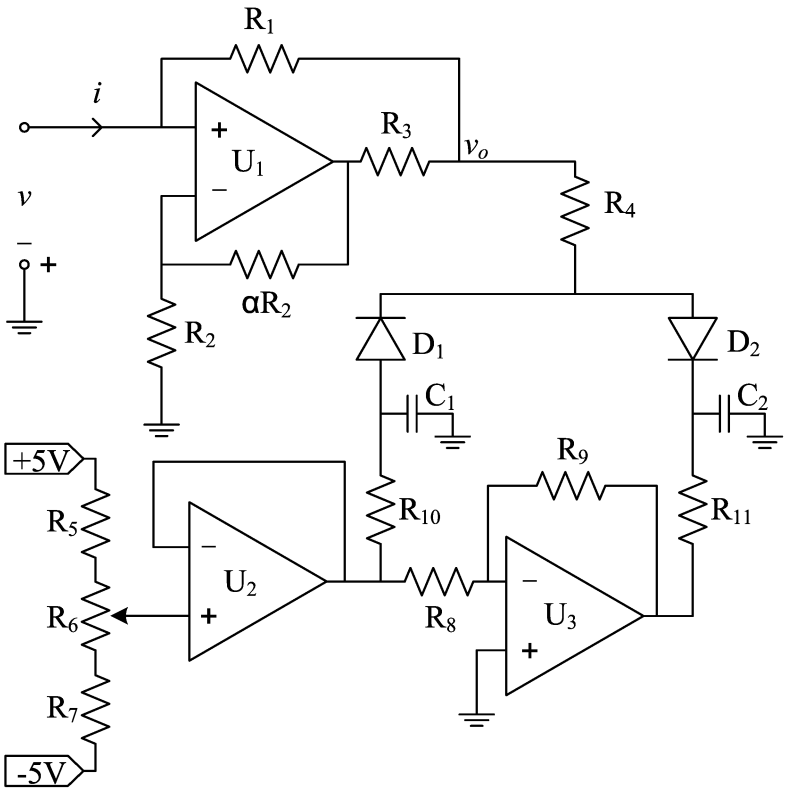


Figure 3.3. Nonlinear NRC - Diodes Biased With Operational Amplifiers

equation

$$i = \frac{v - \left(1 + \frac{\alpha R_2}{R_2}\right) v}{R_1 + R_3} = -\frac{\alpha R_2}{R_2} \frac{1}{R_1 + R_3} v = -\frac{\alpha}{R_1 + R_3} v. \tag{3.3}$$

Since g_A is the slope of the i/v characteristic in this region, it can be determined by taking the derivative of the current expression with respect to voltage. Thus, g_A can be written as

$$g_A = -\frac{di}{dv} = \frac{\alpha}{R_1 + R_3}. \tag{3.4}$$

As expected, the conductance $di/dv = -g_A$ is negative.

The second region of operation occurs when $|v_o| > |v_T|$. Using the argument that the i/v characteristic will be symmetrical, it is only necessary to consider $v_o > v_T$. The slope of the i/v characteristic in that region will be the same as for $v_o < v_T$. To begin the analysis, again assume that the diode's forward voltage drop is 0 V. Then, the equation for the input current i can be

derived using Ohm's Law and KCL using

$$v_o = v - iR_1, \tag{3.5}$$

and

$$\frac{v_o - v}{R_1} + \frac{v_o - (1+\alpha)v}{R_3} + \frac{v_o - v_B}{R_4} = 0. \tag{3.6}$$

Substituting Equation 3.5 into Equation 3.6 yields

$$-i\left(1 + \frac{R_1}{R_3} + \frac{R_1}{R_4}\right) + v\left(\frac{1}{R_5} - \frac{\alpha}{R_4}\right) - \frac{v_B}{R_5} = 0. \tag{3.7}$$

Because g_B is the slope of the i/v characteristic in this region, it can be determined by taking the derivative of i with respect to v. The resulting expression is

$$-\frac{di}{dv}\left(1 + \frac{R_1}{R_3} + \frac{R_1}{R_4}\right) + \left(\frac{1}{R_4} - \frac{\alpha}{R_3}\right) = 0. \tag{3.8}$$

Rearranging this expression results in

$$g_B = \frac{di}{dv} = \frac{\alpha R_4 - R_3}{R_1R_4 + R_3R_4 + R_1R_3}. \tag{3.9}$$

Using equation 3.4, the expression for g_B can also be written in terms of g_A as

$$\begin{aligned} g_B &= \frac{\alpha}{R_1 + R_3}\frac{(R_1 + R_3)\left(1 - \frac{R_3}{\alpha R_4}\right)}{R_1 + R_3 + \frac{R_1R_3}{R_4}} \\ &= g_A\frac{(R_1 + R_3)\left(1 - \frac{R_3}{\alpha R_4}\right)}{R_1 + R_3 + \frac{R_1R_3}{R_4}} \end{aligned} \tag{3.10}$$

This expression demonstrates that the relationship between g_B and g_A is complicated and affected by all of the passive circuit components.

3.2.2 Approximations

The expressions for g_A and g_B in the preceding subsection are much too complicated to make independent adjustment of those parameters easy. As such, it is necessary to make some approximations to simplify the equations for g_A and g_B. The main method for approximating the

above equations is to choose resistor values such that the ratios of resistors can be approximated as zero. Suppose that $R_1 \gg R_3$, $R_4 \gg R_3$ and $\alpha \approx 1/2$, where $\gg$ implies at least a ratio of 10:1. Then, Equations 3.4 and 3.10 simplify to

$$g_A \approx \frac{\alpha}{R_1} \tag{3.11}$$

and

$$g_B \approx \frac{\alpha}{R_1}\left(1 - \frac{R_3}{\alpha R_4}\right) = g_A\left(1 - \frac{R_3}{\alpha R_4}\right). \tag{3.12}$$

From the above approximations, it is now possible to choose two resistors to control g_A and g_B. It is immediately clear that it is impossible to vary g_A without also changing g_B. However, it is possible to change g_B without affecting g_A. Varying R_3 or R_4 will primarily affect g_B, and should have little effect on g_A, while either R_1 or α can be used to vary g_A. Because the loop gain of the NRC is dependent on α, it makes sense to make R_1 a potentiometer to change g_A. Similarly, making R_3 a potentiometer allows for more direct control of g_B.

To compare the approximations for g_A and g_B to the exact values, it is necessary to choose values for resistors R_1 through R_4. Given that the effective parallel resistance of the tuned circuit is 60 kΩ, table 3.2.2 shows a set of standard resistance values that satisfy the design specifications for g_A and g_B.

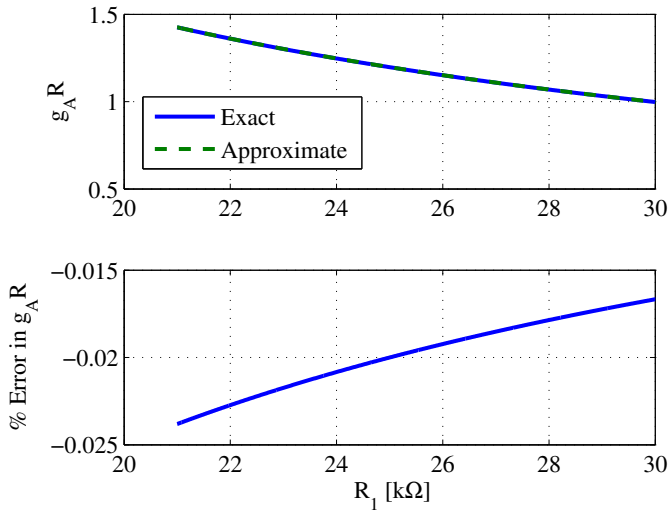
Element	Value
R_1	2.49 kΩ + 100 kΩ potentiometer
αR_2	249 Ω
R_2	499 Ω
R_3	2.2 Ω + 20 Ω potentiometer
R_4	50 Ω

Table 3.1. NRC Resistor Values

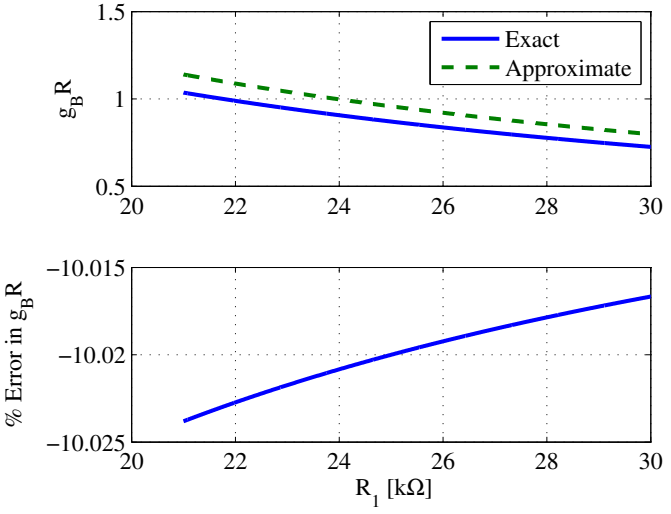
Resistor R_1 is such that it can be tuned using a potentiometer for independent control of g_A. Though it is tunable over a large range of resistance, care must be taken at higher resistances to avoid creating a low-pass filter with stray circuit capacitance. The values of resistors αR_2 and R_2 are chosen such that $\alpha = 0.5$. Like R_1, R_3 is chosen to be a potentiometer to provide a means for independent control of g_B. Note that the range of R_3 is not as large as R_1. This is because R_3 must remain smaller than both R_1 and R_4 in order for the approximations of g_A and g_B to remain valid. Resistor R_4 must be minimized because, in order for the diodes to switch quickly,

the resistance in series with them must be small.

Figure 3.4(a) show a comparison of the approximated and the exact values of g_A and g_B, respectively, over a range of R_1. For these comparisons, the value of R_3 is fixed at 5 Ω. Figure 3.4(a) demonstrates that the approximated value of g_A differs from the exact value by less than 0.5% over this range of R_1. Similarly, Figure 3.4(b) shows that the exact and approximated values of g_B differ by an approximately constant 10% over this range of R_1.



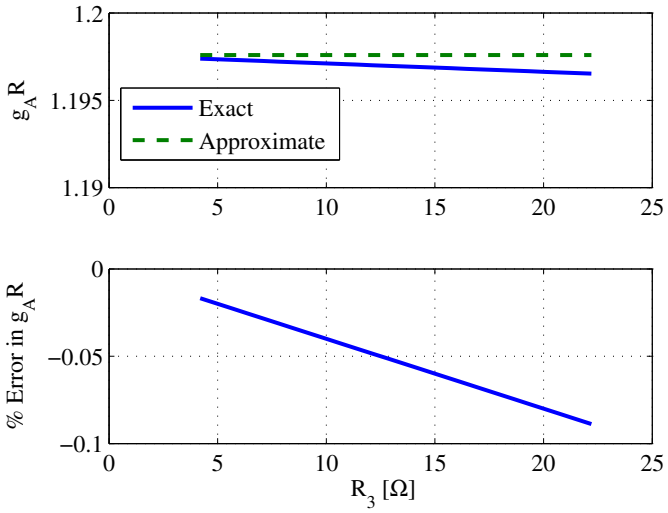
(a)



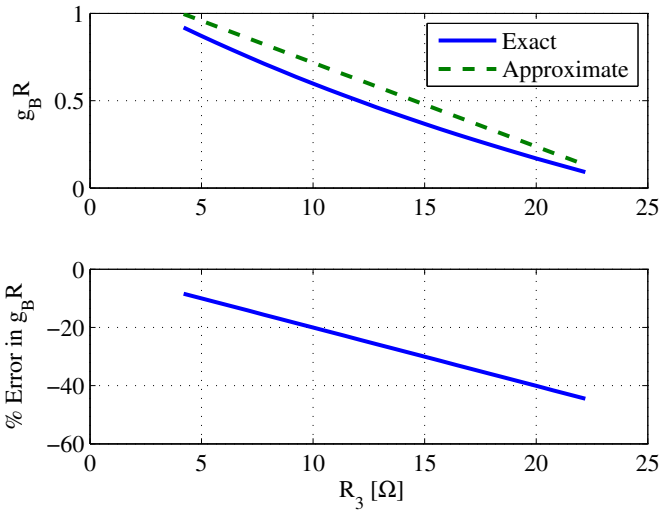
(b)

Figure 3.4. (a) Comparison of Approximate and Exact Predicted g_A Versus R_1, (b) Comparison of Approximate and Exact Predicted g_B Versus R_1

The same analysis is performed over the range of R_3 with R_1 fixed at 25 kΩ. Figure 3.5(a) shows that the approximation for g_A has an error of less than 0.1%. Figure 3.5(b) demonstrates that the approximation for g_B diverges from the exact value by a larger amount as R_3 is increased. However, for values of R_3 less than 5 Ω, the approximation for g_B is valid.



(a)



(b)

Figure 3.5. (a) Comparison of Approximate and Exact Predicted g_A Versus R_3, (b) Comparison of Approximate and Exact Predicted g_B Versus R_3

3.3 Component Selection

Figure 3.6 shows the final NRC design schematic. Note that the layout is nearly identical to that shown in Figure 3.3, with only a few minor differences. First, the resistor reference designators have changed from those used in the analysis section. Also, power connections for the operational amplifiers, along with filtering capacitors for those power rails, have been added. Last, various jumpers and test points have been incorporated to simplify the experimentation process. Jumper JP1 allows the user to add a resistor in series with the input of the NRC to aid in the process of measuring input current. Jumper JP2 is used to open and close the feedback path for open-loop and closed-loop operation.

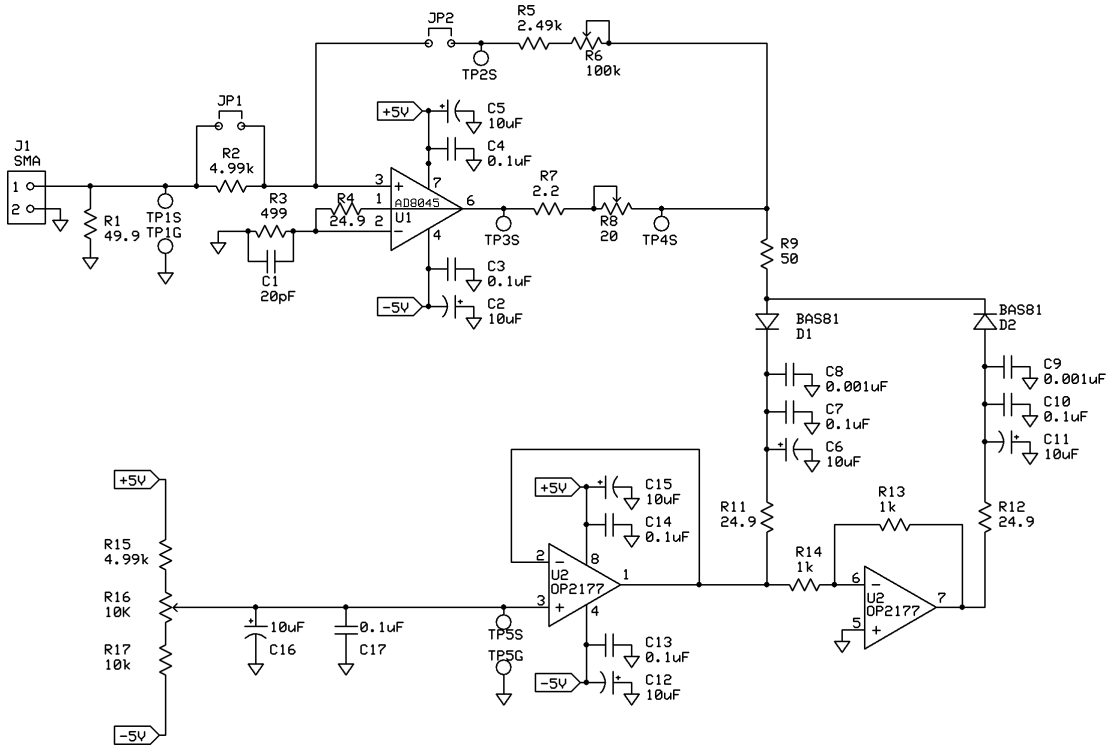


Figure 3.6. NRC Schematic

When selecting components for the NRC circuit, several factors determine the best choice. The main limitation on component choice is the need for little to no phase shift at high frequencies. Secondary limitations include circuit size, component mounting type, and ability to interface with the current QR system.

The component most affected by high-frequency operation is operational amplifier U1. The

design utilizes an AD8045, which is an ultralow distortion, high speed, voltage-feedback operational amplifier. Its high slew rate (1350 V/μs) and high bandwidth (1 GHz) make it an ideal choice for a high-frequency system. The AD8045 has the added benefit of being a surface-mount component, which will minimize stray capacitance and the board space it will occupy. Op-amps U2 and U3 are implemented using an OP2177. The OP2177 is a dual operational amplifier package, which again will minimize the board space it occupies. Unlike U1, U2 and U3 need not be high speed operational amplifiers, because they are used solely to implement a DC bias voltage for the diodes. The OP2177 is ideal for this purpose, as it is an ultra-precision amplifier with almost zero offset voltage.

Diodes D1 and D2 are implemented using two BAS81 series Schottky diodes. These diodes are chosen because they have a low forward-bias voltage drop and a low reverse-bias capacitance which allows them to switch on and off quickly. Also, these diodes are surface mount components that minimize board space and stray capacitance. Potentiometers R_6, R_8, and R_{16} are among the small group of through-hole components in the design. This is to provide more mechanical support so that extensive tuning does not break the component away from the board. The rest of the resistors and capacitors are all surface mount components to reduce circuit size and stray capacitance.

3.4 Numeric Simulation

Figure 3.7 shows the Multisim schematic used to simulate the proposed NRC design. Note that a capacitor is added in parallel with R_3 to further improve the phase shift of the simulated i/v characteristic. The values of the resistors were chosen to achieve typical values of g_A and g_B. Rather than simulate the voltage follower circuit, which is a known functional design, the threshold voltage was set using voltage sources with shunt capacitors to remove any AC component. The input voltage v to the circuit is a sinusoid with an amplitude of 1 V_{rms} and a frequency of 5 MHz. The Tektronix oscilloscope labeled XSC2 is configured to capture the input voltage v on channel 1 and the input current i using a current probe on channel 2.

Figure 3.8 shows the i/v characteristic for the NRC Multisim circuit in Figure 3.7. This plot demonstrates that the circuit can operate at 5 MHz with little to no phase shift between voltage and current. Also, note that the i/v characteristic has two nonlinearities equidistant from the

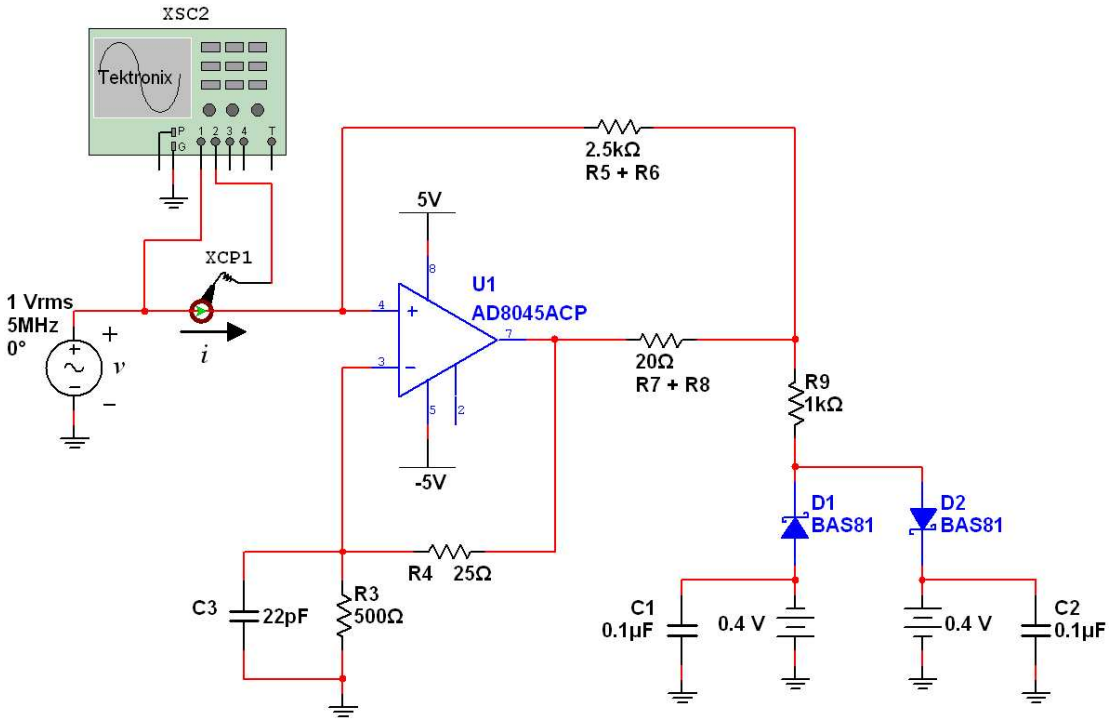


Figure 3.7. NRC Multisim Circuit Schematic

y-axis. The characteristic describes a negative resistance at every point on the curve, since the slope is everywhere negative. Though it is not shown here, simulations reveal that the inner slope can be adjusted using R_1 and the outer slope using R_4. These results provide confidence that a synthesized version of the circuit will function properly.

3.5 Discussion

The NRC designed in this thesis is similar to the basic NRC design utilized by Chua for his autonomous chaotic circuit. Unlike Chua, however, the nonlinearities in this NRC design are implemented using Schottky diodes which introduce a voltage divider at the output of the operational amplifier for voltages greater than or less than a tunable threshold voltage. Within the various regions of operation, it can be shown that the slopes g_A and g_B depend on the values of the passive circuit components in a complicated way. These complicated expressions can be easily simplified by intelligent choice of component values. This is desirable for this study, as it will make it much easier to tune the circuit during experimentation.

The other NRC components must also be chosen carefully. The main concern with the

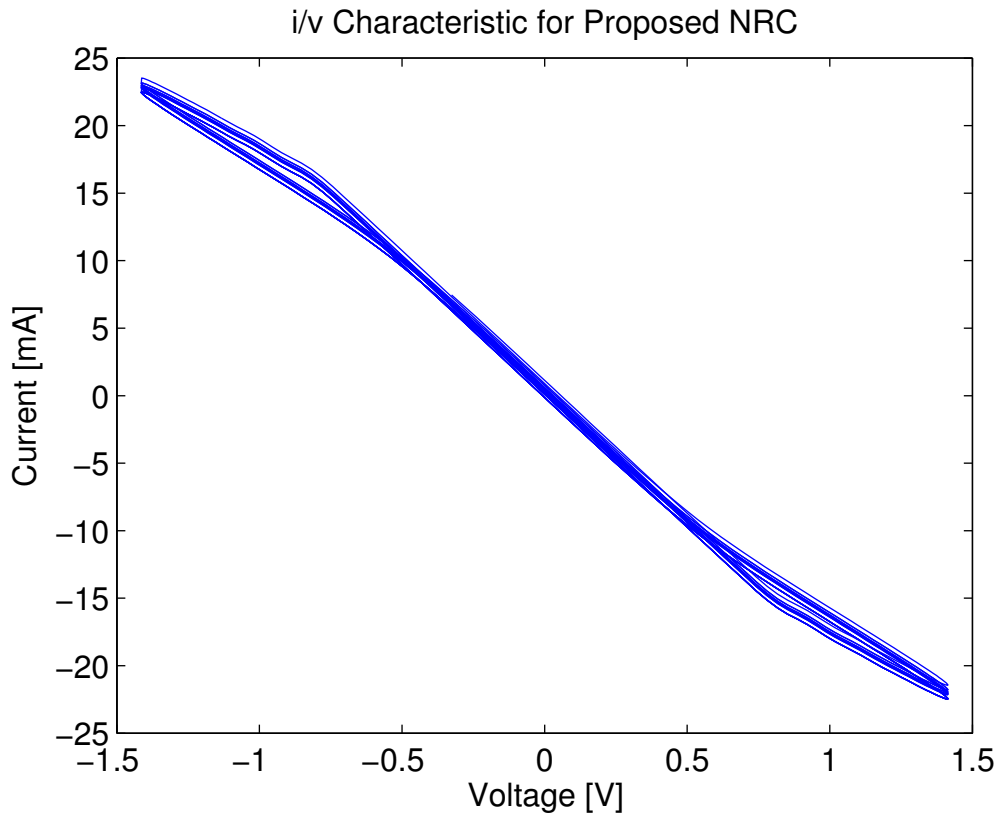


Figure 3.8. Simulated i/v Characteristic for the Proposed NRC Design

other components is how they will function at high frequencies. As such, components were chosen so that their operating range was greater than 5 MHz, and also so that their physical connections would not introduce stray capacitance into the NRC. To verify the final NRC design, it was created in Multisim and simulated with a typical input signal amplitude and frequency. The resultant i/v characteristic is piecewise-linear with an inner amplifying region and an outer limiting region, and has almost zero phase shift. The simulation also verified that the slopes of the i/v characteristic can in fact be adjusted independently. These results provide confidence that the synthesized circuit will meet the requirements of this thesis.

Chapter 4

Experimental Verification

4.1 Test Bed Description

The fully assembled NRC circuit is shown in Figure 4.1. The IC components were affixed using a solder reflow technique in conjunction with an industrial hot plate, while the rest of the components were soldered by hand. During this process, it was determined that future revisions of the circuit should utilize components with at least an 0805 footprint, as the much smaller 0402 components used in this design are difficult to work with. After completion of the circuit, its connections were checked using a DMM.

The physical test bed for the NRC is as follows. The NRC's ± 15 V supply rails will be powered by a DC power supply. A benchtop multimeter will be used to monitor the threshold voltage as measured at TP5. A 15 MHz function/arbitrary waveform generator will be connected to SMA J1 to provide an input sinusoid with an amplitude of 3 V_{pp} and a frequency of 5 MHz. Signals at various test points in the circuit will be measured using two channels of a 500 MHz oscilloscope. Data from the oscilloscope, function generator, and multimeter will all be acquired using LabView and manipulated using Matlab. In addition, potentiometer R_6 will be set to 22.5 kΩ and potentiometer R_8 will be set to 2.3 Ω.

To verify that the design specifications have been met, two experiments will be performed. The first is a measurement of the open-loop gain. For this experiment, the NRC will be connected as described above. Then, jumper JP2 will be removed, effectively removing the positive feedback from the NRC and creating an open-loop circuit. One oscilloscope probe will be connected to

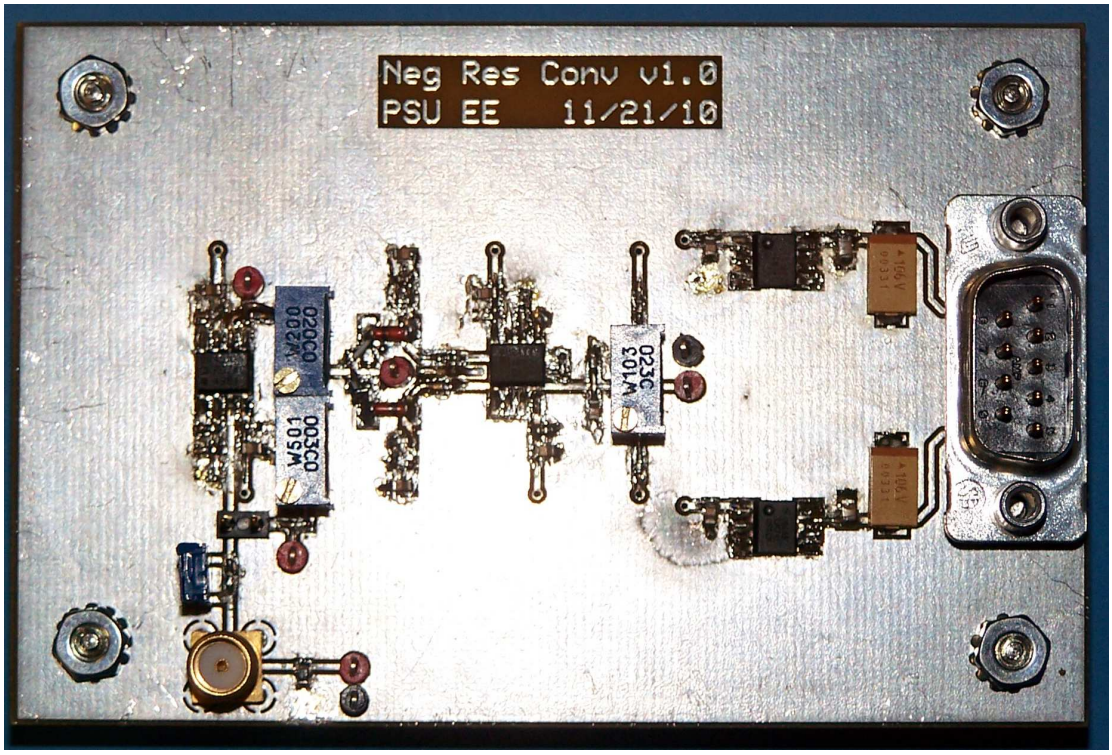


Figure 4.1. NRC Board

test point VTP1 to measure the input signal applied to the operational amplifier's non-inverting input. The second oscilloscope probe will be connected to test point VTP4 to measure the signal at the operational amplifier's output. This experiment will be used to determine both the positive gain of the NRC, as well as any phase shift between the input and output voltages of the operational amplifier.

The second experiment will be to generate a closed-loop plot of the circuit's output voltage versus its input voltage. This measurement is done in lieu of a direct i/v measurement for two reasons. First, a current probe is not available. Second, even if a current probe were available, the current that is flowing into the circuit is small, and so the resulting measrement signal to noise ratio is poor. Before measurements are taken using the oscilloscope, the values of potentiometers R_6 and R_8 must be measured and recorded. This is easiest when jumper JP2 is removed, as it isolates the feedback circuit. To measure the closed-loop gain, jumper JP2 must replaced so that the feedback loop is intact. One oscilloscope probe will be connected to test point VTP1 to measure the input signal and the operational amplifier's non-inverting input. The second oscilloscope probe will be connected to test point VTP4 to measure the signal at the

operational amplifier's output. This plot of the gain $\bar{g}(v)$ will then be used with the values of the potentiometers to calculate the the slopes $g(v)$ of the i/v characteristic as discussed in Section 2.1.

4.2 Open-Loop Gain Measurements

The primary purpose of the open-loop gain measurement is to determine the phase shift of the operational amplifier. This is accomplished by direct measurement of the signal at test point 1 (VTP1) and at test point 4 (VTP4). Measurements from the oscilloscope show a phase shift between the two signals of 1.139 ns $\pm$ 30 ps, which corresponds to 2.05° $\pm$ 0.054° at a frequency of 5 MHz. This is significantly less than the maximum acceptable phase shift desired by the QR lab at Penn State. The second technique is to plot the signals against one another to observe any opening of the eye. Figure 4.2 shows a plot of VTP4 versus VTP1 generated using data captured from the oscilloscope.

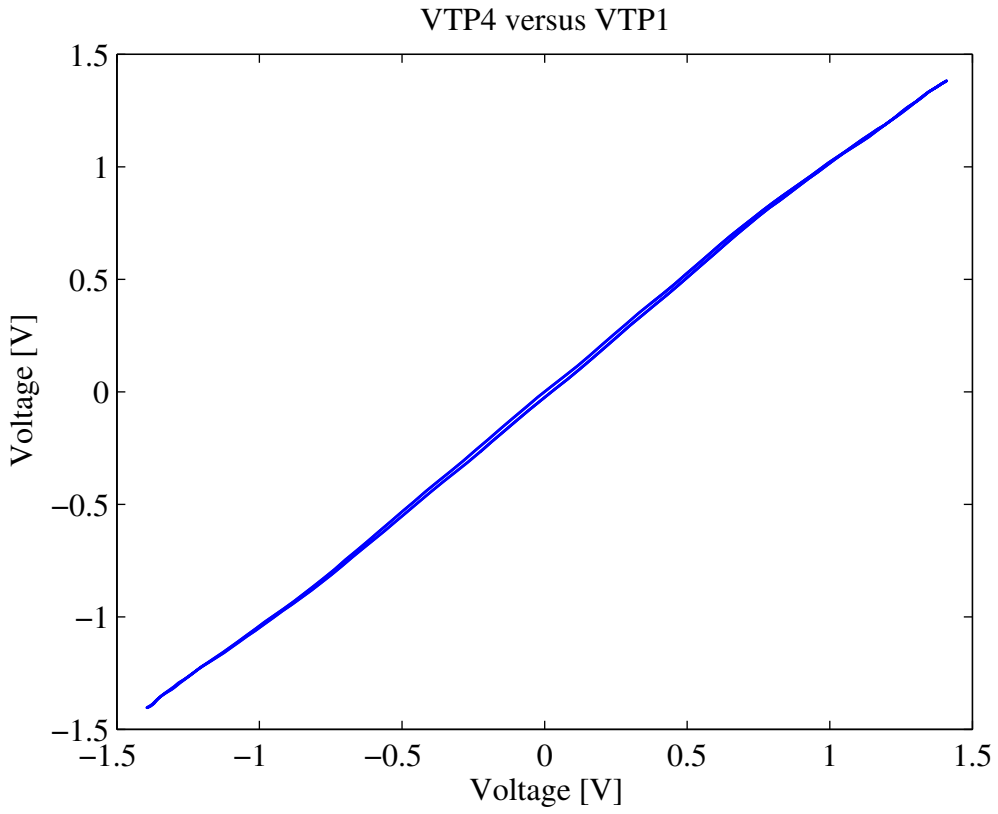


Figure 4.2. Plot of VTP4 versus VTP1 from Oscilloscope Data

Notice that the plot is nearly closed, indicating a very small phase shift through the operational amplifier. It is also important to note that the slope of this graph describes the gain between the two points. There is no change in the gain because, for this experiment, the threshold voltage is set above the amplitude of the input signal, so no limiting occurs.

4.3 Closed-Loop i/v Characteristics

Though the closed-loop i/v characteristic cannot be measured directly, a measurement of the closed-loop gain is an acceptable substitute. For this measurement, the bias voltage is set to 0.5 V, which corresponds to a threshold voltage of 0.79 V. Figure 4.3 shows a plot of VTP4 versus VTP1. The plot is generated using oscilloscope probe data, and then a piecewise-linear curve is fit to the plot using a MATLAB tool called SLMtools.

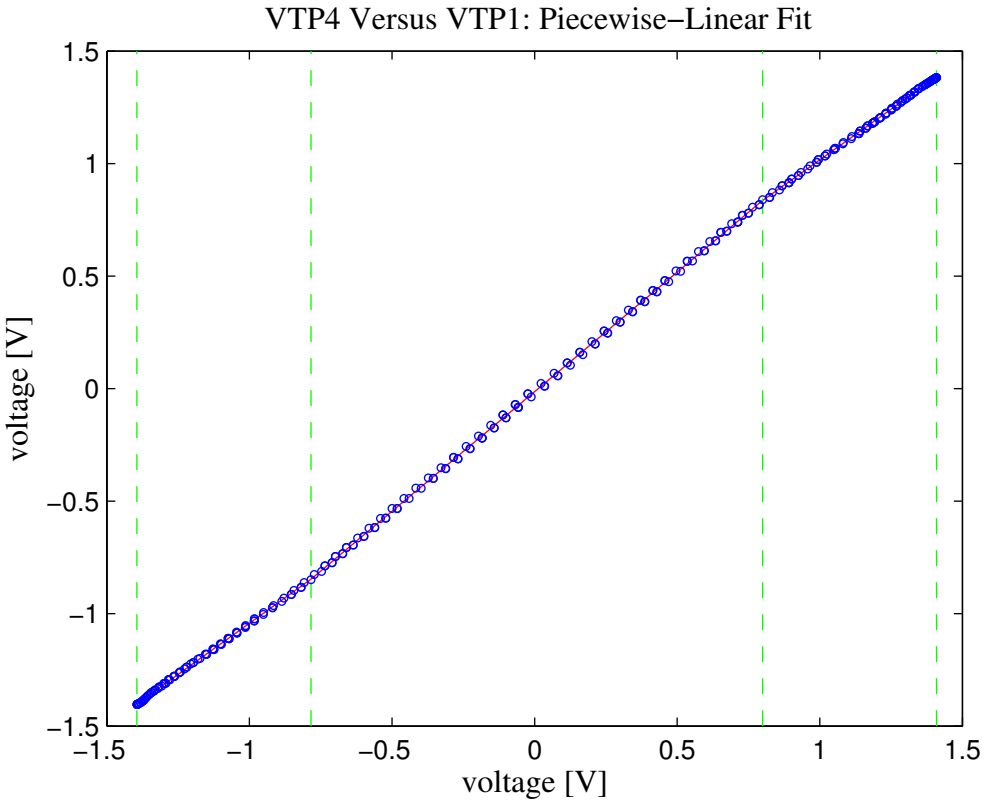


Figure 4.3. Plot of VTP4 versus VTP1 with Jumper JP2 Closed

SLMtools is a curve fitting tool which uses shape language modeling (SLM) to create a

least squares spline fit. SLMtools differs from other least squares curve fitting tools in that it utilizes the user's knowledge of the system being modeled to make more accurate fits. For this experiment, the user is able to command SLMtools to generate a piecewise-linear plot with two "knots," which are the points at which the slope changes. From the curves created by SLMtools, it is possible to determine the slope of the data in Figure 4.3.

Two slopes are obtained. The inner slope, m_i, represents the estimated slope for absolute values of VTP1 less than the threshold voltage. The outer slope, m_o represents the estimated slope for absolute values of VTP1 greater than the threshold voltage.

The data in Figure 4.3 corresponds to the v/v characteristic of the voltage-dependent voltage source $\bar{G}(v)$ shown in Figure 2.5. From equation 2.5, it follows that

$$\hat{g}_A = \frac{m_i - 1}{R_5 + R_6} \tag{4.1}$$

and

$$\hat{g}_B = \frac{m_o - 1}{R_5 + R_6}, \tag{4.2}$$

where $\hat{g}_A$ and $\hat{g}_B$ are the estimated values of g_A and g_B, and $R_5 + R_6$ is the resistance of the feedback resistor. The estimated values $\hat{g}_A$ and $\hat{g}_B$, along with the values of g_A and g_B predicted by the measured resistance values are shown in table 4.3.

Parameter	Predicted Value μS	Estimated Value μS	Percent Error %
g_A	19.796	20.508	3.47
g_B	14.361	16.862	14.8

Table 4.1. Comparison of Predicted i/v Parameters to Experimentally Measured Parameters

4.4 Discussion

Experimental results indicate that the NRC designed in this thesis satisfies all of the design requirements. It exhibits an open-loop positive gain which, when the loop is closed, results in a negative conductance at the NRC's input. The phase shift between the input voltage and the voltage at the output of the operational amplifier is nearly zero. This means that, when incorporated into a marginal oscillator design, the circuit's conversion gain will be able to be evaluated using Viswanathan's analysis. Though a direct method for the measurement of the circuit's i/v

characteristic is not possible, comparison of the operational amplifier's output voltage with its input voltage in closed-loop operation is sufficient to determine the NRC's parameters. When compared to the values predicted by the circuit's analysis, the measured values are sufficiently close to justify incorporating the NRC into a marginal oscillator.

Chapter 5

Summary and Future Work

5.1 Summary

This thesis makes two contributions to the understanding of negative resistance converters. First, it assesses several earlier FET NRC designs, as well as one operational amplifier NRC design, against the i/v characteristic studied by Viswanathan. Next, it analyzes, designs, and synthesizes a functional NRC.

This thesis examines the work of three other authors. The first, Lee and Choh, implemented an NRC as part of a marginal oscillator using FETs. Though Lee and Choh were able to achieve oscillation, their circuit required significant tuning. Simulation results indicate that Lee and Choh did not understand what their NRC's i/v characteristic was or how the potentiometers in their circuit affected its shape.

The second author, Viswanathan, implemented an NRC in a marginal oscillator using FETs as well. She also understood what the shape of the NRC i/v characteristic should be to sustain oscillation, and indeed the simulated i/v characteristic in this study closely resembles her model. However, Viswanathan lacked the tools necessary to experimentally obtain the i/v characteristic for her low- and high-frequency NRCs. Simulation results indicate that both circuits exhibit i/v characteristics that are similar, but not identical, to the shape of her predicted characteristic.

The final author whose work is examine herein is Chua. Chua implemented an NRC for an autonomous chaotic circuit by utilizing the nonlinear regions of operational amplifiers' i/v characteristics. Unfortunately, Chua's NRC is not useful for use in high frequency circuits like

marginal oscillators.

The design in this study is similar to the design by Chua. There are, however, several major differences. First, the design in this study was redesigned for approximately independent adjustment of g_A, g_B, and v_T. Second, the our NRC design utilizes High Gain Bandwidth operational amplifiers that simply did not exist at the time of Chua's design. Lastly, Chua capitalized on the nonlinear characteristics of the operational amplifiers themselves to create a piecewise-linear i/v characteristic, while this design utilized Schottky diodes to implement the nonlinearity.

Finally, an NRC was synthesized that exhibits the i/v characteristic studied by Viswanathan so that the quadrapole resonance lab at Penn State could test the theory for the prediction of conversion gain experimentally. Earlier marginal oscillator designs did not realize NRCs with the i/v characteristics analyzed by Viswanathan. This does not mean that they were not marginal oscillators, but rather that we do not have, as yet, an analytical prediction of the conversion gain.

5.2 Future Work

The NRC designed in this study is useful for determining the effects of a single negative, nonlinear i/v characteristic on the conversion gain of a marginal oscillator. However, future work is needed to improve the analytical prediction and experimental verification of the NRC's effects on the marginal oscillator's conversion gain.

In high-frequency, low-voltage applications, the effects of thermal noise present in resistors must be considered. As such, one future project will be to compute the contribution of thermal noise from the NRC to the marginal oscillator. An understanding of the thermal noise contribution from the NRC will facilitate prediction of the noise present in a marginal oscillator.

The NRC i/v characteristic implemented in this thesis was used because it lent itself well to the theoretical computation of conversion gain. However, there may be another i/v characteristic that optimizes the conversion gain of the marginal oscillator. To allow future researchers to explore these other i/v characteristics experimentally, the analog NRC circuit designed in this study should be implemented digitally. One such implementation is to use a look-up table to implement the i/v function with an A/D and D/A converter on the input and output respectively.

Similarly, a digital implementation makes it prudent to investigate the effects of quantization in time and amplitude on the functionality of the NRC.

Bibliography

[1] T.L. Viswanathan, T.R. Viswanathan, K.V. Sane, "Study of Marginal Oscillator Behavior", *IEEE Transactions on Instrumentation and Measurement*, vol. IM24, no. 1, pp. 55-61, 1975

[2] A. Roberts, "Two New Methods for Detecting Nuclear Radio Frequency Absorption" *The Review of Scientific Instruments*, vol. 18, no. 11, pp. 845-848, 1947

[3] B.V. Rollins, "Nuclear Paramagnetism", *Reports on Progress in Physics*, vol. 12, no. 1, pp. 22-23, 1949

[4] R.T. McIver, "A Solid-State Marginal Oscillator for Pulsed Ion Cyclotron Resonance Spectroscopy", *The Review of Scientific Instruments*, vol. 44, no. 8, pp. 1071-1074, 1973

[5] G.L. Miller, M. Soni, R.L. Fenstermacher, "A Technique for Investigating the Properties of Surfaces, Thin Films, and Interfaces by Means of a Mechanical Marginal Oscillator", *Journal of Applied Physics*, vol. 53, no. 2, pp. 979-983, 1982

[6] D. Alexiev, M.I. Reinhard, L. Mo, A. Rosenfeld, "A Transient Conductance Technique for Characterization of Deep-Level Defects in Highly Irradiated Detector-Grade Silicon", *Nuclear Instruments and Methods in Physics Research Section A*, vol. 434, no. 1, pp. 103-113, 1999

[7] A. Gauzzi, J. Le Cochec, G. Lamura, B.J. Jönsson, V.A. Gasparov, F.R. Ladan, B. Plaçais, P.A. Probst, J. Bok, "Very High Resolution Measurement of the Penetration Depth of Superconductors by a Novel Single-Coil Inductance Technique", *The Review of Scientific Instruments*, vol. 71, no. 5, pp. 2147-2153, 2000

[8] Leon O. Chua, "The Genesis of Chua's Circuit", *AEÜ*, vol. 46, no. 4, pp. 250-257, 1992

[9] Takashi Matsumoto, "Eventually Passive Nonlinear Networks", *IEEE Transactions on Circuits and Systems*, vol. CAS-24, no. 5, pp. 261-269, 1977

[10] Jongmin Lee, Sung Ho Choh, "Robinson-Type Nuclear Quadrupole Resonance Spectrometer Adapted to Field-Effect Transistors", *The Review of Scientific Instruments*, vol. 53, no. 2, pp. 232-235, 1982

[11] Thomas Tyson, Jeffrey Schiano, "Development of Undergraduate Laboratory Modules in Continuous-Wave Quadrupole Resonance Spectroscopy", *NSF EE REU PENN STATE Annual Research Journal*, vol. IV, 2006

[12] T. Lakshmi Viswanathan, "Design of a Nuclear Quadrupole Resonance Spectrometer", PhD Thesis, Indian Institute of Technology, Kanpur, 1970

[13] Michael Peter Kennedy, "Robust Op Amp Realization of Chua's Circuit", *Frequenz*, vol. 46, no. 3-4, pp. 66-80, 1992

Vita

Brandon Tricou

Address: 202 W. Fairmount Ave.
State College, PA 16801

Email: brandon.tricou@gmail.com

Education:

Schreyer Honors College
The Pennsylvania State University, University Park, PA
B. S. in Electrical Engineering, May 2011

Work Experience:

May 2009 - May 2010
Student Co-op
Videon Central, State College, PA
- Aided in the testing and development of several in-flight video products
- Constructed cables for use in engineering design and quality testing
- Compiled component failure rates to predict product Mean-Time-Before-Failure

May 2008 - August 2008
Student Intern
Applied Research Laboratories, The Pennsylvania State University
- Developed an algorithm for underwater mine countermeasures
- Learned about genetic algorithms and other advanced decicion-making processes

June 2010 – May 2011
Private Tutor
PSUKnowHow, State College, PA
- Communicated information in both one-on-one and group settings

Service:

August 2007 – February 2011
Penn State Dance Marathon (THON)
- Procured food donations for several events as a Hospitality Captain
- Raised money through solicitation and fundraising

August 2008 & August 2009
Schreyer Honors Orientation Mentor
- Helped incoming freshmen scholars become acclimated to college life