THE PENNSYLVANIA STATE UNIVERSITY
SCHREYER HONORS COLLEGE

DEPARTMENT OF ELECTRICAL ENGINEERING

LONG TERM ELECTRICAL STABILITY TESTING OF ZINC OXIDE THIN FILM TRANSISTORS

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Abstract

The electrical stability of semiconductor devices over long periods of time is an important attribute in determining the usefulness of devices or new semiconductors compared to conventional devices and silicon, the industry standard semiconductor. Zinc oxide is a relatively new semiconductor material for which the long term stability of the material and devices is currently unknown. In this work, the electrical stability of zinc oxide thin film transistors was measured through electrical stress testing. The temperature sensing properties of a zinc oxide transistor array were also measured.

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Acknowledgments

I would like to thank Dr. Jackson for his help and patience which were crucial in my studies. I would like to thank all of the graduate students in the Center for Thin Film Devices especially: Devin Mourey, Dalong Zhao, Yuanyuan Li, and Israel Ramirez who patiently worked with me and provided samples to test.

I would also like to thank Dr. John Mitchell for helping me throughout my Schreyer career and for the insightful help he has provided to guide my thesis.

Chapter 1: Introduction

1.1 Importance of Long Term Electrical Stability

The long term electrical stability of a semiconductor device is a primary concern because it will affect the reliability of any applications structures created. Semiconductor devices must be electrically stable and have high reliability, maintaining performance characteristics over the expected useful life of the device. For example, if an unstable device powered an LED, it might become noticeably dimmer or brighter over an unacceptably short period of time.

1.2 Why Zinc Oxide?

The most common semiconductor used in manufacturing today is silicon. Silicon is an exceptional single crystal semiconductor, however, there exist applications where it is not feasible or cost effective to use single crystal silicon, and so amorphous silicon is used instead. Applications that use amorphous silicon however, open opportunities for other semiconductor materials, such as zinc-oxide (ZnO), which may provide superior performance and lower temperature processing. The much lower processing temperature for ZnO is a large advantage when working with flexible substrates.

There are many properties that set zinc oxide apart from silicon. ZnO is an II-VI oxide semiconductor that forms a lattice with two elements instead of only one. ZnO forms a hexagonal wurtzite crystal lattice structure with parameters of a = 0.3296 nm and c = 0.52065 nm [1] instead of a diamond lattice with parameters a = 0.54307 nm [2]. The crystal lattice can be visualized as tetrahedrally coordinated O^{2}- and Zn^{2}+ ions in alternating planes stacked along the c-axis [1]. The crystal lattice of ZnO gives it strong piezoelectric and pyroelectric properties. ZnO has a direct bandgap of 3.4 eV compared to the indirect bandgap of 1.1 eV for silicon [1]. ZnO is also a transparent film for visible light, which combined with the wide direct bandgap makes it well suited for photovoltaic

applications. Compared to amorphous silicon, ZnO has high electron mobility at room temperature, reportedly as high as 205 cm^2/ V-s [1], compared to only 1 cm^2/ V-s for amorphous silicon [2]. ZnO is naturally n-type due to defects in the film, however the exact defect or combination of defects that this arises from is currently disputed. [1] These properties, in addition to the low material cost of ZnO and the ability to easily form a high quality film, allow ZnO to excel.

1.3 Zinc Oxide Thin Film Transistors

Zinc-oxide is typically deposited as a film on top of another substance that acts as a substrate instead of being manufactured in a wafer format like silicon. The films of zinc oxide used in these experiments were deposited using Plasma Enhanced Atomic Layer Deposition (PEALD). The thin film transistor (TFT) design used for these experiments is "bottom gate staggered", where the gate is below the active layer and the source and drain contacts are above the active layer. The bottom gate structure for ZnO TFT's is preferred in the tested devices due to the more mature processing techniques and the isolation of the ZnO from the substrate. The bottom gate structure design can take advantage of the wide bandgap of ZnO to form self aligned source and drain contacts to reduce the capacitance of the device [3].

There are many methods of depositing a film of zinc oxide onto a substrate. Common substrates for ZnO are glass, ITO, silicon wafers, Kapton, PET and PEN [4]. Atomic layer deposition (ALD) is a self limiting process of depositing ZnO one atomic layer at a time onto the substrate. This process is done by bringing a metal-organic species into the reactor, diethylzinc (DEZ) in this work, aided by a carrier gas such as argon [5]. The metal-organic impinges on the surface until it saturates, after this the excess metal-organic is removed by purging and an oxidant is introduced which reacts with the metal organic, forming a monolayer. This process provides a uniform film at a relatively low temperature. However, this process is slow due to the need to purge the chamber between every cycle; this is needed to prevent the metal organic and the reactant from

interacting in a non-controlled manner [5].

The film of zinc oxide for the samples measured in this experiment was deposited using plasma enhanced atomic layer deposition (PEALD). PEALD has many advantages over the more typical ALD deposition technique. In PEALD a weak reactant is used (typically CO_2 or N_2O) so there is minimal interaction with the metal organic (typically diethyl zinc) so that the weak reactant can be used as the purge gas (Figure 1), simplifying the system to only needing two gases instead of three [5]. The use of a weak reactant as the purge gas allows for a constant flow to be set, which results in a faster cycle time. The semiconductor film is formed when the plasma activates the weak reactant making it behave as a strong reactant. An RF plasma (13.56 MHz) is pulsed to provide the energy needed to activate the weak reactant [1]. One disadvantage in using PEALD comes from the small amount of ion bombardment caused by the plasma.

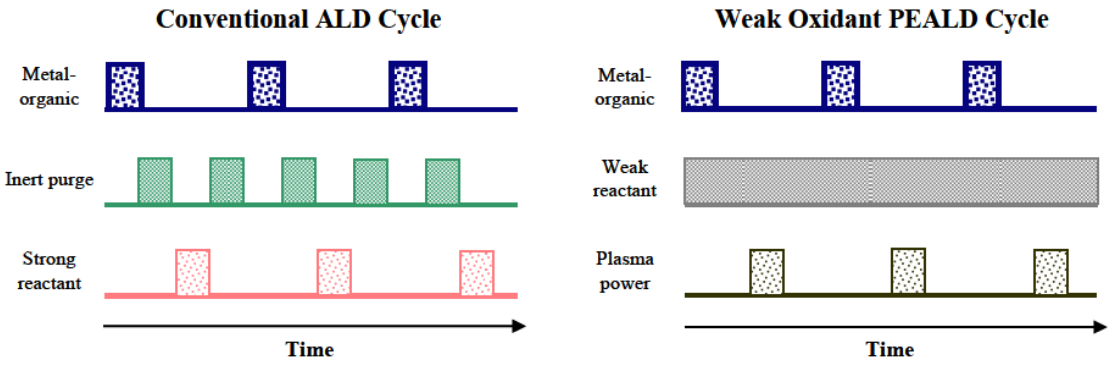

Figure 1 - ALD vs. PEALD cycle for three cycles [1]

1.4 Bias Testing

One method of stability testing has all the terminals of the device set to constant voltages, with the device biased in the active region, and measures the output current as time passes. This method of testing determines how the device performance changes over time. Much of the short term data about the behavior of a charge in the device gate and oxide can also be obtained from this test. This information can also be gathered from capacitance-voltage (C-V) measurements.

Bias testing is a method of measuring how the charge in the device structure changes while the device is under stress. Bias testing results provide a picture of the aggregate effect of mobile charges in the device, fixed charges in the oxide, mobile charges in the oxide, and accumulation of charges in the oxide [6]. Fixed charges in the oxide are generally caused by interface traps between the oxide and the semiconductor. The fixed charge generally stays constant in a device unless sufficient heating occurs to modify the interface states [2]. Mobile charges are typically caused by minute contamination during fabrication. The device can be contaminated with metals or other materials that have a high diffusivity in the oxide or semiconductor when processed. The accumulation of charges in the oxide occurs from charge injection into the oxide. Differentiating between these various effects can be done by tracking the different time scales through which these effects operate [6].

1.5 Sweep Testing

Another method of stability testing a transistor is to set the source and drain to a constant value and perform multiple sweeps of the gate voltage while measuring the current over time. The actual performance of the device across the intended voltage range is measured and information on unwanted charges in the oxide and semiconductor is obtained. The differential mobility can also be obtained from the sweep of a device if information about the dimensions of the device structure is known [7].

One of the methods of modeling thin film devices is by tracking changes in the device's threshold voltage between sweeps. Repeated measurements of the device output over time allows for the fitting of the measured data to threshold-voltage shift models [8].

Sweep data also allows for a quantification of the charges measured in the bias testing by comparing the location of the device threshold voltage and the shape of the current-voltage (I-V) curve [6].

Chapter 2: Measurement System Setup

2.1 Purpose of a Long Term Measurement System

A measurement system was created to perform automated testing of thin film transistors for long periods of time. Long term testing can be used to determine the electrical stability of semiconductor devices. Prototype systems have been measuring devices since the summer of 2010 (Figure 2Figure 2). A more complete measurement system was implemented in the fall of 2010. Since then the measurement system hardware has remain unchanged while software utilization of the hardware has become more sophisticated.

The prototype setup only had the measurement capabilities to record data from voltage sweeps, so tests were composed of repeated sweeps everytime a datapoint was desired. The second version of the setup was able to record datapoints during the bias time without using a sweep. The third version implemented limited climate control through the addition of a heat source and a primitive isolation box. The final test setup included the ability to define the DIP connections of the tested sample in the software.

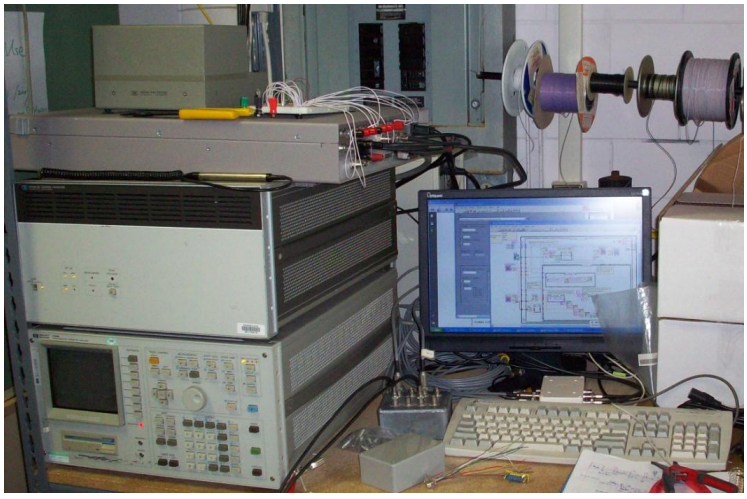

Figure 2 - Prototype System

2.2 Hardware Setup

The measurement system is composed of several interconnected instruments. A computer controls the system and receives the data over the IEEE-488 interface bus. The system can be divided into three segments: a measurement unit, a switching unit and the wire-bonded sample to be tested Figure 3.

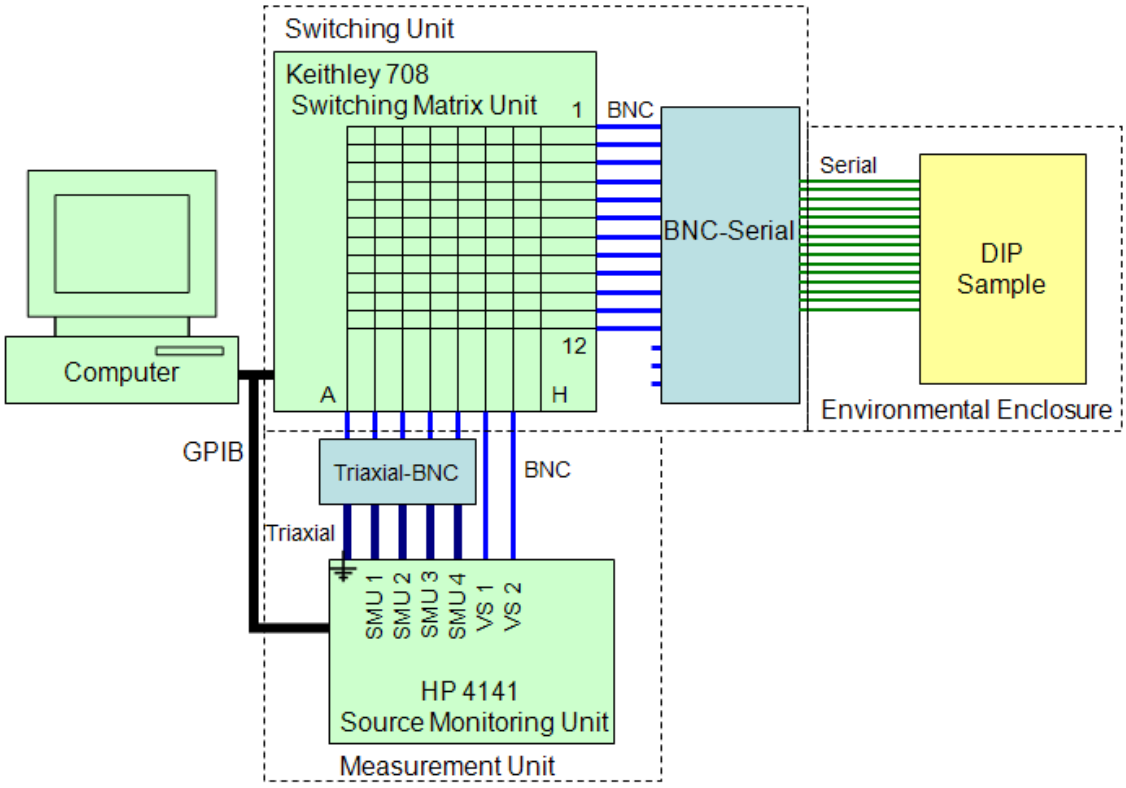

Figure 3 – Long Term Testing Hardware Layout

The measurement instrument was the HP 4141 which provided a combination of accuracy & speed of measurements for a reasonable cost. The HP 4141 has four programmable Source Monitoring Units (SMUs) that can accurately measure currents down to the pico-amp range, two programmable voltage sources and a ground monitoring unit (GMU). The limited number of SMUs leads to the limitation of only being able to excite one gate line and measure three drain lines at once. The SMUs and the GMU of the HP4141 had triaxial connector outputs which were converted into BNC compatible

outputs for system compatibility [9]. This came at the cost of reducing accuracy to the tenth of a nano-amp range. The key feature for integrating the system is the IEEE-488 programmability of the HP 4141 (also known as the general purpose information bus (GPIB) link). This is a significant benefit that allows the instrument to be remotely controlled through LabView.

The switching instrument for the setup was the Keithley 708A switching matrix with a 7075 BNC switching card. The Keithley 707 card has an 8 by 12 switching matrix that interfaces with two banks of BNC connectors. The bank of 8 BNCs are labeled alphabetically and connected to the measurement instruments while the bank of 12 BNCs is labeled numerically and connected to the samples. The switching matrix allows for connecting multiple samples to the test setup while using different test connection configurations. With this setup it is possible to do in-place substitution with a Keithley 707 switching matrix. The Keithley 707 contains slots for up to six additional switching cards that can create up to an 8 by 72 switching matrix. The Keithley switching matrix is also programmable over IEEE-488 [10].

The samples tested were wire-bonded into 16 pin DIP packages for ease of measurement as well as to ensure a reliable connection. The package is then placed in a DIP socket that is connected to the Keithley switching matrix.

2.3 Software Setup

The software controlling the system is a LabView program that contains two levels of abstraction. The top level that the user interfaces collects the parameters needed for the run and passes it to the lower level program, displaying the measurement results from the lower level. The lower level of abstraction takes the user inputs and sends the system appropriate commands to perform the measurements.

The user-level abstraction layer program is called DiscreteAnalysis and is explored in detail in appendix A.2 Discrete Analysis v3. This program consists of two sections: the first section takes the user inputs from the graphical interface and controls whether

previous measurements will be reviewed or new measurements will be taken. The second section of the program takes the measurements from a file and processes the data translating the information into graphs of measured current and voltage.

The instrument-level abstraction layer program is called DiscreteMeasure and is explored in detail in appendix A.3 Discrete Measure v2. This layer consists of several major sections. The first section takes parameters for the measurement and initializes arrays of commands that will be used in other sections. The second section initializes the instruments by sending commands over the IEEE-488 interface preparing the instruments for measurement. The third section performs the sweep measurement on all the devices. The section after this performs a bias test on all the devices. The last section generates a list of all the files generated in the measurement after all the sweeps and bias measurements have been taken.

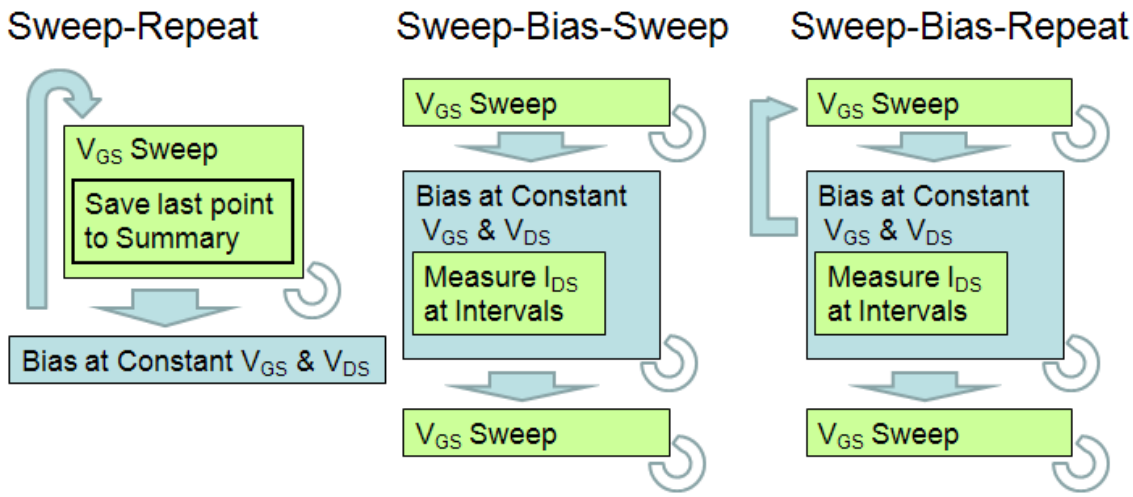

Figure 4 - Measurement Algorithms

Three different measurement algorithms have been developed for the instrument level LabView program. These algorithms are called: “sweep-repeat”, “sweep-bias-sweep”, and “sweep-bias-repeat” (Figure 4). This program communicates commands and listens for results from the instruments over IEEE-488.

The sweep-repeat was an early algorithm that only measured sweep data. In this algorithm, each transistor in the array would be swept and the last data point of the sweep

would be stored as the summary over time. Between sweeps, the devices were biased but no data was measured. This method can also be seen as the "sweep-bias-repeat" method with the bias time to zero and number of measurements taken during the bias period to 1.

The sweep-bias-sweep method was the next algorithm developed. A sweep of every device is performed, then all the devices are biased and then the sweep is repeated on all the devices. This method can also be seen as the "sweep-bias-repeat" method with the number of bias intervals set to one. This method can be useful because in some cases gate sweeps provide a restorative effect on the device output that obscures the long term device trends.

The sweep-bias-repeat method is the final measurement algorithm developed. The gate line is swept while measuring the drain current and it then repeats on the remaining gate line voltage for all the devices in the array. A constant voltage is supplied to the gate while measurements are made at intervals during the bias time - this is then repeated for all devices in the array. This cycle is repeated as many times as the user desires. The length of the bias interval used was typically an hour. This method tests the performance of the device and provides information on the threshold voltage of the device over time.

2.4 Device Fabrication

The Zinc Oxide TFTs used in this experiment were discrete transistor devices. The majority of samples were fabricated and provided by Dalong Zhao in November 2010 on a glass substrate.

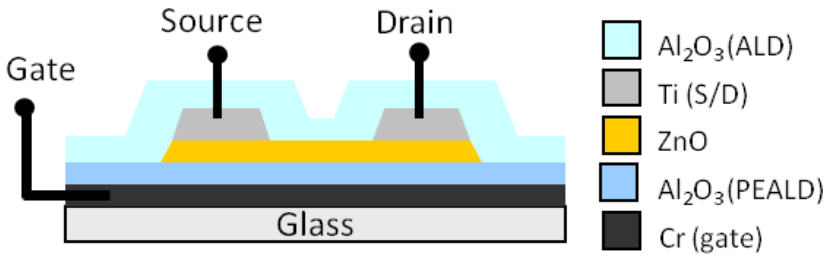

Figure 5 - Schematics for passivated bottom gate staggered-inverted structure for ZnO TFTs [1]

The fabrication process for bottom gate devices on a glass substrate uses the following steps: first is the deposition of the bottom gate metal, chrome, which is uniformly deposited to a thickness of approximately 100 nm. The gate metal is then patterned to form the gate line and the gate contact. Next, the aluminum oxide insulator is deposited with the PEALD system to provide the gate oxide. After that step the zinc oxide semiconductor is deposited in-situ by PEALD system. This prevents contamination and damage of the semiconductor/gate oxide interface. The zinc oxide and aluminum oxide layers are patterned through simple lithography. A double lithography is performed to create contact locations. Titanium or aluminum is deposited to form the contacts and the excess metal is removed by lift off. At this point a thin passivation layer of aluminum oxide is deposited to protect the device from environmental contamination and interactions while waiting for further testing [1]. For a more in-depth description of the fabrication process, see Appendix C: Device Fabrication Steps.

2.5 Device Test Preparation

The devices must be packaged in order to be connected to the test seat which connects the sample to the measurement system. This is accomplished by dicing samples into small sections using a glass scribe. PMMA is placed on top to protect the surface of the samples while in storage. The PMMA is later removed with a rinse of acetone, followed by a rinse of IPA and DI water, which is then followed by air drying.

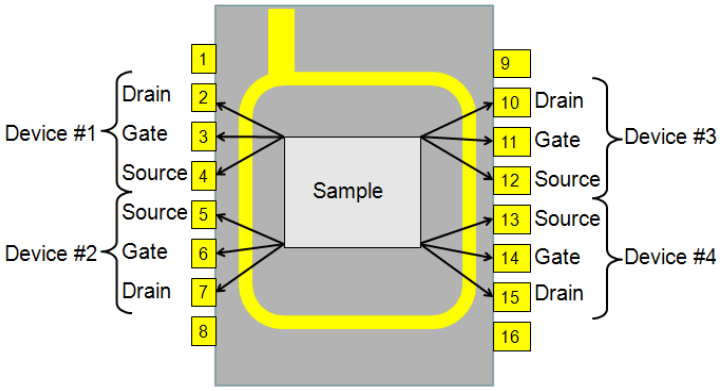

Figure 6 - Standard DIP Layout

The samples are then bonded to the dual in-line pin (DIP) package with an adhesive to secure the sample and prevent movement while the devices are wire bonded to the terminals. The pin out configuration seen in

was chosen to provide open pins for future device bonding on the sample and to provide an easy way to hold the package without damaging the transistors with static discharge. Shorting the open pins and measuring across them provides information on the system noise.

Chapter 3: Device Results

3.1 Device Characteristics

The results of numerous testing runs provide for a glimpse into the performance of zinc oxide transistors. Device characteristics of a typical zinc oxide TFT shows the output current generally decreases as the length of time in the "on" state increases. Typical characteristics for the device output are a current between 10 µA and 200 µA for a drain voltage of 0.5 V and an 8 V gate voltage (Figure 7). These devices typically have a turn-on voltage of -2V for a drain voltage of 0.5 V (Figure 8).

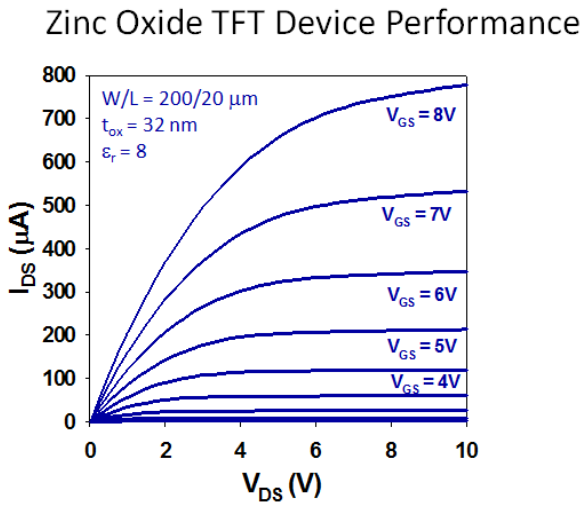

Figure 7 - Typical ZnO TFT Performance V_{DS} vs. I_{DS} curves [7]

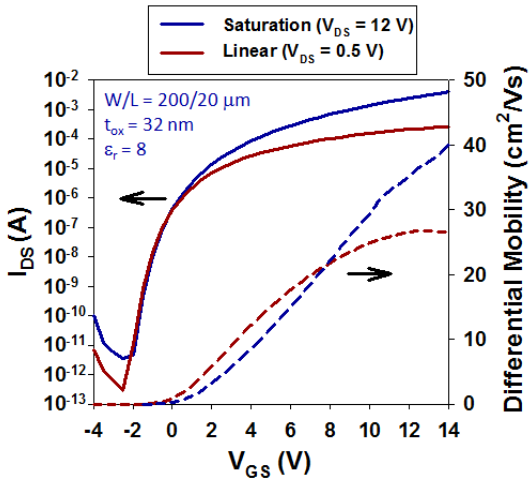

Figure 8 - Typical JERG Device Performance V_{GS} vs. I_{DS} curve and Differential Mobility [7]

The initial experiments used the "sweep-repeat" method and only recorded the sweep measurements, tracking the last point of the sweep over time. These included experiments #1 to #4, with the results shown in Figure 9. Experiments #1 & 2, sample #1 device #2 was measured with a 2V V_{DD} and a V_{GS} range of -10 V to 10 V and the current slowly decreased. Experiments #3 & 4, sample #2 device #1 was measured with a 0.5V V_{DD} and a V_{GS} range of -4 V to 8 V and the current gradually increased over time. The gradual increase in current in this sample may be an indication that sweeping the gate of the device regenerates the device output. However experiments #1-4 are the only experiments made with rapid succession sweeps and minimal bias times.

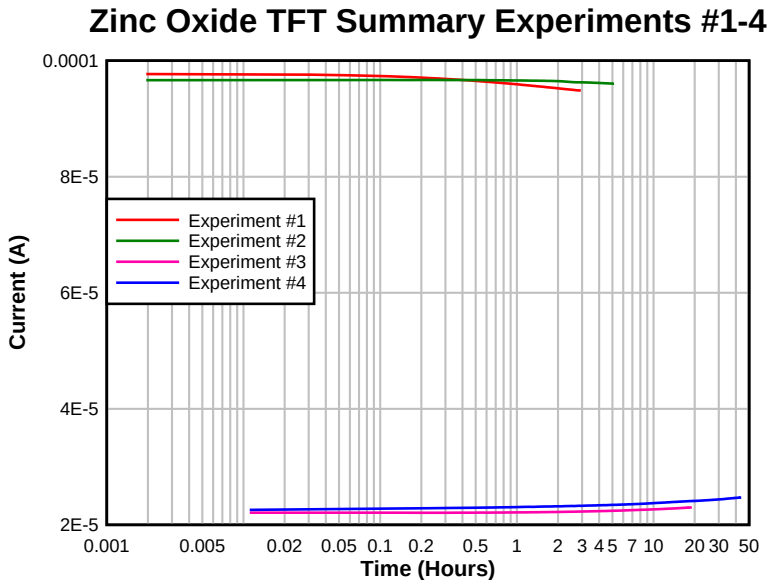

Figure 9 - Summary Experiments #1-4

The next batch of experiments used the "sweep-bias-sweep" method and was limited to a sweep at the beginning and at the end of the experiment with a 0.5V V_{DD} and a V_{GS} range of -4 V to 8 V. These experiments include experiments #5-7 and the outcome can be seen below in Figure 10, showing the results of sample #3 device #1, sample #3 device #4 and sample #4 device #4 respectively. Experiments #5 & 6 have a much lower current output expected, so it is likely they are not fully functional. Experiment #7 shows that the device slowly turned off and then turned back on after a half an hour of testing, likely due to a loose bond the lost connection and then wavered back.

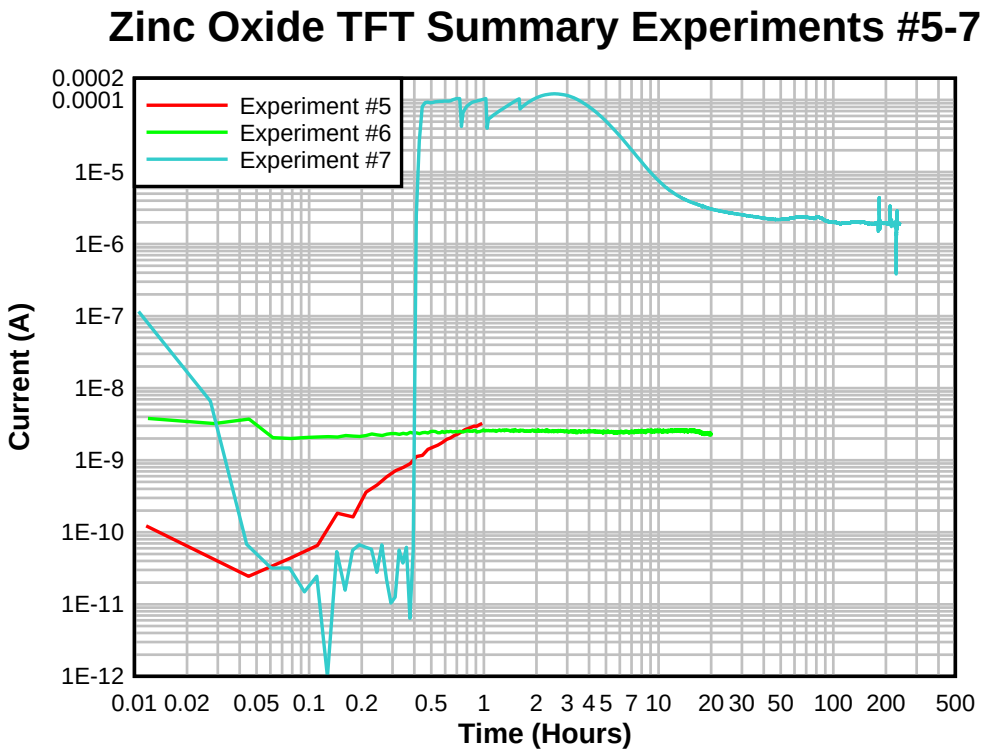

Figure 10 - Summary of Experiments #5-7

The last set of experiments performed sweeps at regular user-defined intervals (typically every hour) while measuring the bias current. This set of experiments includes #8 through #25. The addition of additional sweeps allowed finding the shift of the curves as time elapsed. From this information the majority of the shift was seen toward the beginning of the measurement, and the amount of the shift was seen rapidly decreasing. Typically 95% of the shift was made within the first twelve hours.

An aggregation of measurements from experiments #10-16 (Figure 11) consistently shows the same trend in the drain current over time. Here the absolute current measurement is shown on the left and the percent change from the initial value measured is shown on the right. The data for this figure is measured from sample #7, device #3.

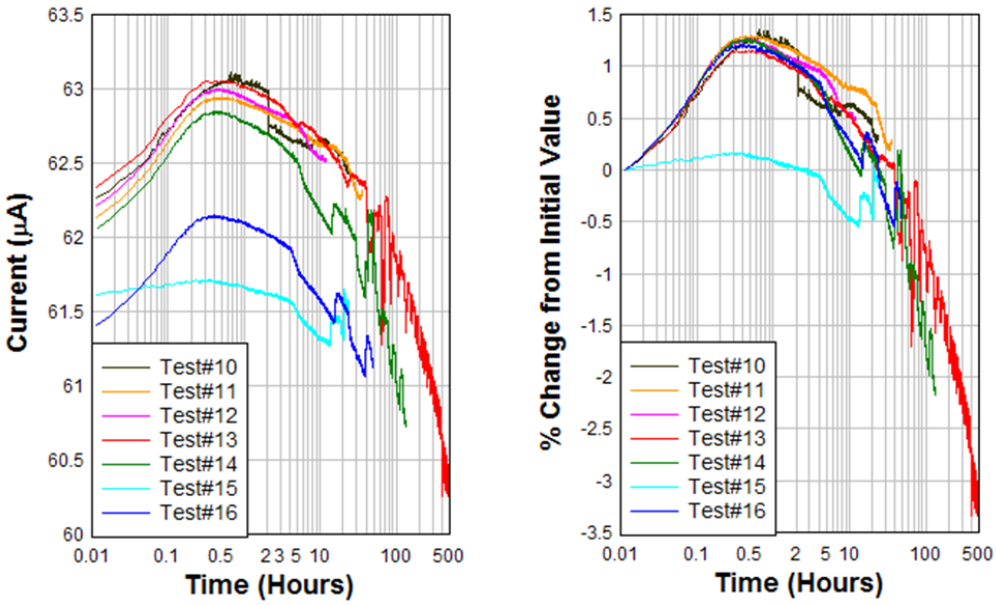

Figure 11 - Aggregate summary of Bias measurement results in a) Absolute current and b) Relative to the initial measurement value

Experiment #13 was the tested over the longest period of time, and thus provided the most interesting set of measurements. The experiment started at 5pm on Friday, December 10th and continued until December 30th. The parameters of this experiment are a 0.5V V_{DD} and a V_{GS} range of -4 V to 8 V for the sweep performed every hour and 0.5V V_{DD} and a V_{GS} of 8 V for the bias period. In this experiment, there is a rise in current for the first 30 minutes resulting in approximately a 3% increase in current. This was followed by a drop off in current that ends with the current output approaching 3.5% lower than the initial value. One additional thing to note about this experiment (that is most easily seen in Figure 12) is the periodic bumps to the output current. These bumps match the ambient temperature of the lab and predate the addition of a warming plate to ensure a constant temperature. The bumps clearly follow the diurnal temperature cycle of the lab during winter, with a sharp rise when the heat for the lab was turned on followed by the slow overnight cooling of the room.

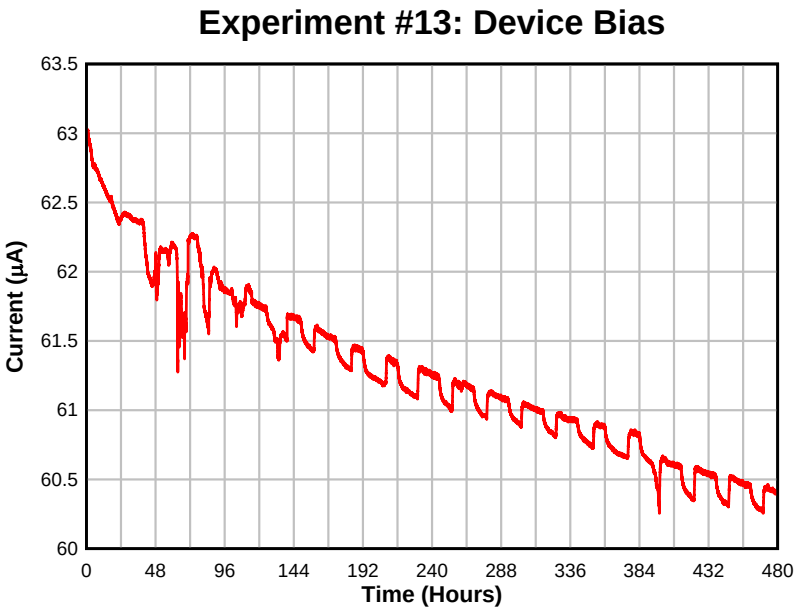

Figure 12 - Long Term Test Results of Experiment #13

3.2 Analysis of Device Characteristics

The devices measured in these experiments performed similar to transistors fabricated and measured by the group prior to this experiment. The similar performance between the devices measured suggests a high uniformity and reproducibility to the production process. The long term testing has suggested that the drain current fall-off rate decreases as time passes. Fitting the results to a model will allow us to see analysis of the performance of the devices [8]

One of the more interesting attributes observed in the device measured was a slight increase in current for the first half-hour measured. This was then followed by the more commonly reported drop off in current. The increase in current seen initially is likely to be a confluence of several effects. The gradual roll off of current is a commonly reported thin film characteristic which also shows up in amorphous silicon devices [11] [12]. As can be seen in Figure 13, the initial current increase is related to the drain voltage, where larger drain voltages result in a lower hump in output current. The mechanism behind this is possibly a very slow mobile charge effect; however it is not known positively, but

appears to be directly related to the drain-source voltage difference [13].

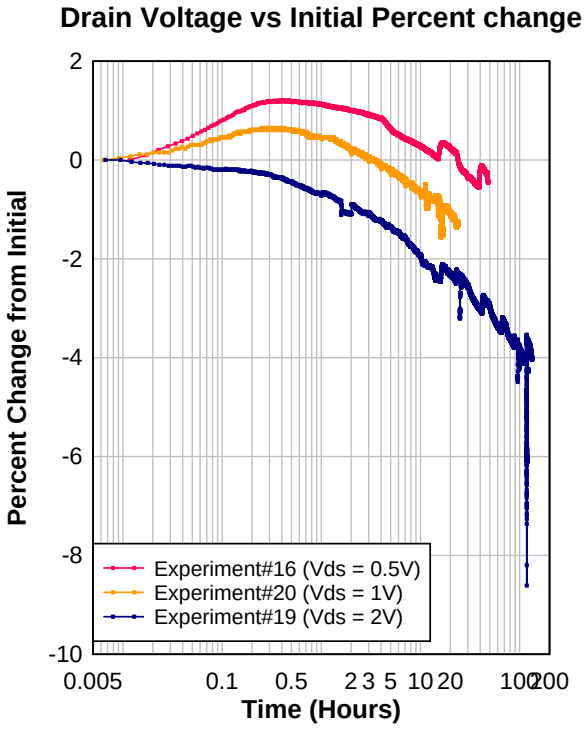

Figure 13 - Drain Voltage vs. Initial Percent Change

The results from experiment #13 were fitted to a curve extrapolating the device performance to a longer amount of time (Figure 14). The curve shows that the decline in drain current output is gradual reduced, resulting in a device performance loss maximum of approximately 3.7 % of the initial current. The theoretical maximum loss is expected to be approached only after 60 days of constant testing. This drop in performance is typically believed to be due to a degradation of the device channel region or charge injection into the oxide from the channel [12].

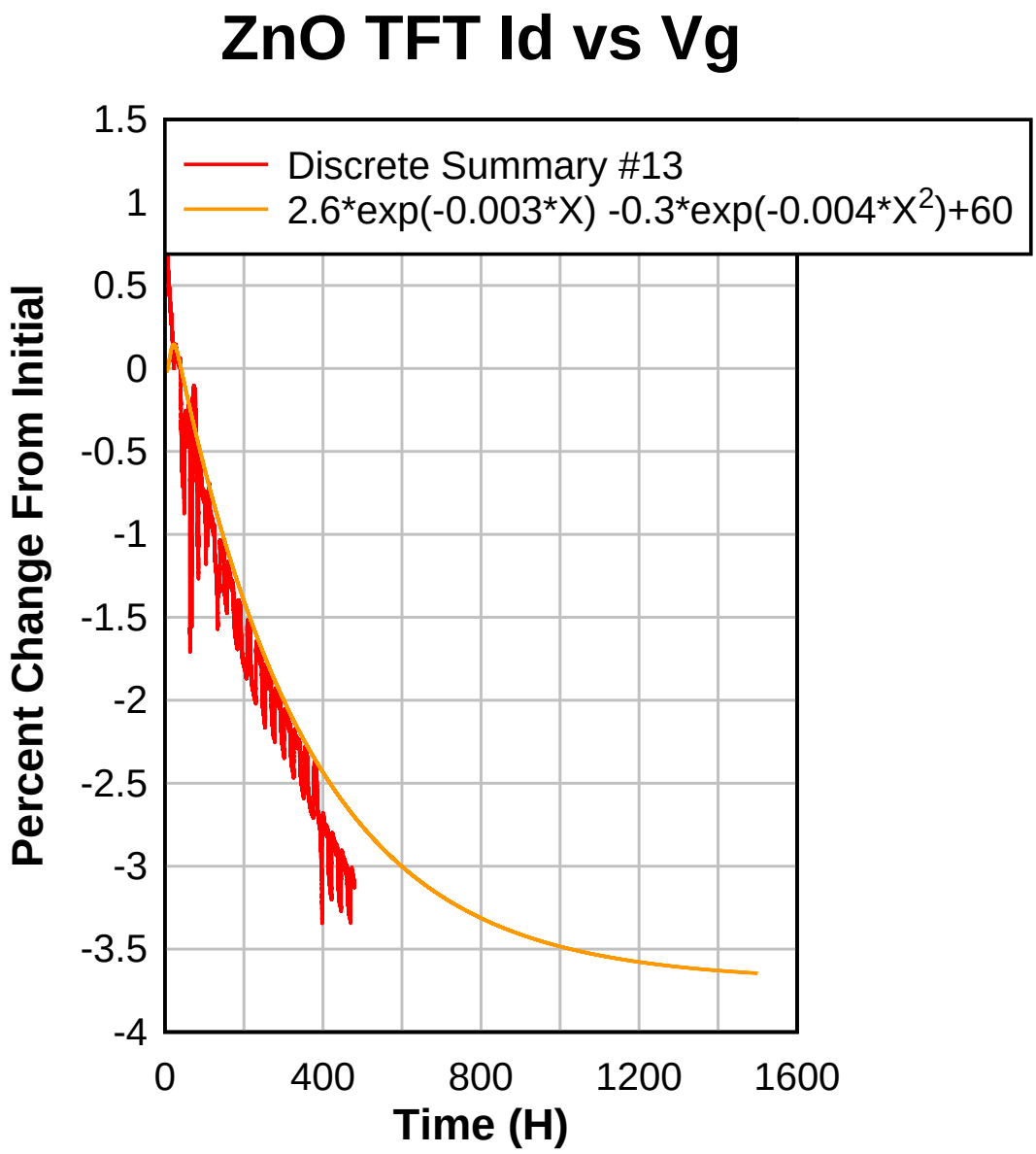

Figure 14 - Percent change from the initial value for Experiment #13 and an exponential fit that extrapolates the change towards the future.

Chapter 4: Temperature Sensor Array

Zinc Oxide was shown to be temperature sensitive in experiment #13 which makes it naturally suited for thermal measurements [1]. To observe this effect, two different array structures were designed by Dalong Zhao: a differential output array and a single ended ouput array. The design of these structures have several aspects in common: three pins for providing ground, a drain voltage and a current bias; and gate lines that provide voltage to the entire column of devices (Figure 15). The single ended devices have one TFT at each node, while the differential array has two TFTs at each node with different current biases caused by different W/L ratios of the current mirror.

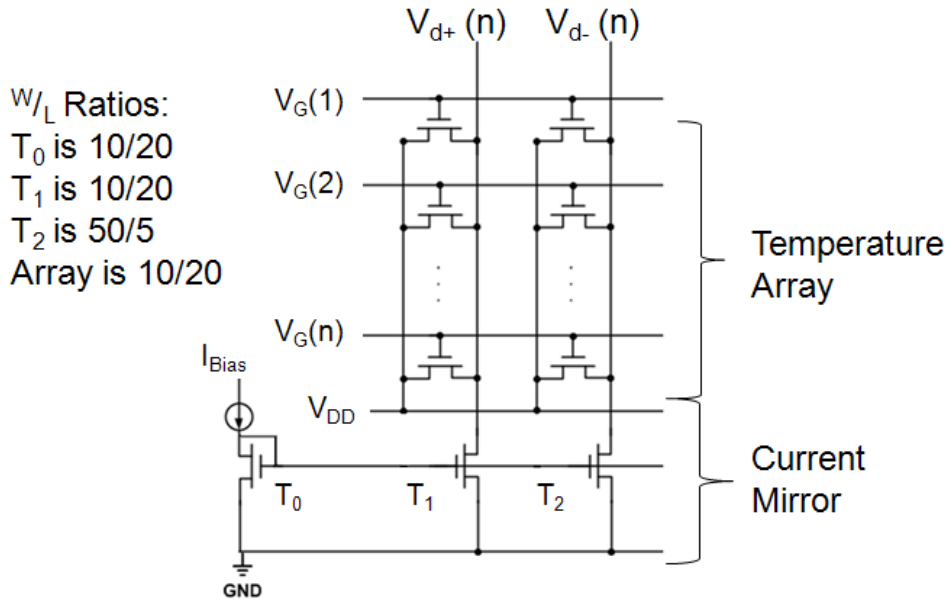

Figure 15 - Differential Thermal Array Circuit Diagram

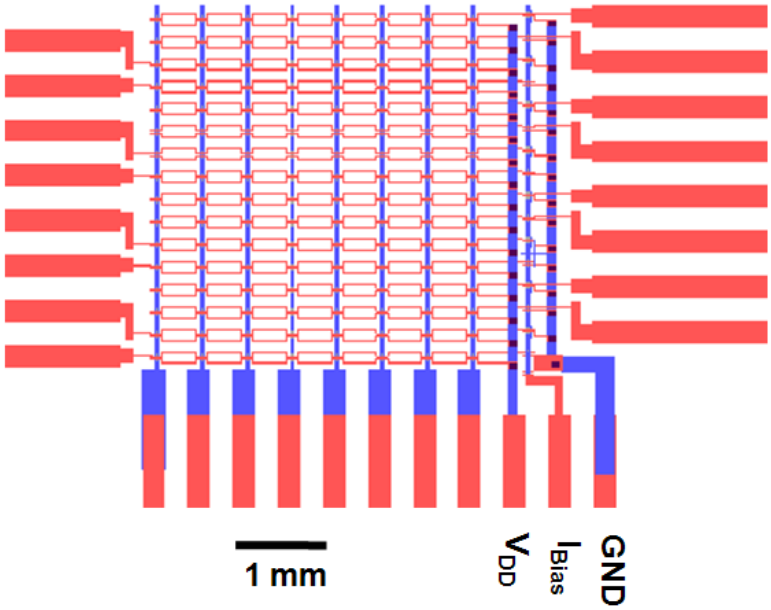

Figure 16 - Layout Schematic for 8x8 Differential Output Thermal Sensor Array

4.1 Temperature Measurement Hardware Setup

The thermal sensor array measurement system is composed of a computer that runs a LabView program (to control the rest of the setup), a NI 6229 Data Acquisition Card and a custom interface board (Figure 17). The NI 6229 was chosen for its ability to simultaneously handle 32 analog inputs and provide over 32 digital outputs. The custom interface board converts the digital outputs of the NI 6229 describing the state of the gates into the "on" and "off" gate voltages that are used in the experiment. The samples are bonded using anisotropic conductive film (ACF) to 25-pin blue ribbon flexible ribbon cables with a 500 µm pitch connected to the drain and gate lines (Figure 16). The blue ribbon cables then plug into the NextGen board (a custom interface board) that connects to the NI 6229 (Figure 18) [14].

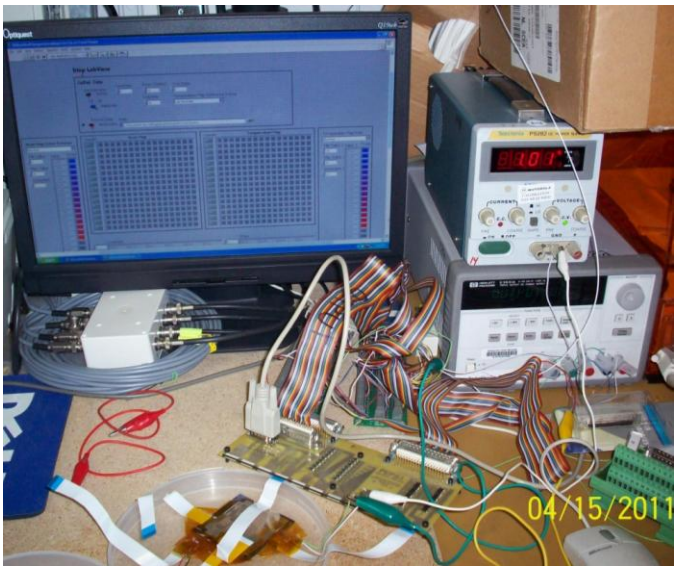

Figure 17 -Temperature Measurement System

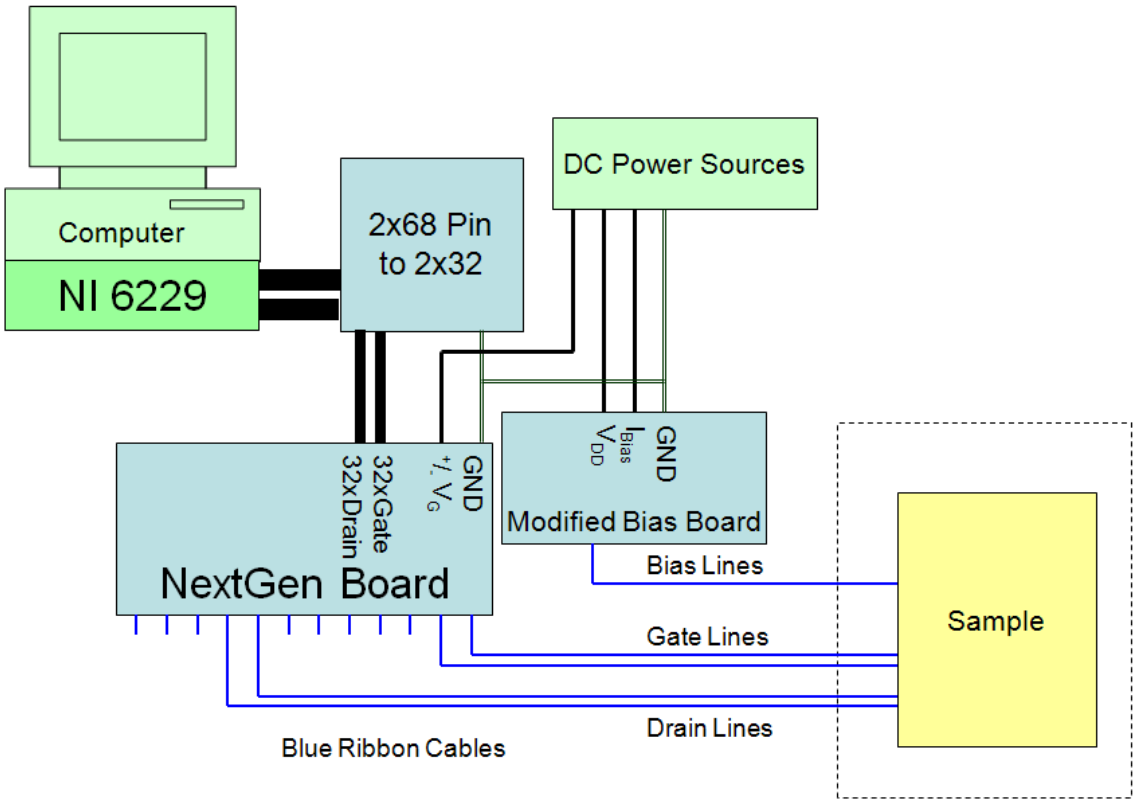

Figure 18 - Block Diagram of Thermal Sensor Array Measurement System

4.2 Temperature Measurement Software

The measurement software used is SEThermalTemperatureMap(16x16); the custom LabView program is included in Appendix B: Temperature . The setup is only able to read from one row of the array at a time. To handle the multiple rows in the sample, the program sets one gate line to 'ON' and the other lines to 'OFF'. This allows for data to be read from the one 'ON' row. Multiple readings are rapidly taken by the NI 6229 DAQ, and the readings are averaged to provide a final measurement for a row. If the sample is defined as a differential sample, pairs of lines are subtracted from each other to create the differential signal measurement. If the sample is defined as single-ended, then the measurements are left alone. In the next step, the software maps the values measured to a user defined color scale to provide a scan map of the array. The measured values are also compared to reference data and mapped to another user defined color scale that shows the difference between the reference and the measured data as the temperature map of the system. The software then repeats this step until all the defined rows are measured. The reference frame can be defined as either the last complete sweep, the last recorded sweep or a previously recorded sweep. Data is recorded in comma separated value (.cvs) format to preserve formatting of the array of data.

4.3 Results from the Temperature Sensors

The temperature sensor array did not have a large amount of samples tested due to the relatively late design and fabrication. To collect more extensive data from fewer devices, many runs were repeated on the same device. These devices were fabricated by Dalong Zhao and Yuanyuan Li.

From the results of the thermal sensor array the temperature sensing properties are seen. Figure 19 (below) shows the temperature sensor array when the array is only exposed to the ambient environment and no additional stimuli. The speed which the array could be measured and visual data updated was limited to the speed in which the hardware could update the display with the results. Measurement of discrete devices showed rapid (<1s)

response to temperature stimuli.

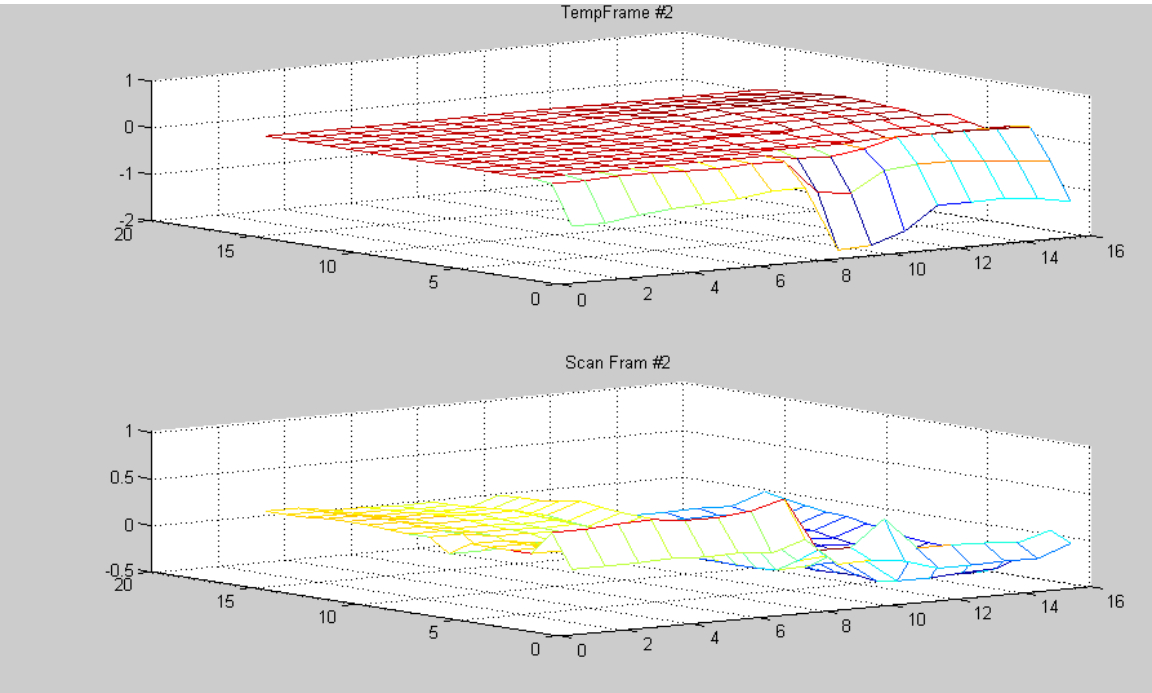

Figure 19 - Ambient temperature sensor measurement

A heat gun was used to raise the temperature of the sample to between 70ºC and 90ºC which resulted in a large change in voltage visible across the entire sample array. A drastic change compared to the measurement with no heating can be seen in Figure 20. The thermal sensitivity of the temperature can be calculated by dividing the temperature increase (57ºC) by the average voltage increase (3.1 V) resulting in approximately 18.4ºC per volt or 54.4 mV per ºC.

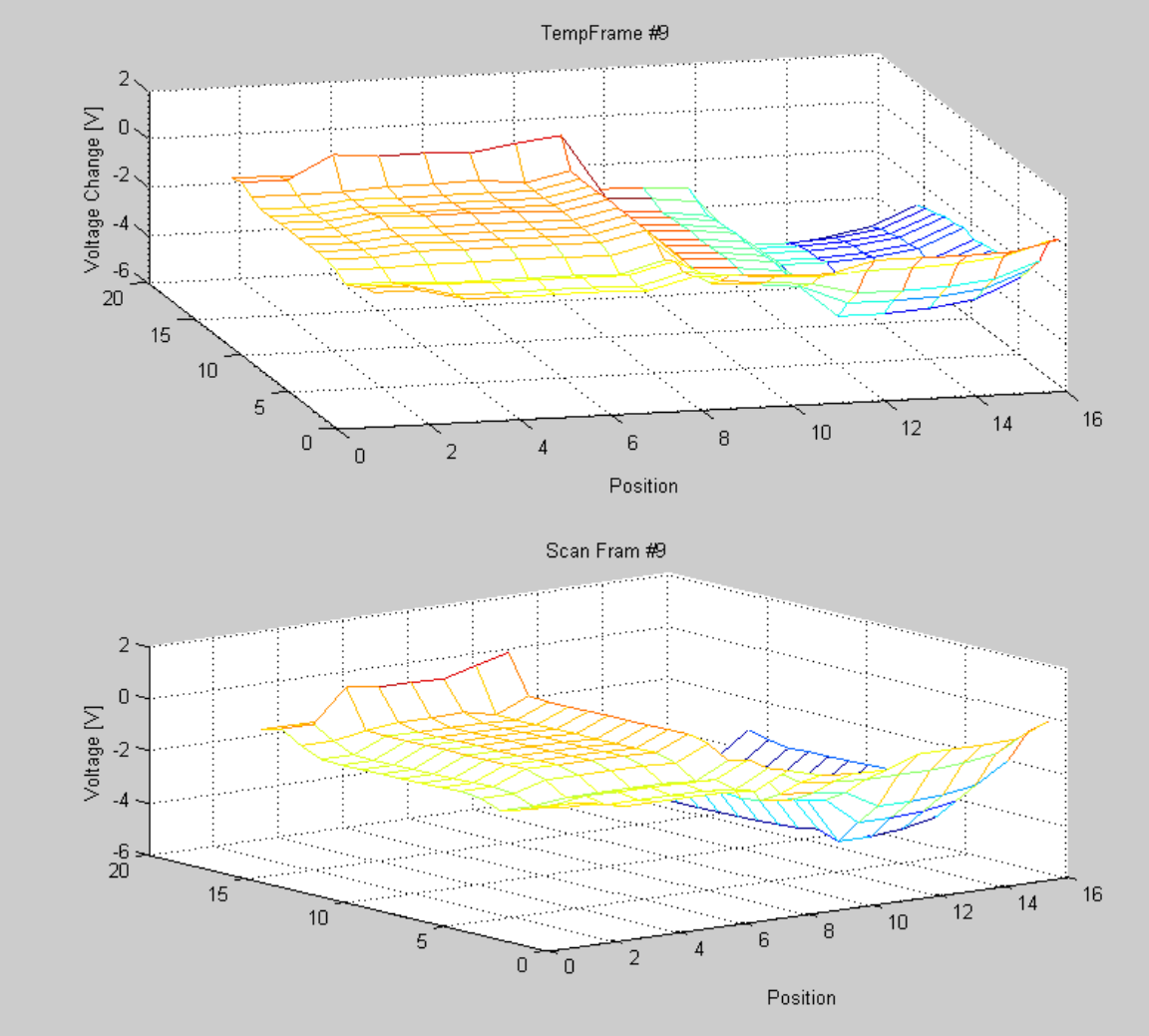

Figure 20 - Temperature sensor array after heat gun

A red laser (5 mW, 650 nm) was used to raise the temperature of the sample in localized regions. This resulted in a moderate change in voltage visible in the localized portion of the sample array. Figure 21 shows a spike in voltage on the temperature map due to the laser being pointed at the right half of the array. This test shows the ability of the thermal sensor array to have a reasonable spatial resolution to the temperature response.

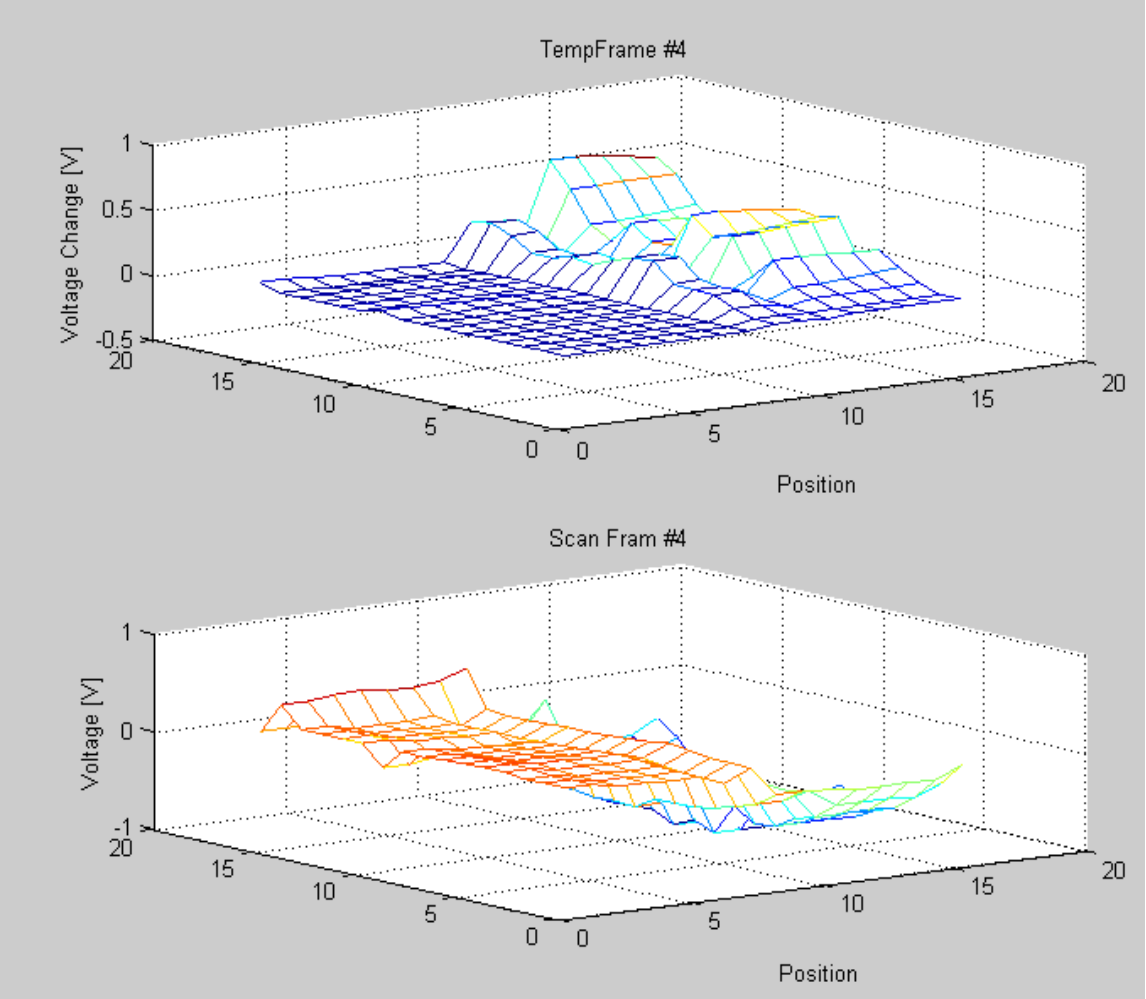

Figure 21 - Temperature sensor array with the red laser

Chapter 5: Conclusions & Further Steps

The device testing capabilities of the Center for Thin Film Devices were improved by the addition of a long term testing suite and a thermal array testing suite. From the long term measurement platforms it was shown that that zinc oxide is a viable semiconductor material for applications requiring circuits to be active for long periods of time.

The long term testing suite revealed several aspects of the zinc oxide TFTs. A small hump in steady state current output centered on a half hour of constant biasing was found, that has not been previously reported. Over long periods of time (hundreds of hours) the current drive of zinc oxide TFT's was shown to only drop only a few percent from the initial output current.

Zinc oxide was also shown to be significant and useable as a temperature sensor. The device sensors were shown to be responsive enough to distinguish localized heating caused by a laser as well as general heating from a heat gun.

There are several further steps that can be taken in the future to increase confidence in the results in both the long term stability testing and the temperature sensor array. These steps include increasing the sample size, scaling the measurement system and increasing control of environmental conditions.

5.1 More Samples

Increasing the number of samples measured would provide a higher confidence in establishing the value for the electrical stability of zinc oxide thin film transistors. Currently results are based upon the testing of 10 different devices. Increasing the number of samples tested will increase the statistical significance of the measurements made and demonstrates the reproducibility of the results. Increasing the number of samples tested also reduces process variation noise from the general device performance model. One of the limiting factors in the sample size for both test systems is the ability to reliably bond large numbers of devices in short amounts of time. Wire-bonding relies on

the sample being diced to the appropriate size, which limits the number of the devices that can be measured from a single wafer. Anisotropic conductive film bonding has not been reliable in this work and requires several consecutive bonds on the same connection to ensure all the lines are connected.

There were several limiting factors in the quantity of working devices to test for the long term stability test. One step that reduced the number of samples was due to how the samples were separated. In order to separate the samples on the glass substrate a scribe was used to score the glass and pressure was applied to snap the glass. This process of scoring and snapping has the potential to damage the TFT's if any scratching occurred. Another limiting factor on sample size was due to accidental damage to devices. These devices have no protection from static discharge and the lifespan of devices handled often was significantly reduced. In the handling of the DIP packages, it is easy to build up enough charge to destroy the device without noticing that a fatal discharge occurred.

The main limiting factor in the quantity of samples for the thermal array was the quantity of samples produced. The decision to test thermal sensor arrays was made too late for a large number of thermal arrays to be produced.

5.2 Scaling of Measurement System

Increasing the number of samples placed through long term testing will result in a large time investment before obtaining all the necessary results. The testing setups for both the thermal sensor array and the long term stability test can both be scaled to measure an increased number of samples in a reduced time span. This can be accomplished through one of two different methods: creating parallel testing setups or through the testing of a larger array of samples.

Additional testing setups scale the number of samples that can be tested simultaneously in a linear fashion. Separate test setups allow for independent measurement of multiple groups of devices under different conditions. The primary disadvantage of this method of scaling is the additional equipment needed. The cost of scaling using this method is

directly related to the cost of obtaining additional equipment and the associated space required to fit the test setup. The primary advantage of this however is that all the old equipment can still be useful and an incremental increase in capacity is only an incrementally larger cost. The long term stability measurement system sees the most benefit from increasing the number of setups because it benefits the most from an increase in parallel measurements.

Increasing the size of the array greatly increases the number of devices that can be tested. The benefit of increasing the testing with array setups is that more devices can be measured for less hardware. The disadvantages are that there are limits to the number of simultaneous devices that can be measured; however there are time savings in being able to automate changing between devices. A shortcoming to array testing is that all devices must be under the same bias and measurement regime. The main disadvantage of array testing is an incremental increase in capacity is will require replacement of all the equipment. The temperature measurement array benefits the most from an increase in the number of devices in the array because this will increase the spatial resolution of the device.

The most cost effective way to increase sample measurement throughput is a combination of these two methods to maximize the increase in automation and an increase in simultaneous measurements.

5.3 Environmental Conditions

There are other conditions that can affect the electrical stability of a semiconductor and the sensitivity of the measurement system which are the operating temperatures, the presence of light and the ambient humidity.

Temperature affects semiconductor operation by affecting the carrier concentration, mobility, or interface charge. The long term stability system needs to minimize changes in the ambient temperature around the device that can lead to changes in the operation of the device, especially devices with known strong thermal effects like ZnO. Without

appropriate environmental control it is difficult to ensure that device output changes are due to changes in performance and not a change in the ambient temperature [2].

Samples tested in the presence of light can also result in changes to the results. The light can be absorbed by exposed semiconductor material and result in a higher carrier concentration than the test conditions would otherwise indicate. An increase in carrier concentration might cause the device to function better on high frequency characterization or behave normally at higher frequencies and would lead to poor estimations of mobility and the threshold voltage [6]. The temperature sensor array needs to have a consistent light environment, so changes in performance can be assumed to be from changes in the temperature and not due to the photoelectric effect [1].

Humidity can slightly affect the test setup. Changes in humidity create the biggest impact in the manufacturing steps where the chemistry of the device creation can be greatly affected. The test setup is primarily affected by slight changes in capacitance as the humidity minutely changes the capacitance of some of the connections. Humidity can also affect the amount of moisture contaminating the sample if the sample has not been passivated [5].

5.4 Additional Test Conditions

The test conditions used so far do not exhaustively cover the range of conditions that can be used on the devices. The long term stability measurements have a range of additional conditions to be tested. One expansion of the tests done would be to include a wider range of values for the drain voltages to see the effect on the hump that appears centered at half an hour. Another set of test parameters that could be changed would be varying the length of the bias interval and gate voltage ranges. This would check if ZnO has any regenerative effect as a result of the sweeps. An additional test that needs be performed, but was not due to time limitations, is having at least one test run for 60 to 70 days. This will be a direct test of the analysis drawn in Chapter 3.2 Analysis of Device Characteristics.

The temperature sensor array measurements also have a large range of additional test conditions that could be used. Over the course of the measurements, the gate voltage for these measurements was a constant +5V for the on state and -5V for the off state, and it should be checked if increasing the voltage of the on state would increase the response of the sample. Another set of conditions to test would be to modify the V_{DD} value applied to see if the sample became more or less responsive to changes in temperature.

5.5 Conclusion

In conclusion is can be found that zinc oxide is a viable semiconductor material for applications requiring circuits to be active for long periods of time and as a temperature sensing material. The long term testing suite has revealed a small hump in steady state current output centered on a half hour of constant and that the drive current of zinc oxide TFT's was shown to only drop only a few percent from the initial output current. The temperature measurement system has shown zinc oxide TFTs can be used as temperature sensors that can be responsive enough to distinguish localized heating caused by a laser as well as general heating from a heat gun.

Appendix A: Long Term Measurement System

This section describes the temperature measurement system in more detail. Section A.1 Long Term Measurement System User Manual describes the setup and use of the system. Sections A.2, A.3, A.4 and A.5 go into depth about the LabView program code used to control the sweep and bias measurements is depicted here.

A.1 Long Term Measurement System User Manual

The section will describe the proper method to setup and use the long term measurement system.

A.1.1 Long Term Measurement System Setup

1. Gather the materials
   - Computer with IEEE-488 Port
   - HP 4141 Source monitoring unit
   - Keithley 708 Switching Matrix
   - 2 IEEE-488 Cables
   - 19 BNC Cables
   - 5 Triaxial Cables
   - 15 BNC to Serial Converter Box
   - Triaxial to BNC Converter Box (Isolated Connections)
   - Serial Compatible Test seat
2. Connect the computer, HP 4141 and Keithley 708 IEEE-488 Ports
   - Remember the IEEE-488 Addresses of the HP4141 & 708 for later
3. Connect all the HP 4141 SMUs and GNDU to the Triaxial-BNC converter box
   - The outer sheath of the HP4141 Triaxial is Hot, so triaxial connections on the box must be isolated
4. Connect the converted BNC connection of HP 4141 SMU's & the two VS to the

Lettered bank of the 708

- GND connects to A, SMU1 to B…VS1 to F, VS2 to G

5. Connect the 12 numbered bank of the 708 to the corresponding port of the BNC-Serial converter box
    - It is recommended to connect GND to pin 15 of the BNC-Serial Box
6. Plug in serial compatible test seat to the BNC-Serial box

A.1.2 How to use the Long Term Measurement System

1. Insert DIP package into test seat
2. Connect source pins the DIP package to serial Pin 15
3. Turn on Computer, HP 4141 and Keithley 708
4. Load DiscreteAnalysis.vi
5. Enter & save the IEEE-488 address of the HP4141 & Keithley 708
6. Select the file path to save files
7. Set the switch to “measure” measure a new device or “read” to review old measurements.
8. Select “Array” or “Discrete” (Array measures N x M array while Discrete measures N devices)
9. Enter the Drain Pin and Gate Pin numbers
10. Enter the Bias Parameters
11. Enter the Sweep Parameters
12. Press “Run” to start the LabView program
13. Once the experiment is done, cycle through the desired devices and press OK to bring up the graphs
14. For additional measurements press “Run Again”

A.2 Discrete Analysis v3

DiscreteAnalysis is the user level program that receives user inputs and displays the measurements back to the user. The program is designed to be save measurements to file as the program progresses. This allows the program to be interrupted and a new run made with different parameters and still retain the old data. The formatting of the save files also makes it easy to patch files together so that multiple runs can seen as one large run.

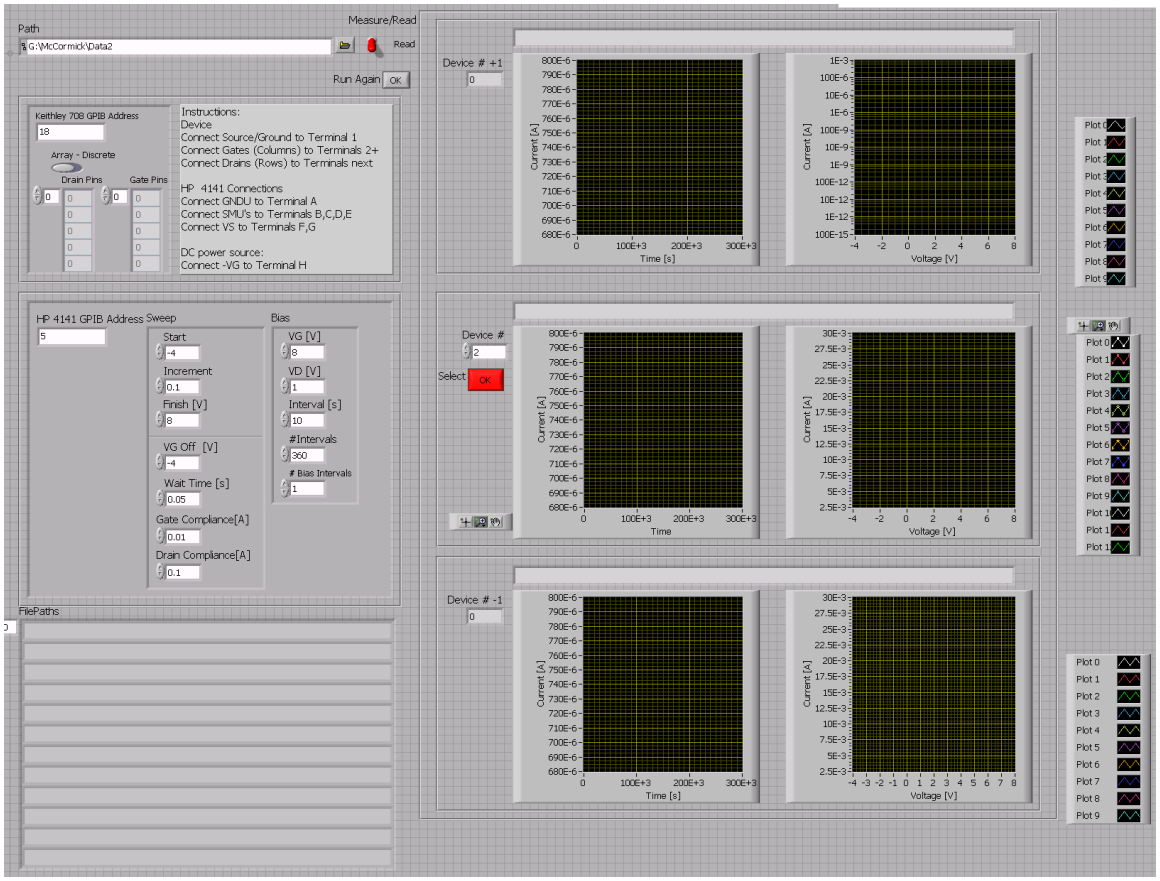

Figure 22 - Front Panel of Discrete Analysis Program

The user inputs are on the left and the graphs on the right show the device measurements. The ability to change which of the devices are displayed is in the center and the new device choice can be displayed at the touch of a button. Device measurements are only displayed after all measurements have been taken.

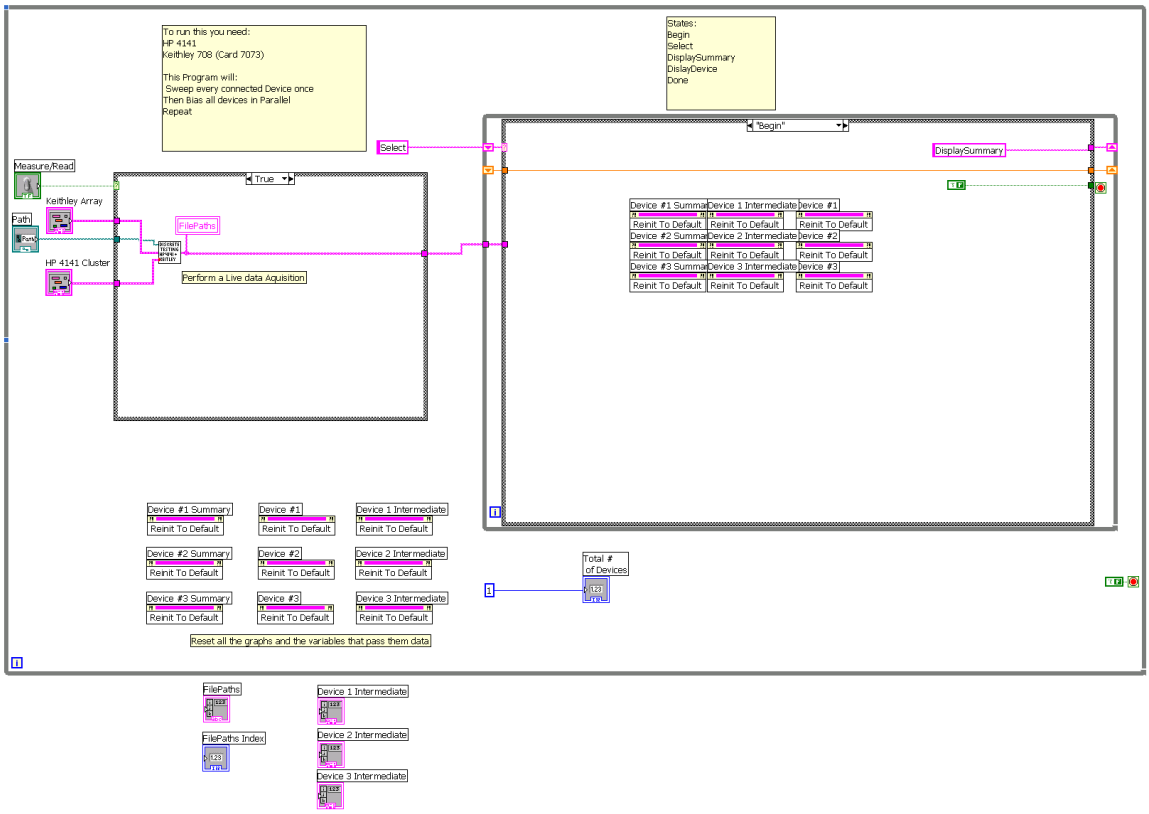

Figure 23 - Discrete Analysis Block Diagram

The left side of the program generates the file names of all measurements. The right side of the program is where the relevant files are selected, read and outputted to the main interface through the use of a state machine.

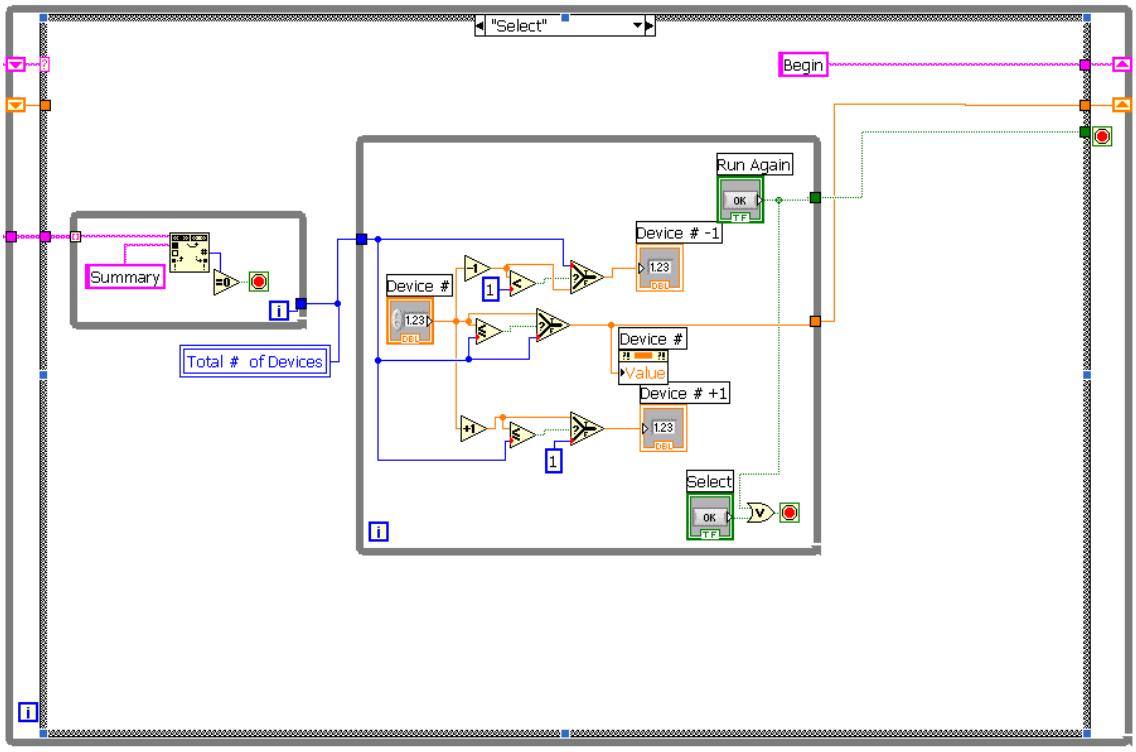

Figure 24 - Discrete Analysis – Select Device State

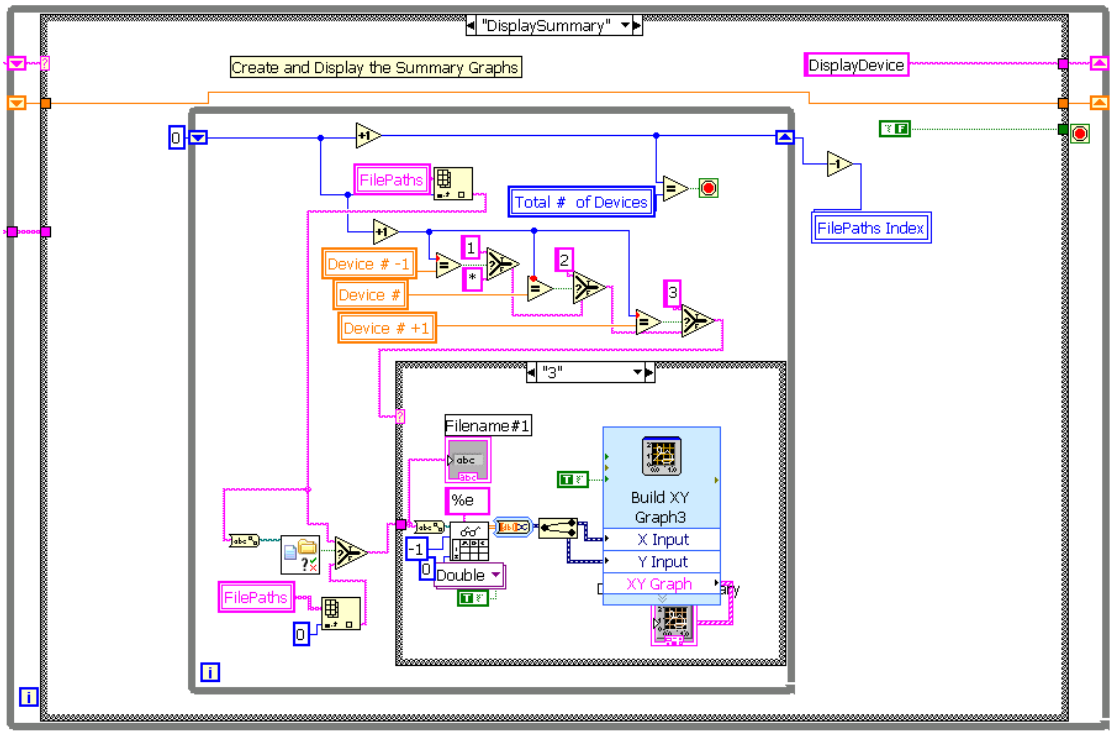

Figure 25 - Discrete Analysis - Display Summary Data State

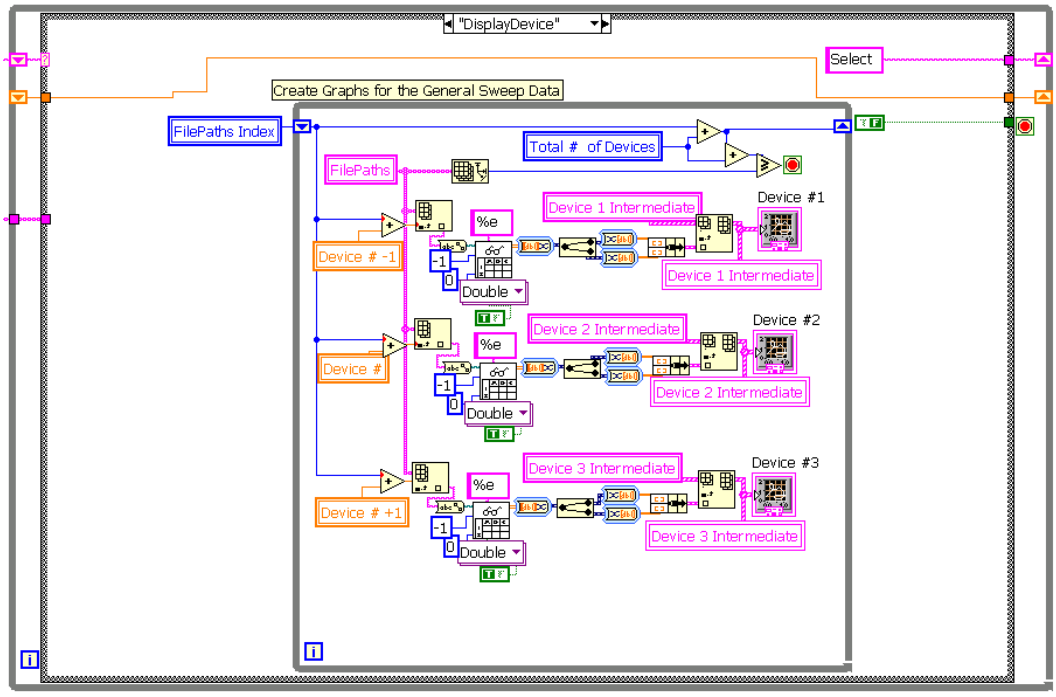

Figure 26 - Discrete Analysis – Display Device Sweep Data State

The DisplayDevice State collects and outputs on the screen the sweep measurements.

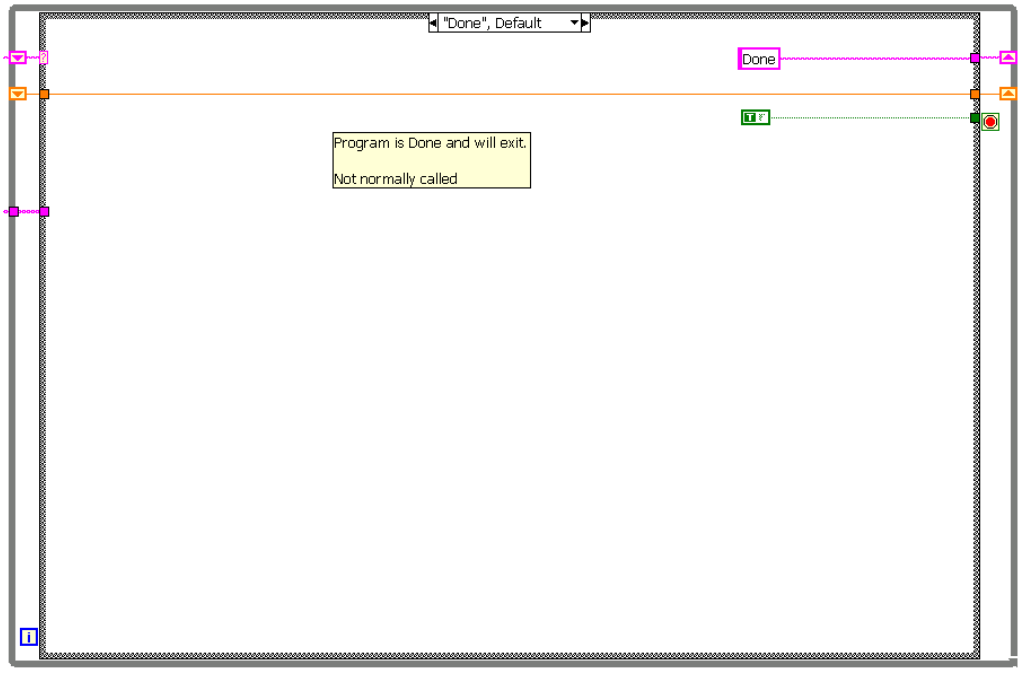

Figure 27 - Discrete Analysis - Done State

The Done state ends the program and also acts as the default error state.

A.3 Discrete Measure v2

This is the workhorse program that takes inputs from the Discrete Analysis program and directly controls the instrument measurements creating the measurement files. This program uses a state machine to control what the current operations the instruments are performing, and on which devices. In the 'Sweep' and 'Bias' states there is a sequence structure that ensures operations in the frames occur in a fixed linear order (i.e. the first is action frame #0, the next is action frame #1, and last is action frame #2)

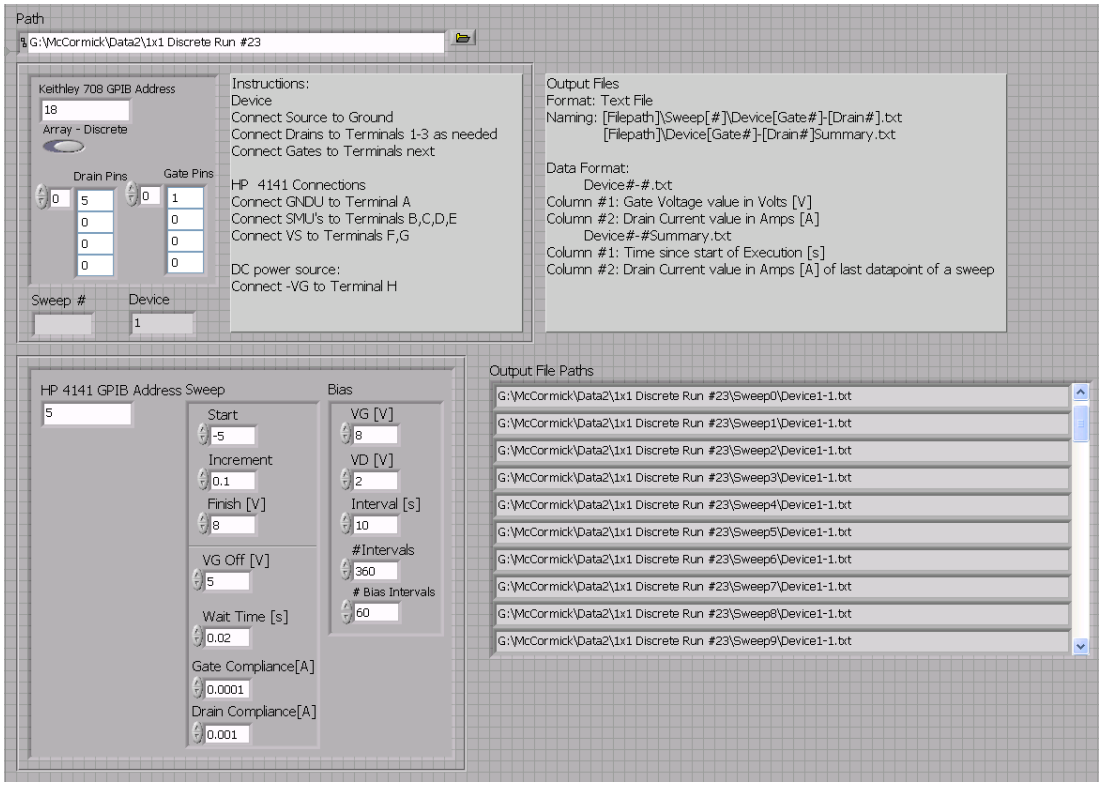

Figure 28 - Discrete Measure Front Panel

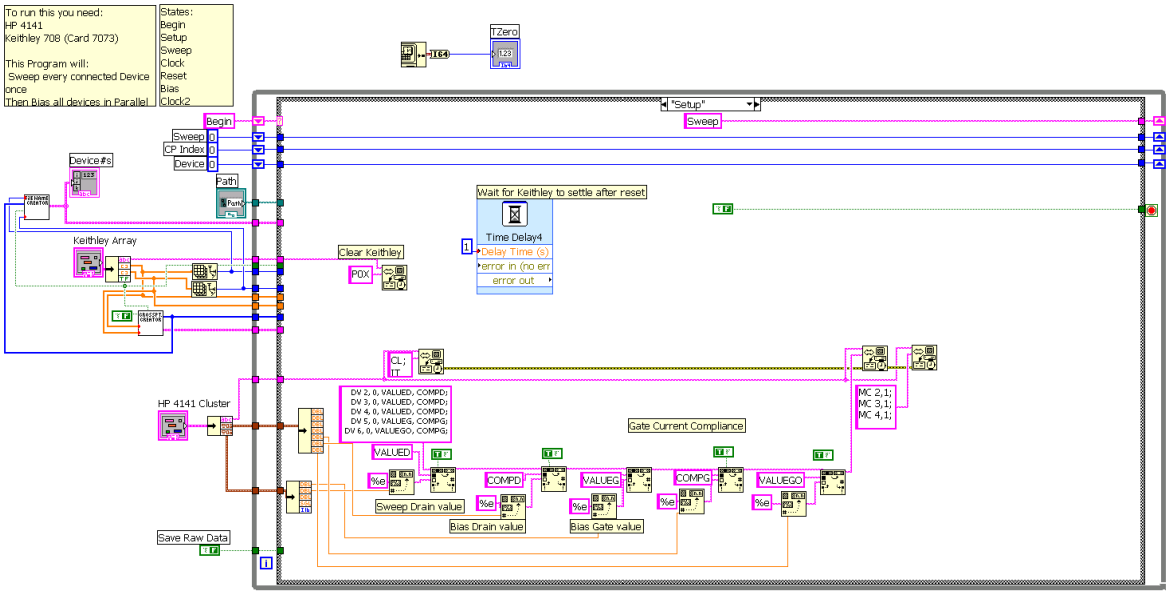

Figure 29 - Discrete Measure Block Diagram

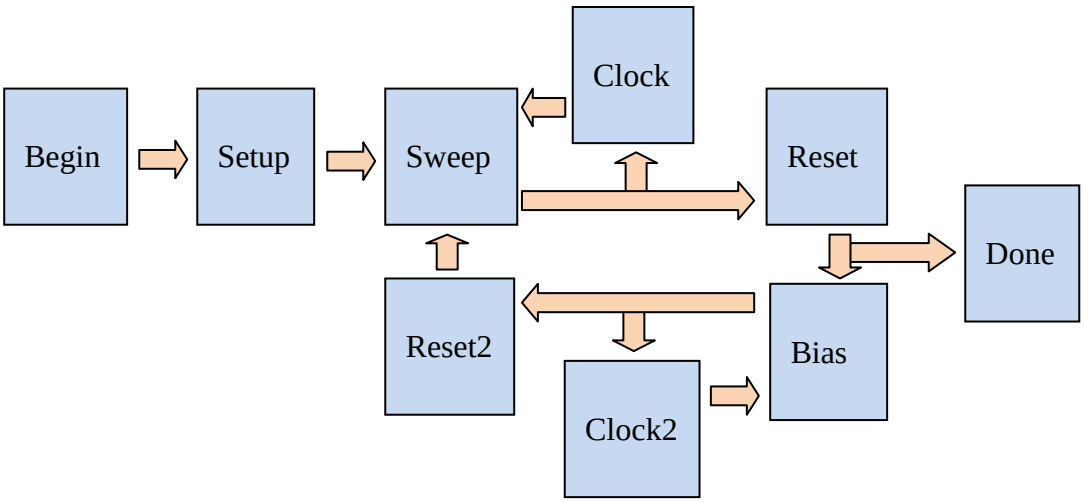

Figure 30 - Discrete Measure State Diagram

The state machine is essentially a linear program that contains three forks. The first fork occurs when you leave the Sweep state, the choice of next state is dependent on if all the devices in the array have been swept (and if no devices remain to be swept the state machine moves to reset), or it moves to clock. A similar decision is made leaving the Bias state resulting in a move to Reset2 or Clock2 if the device remains to be biased. Leaving the Reset state, the state machine moves to the Done state if no more bias sweeps remain, else it moves to the Bias state.

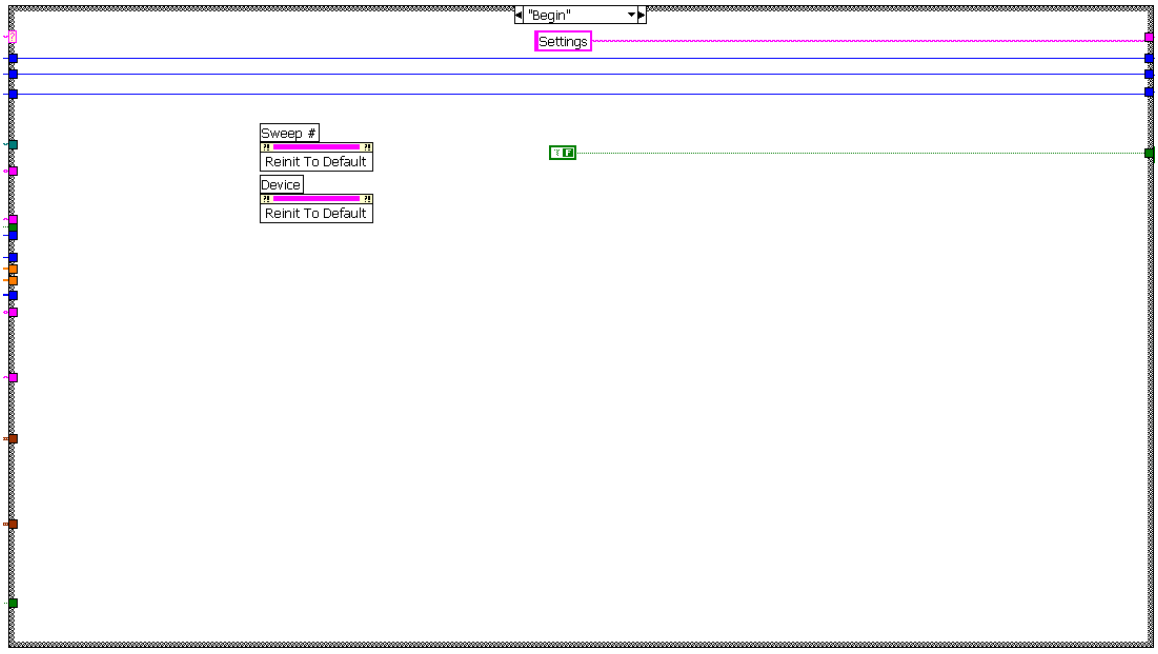

Figure 31 - Discrete Measure - Begin State

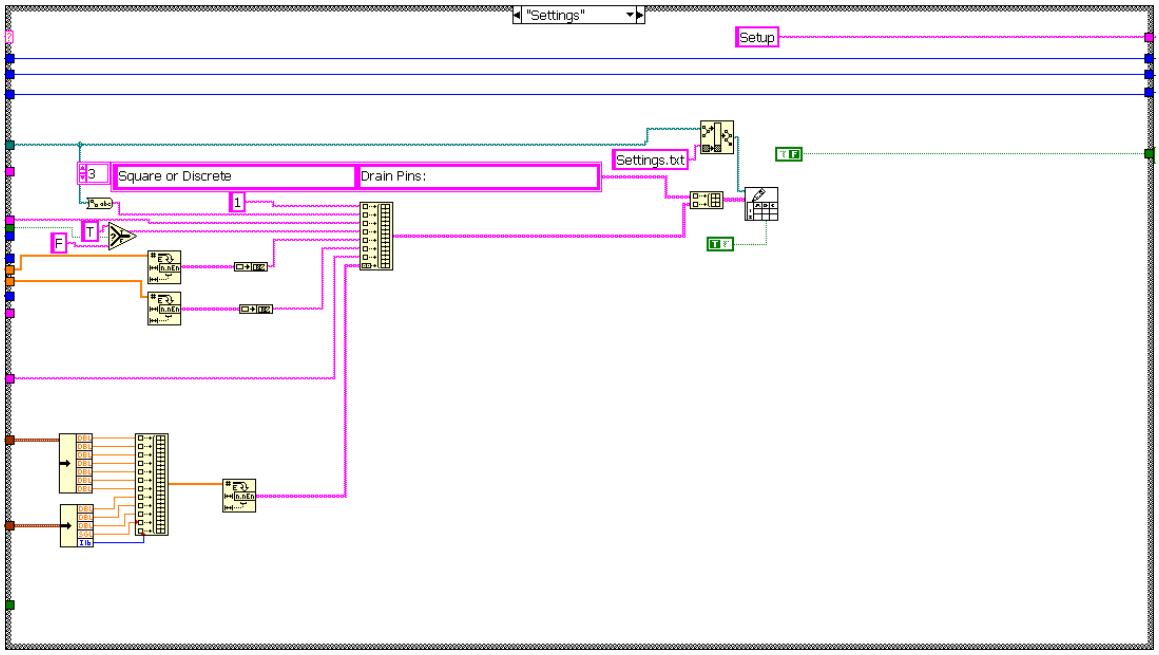

Figure 32 - Discrete Measure - Settings State

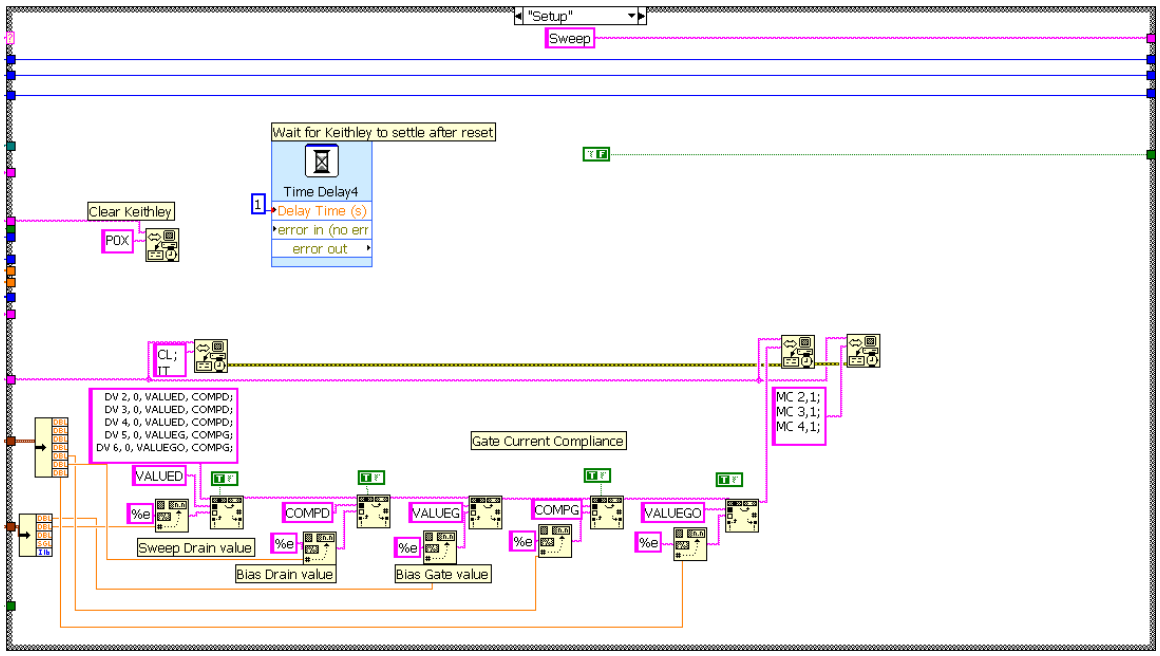

Figure 33 - Discrete Measure - Setup State

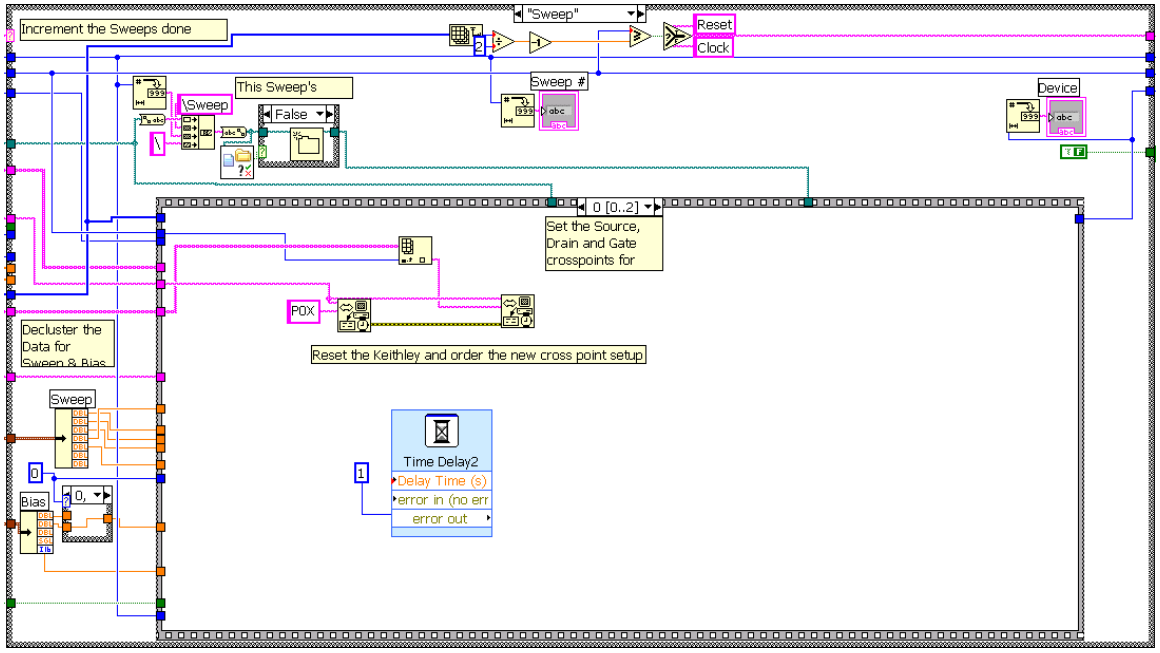

Figure 34 - Discrete Measure - Sweep State with Sequence Action #0 of 2

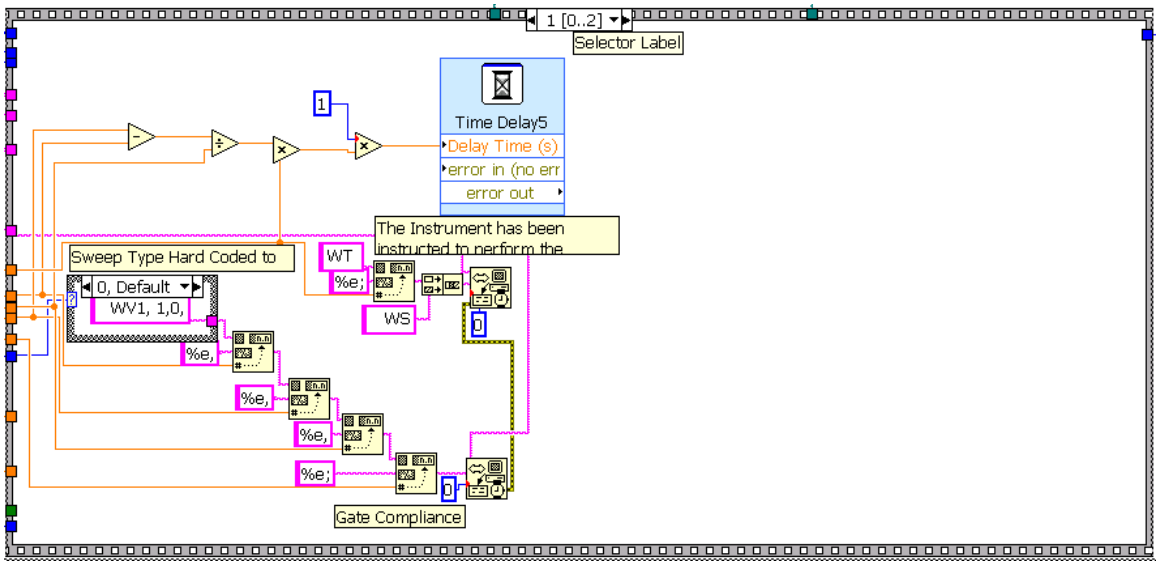

Figure 35 - Discrete Measure - Sweep State – Sequence Action #1 of 2

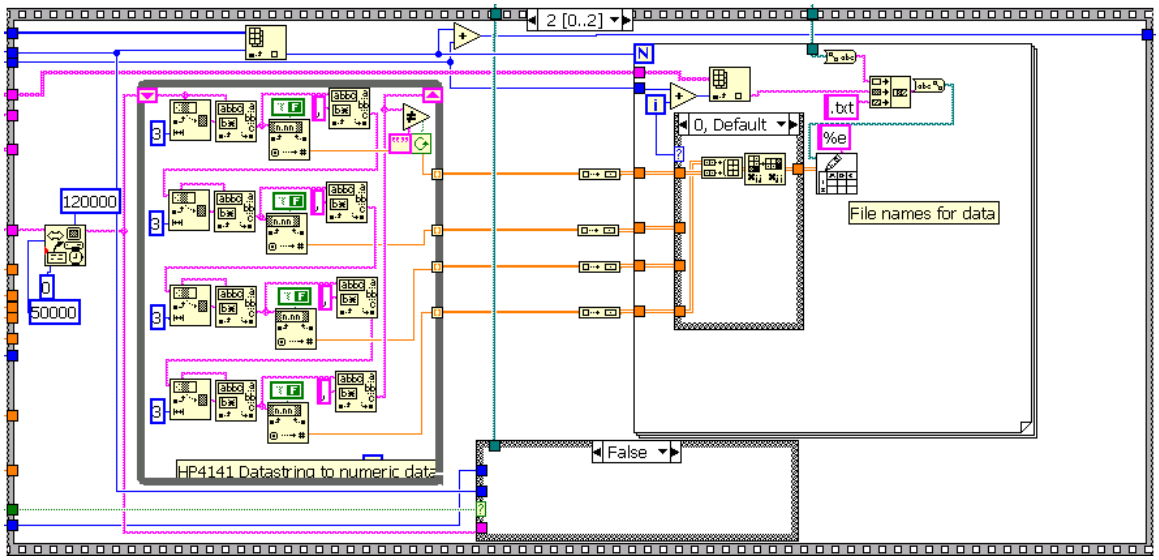

Figure 36 - Discrete Measure - Sweep State – Sequence Action #2 of 2

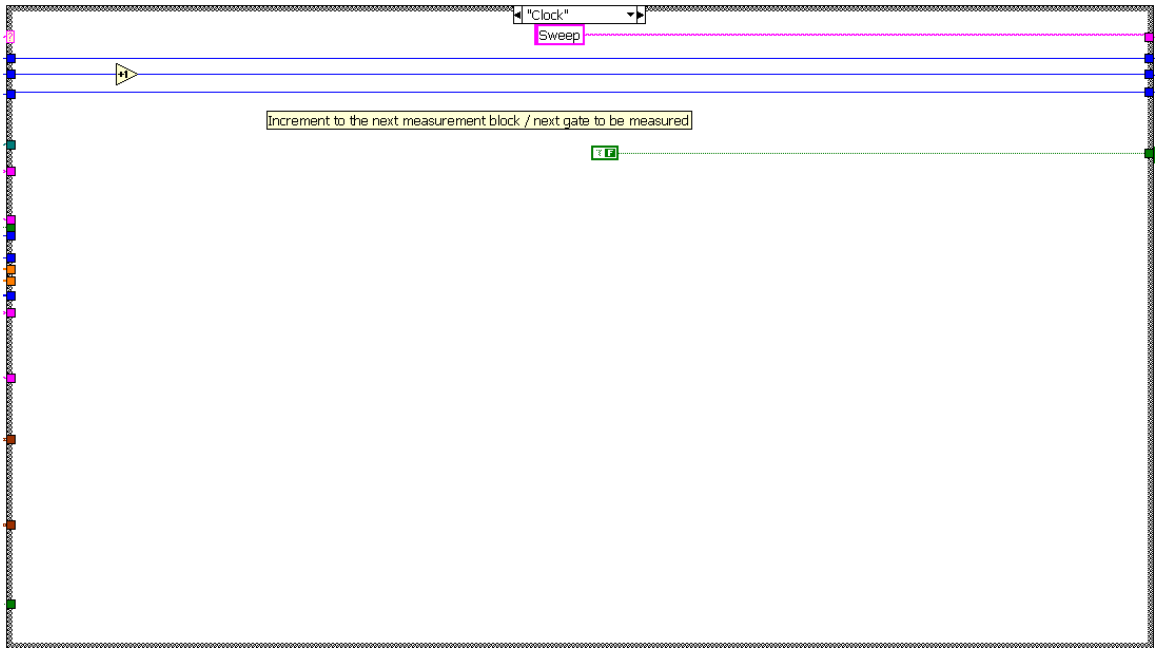

Figure 37 - Discrete Measure - Clock State

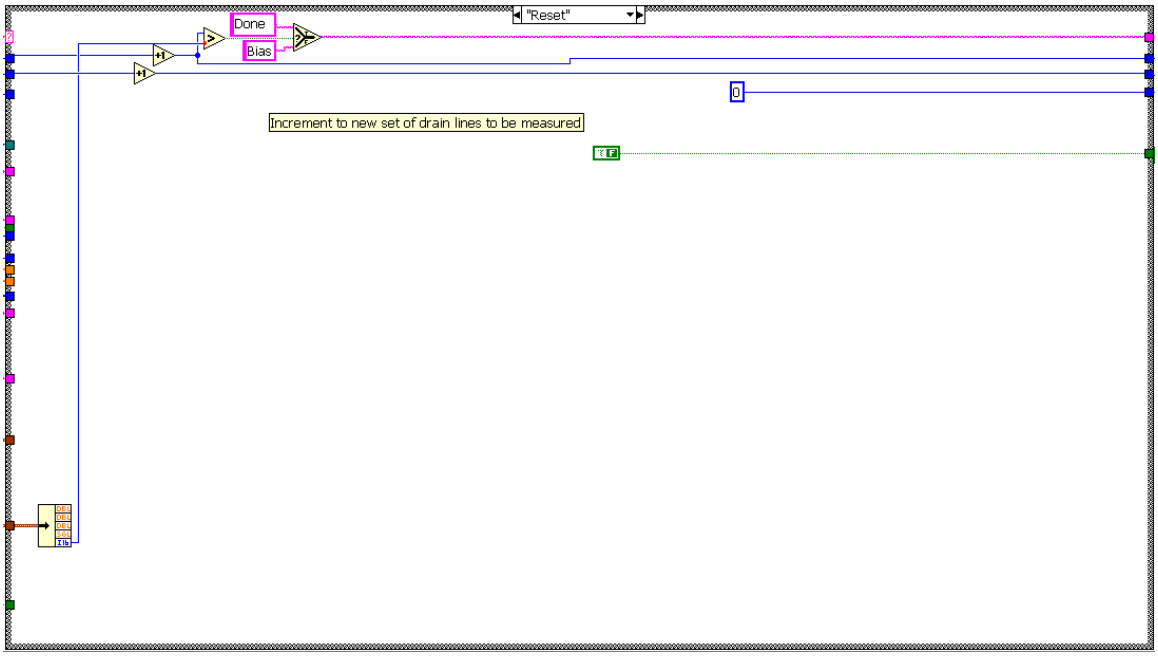

Figure 38 - Discrete Measure - Reset State

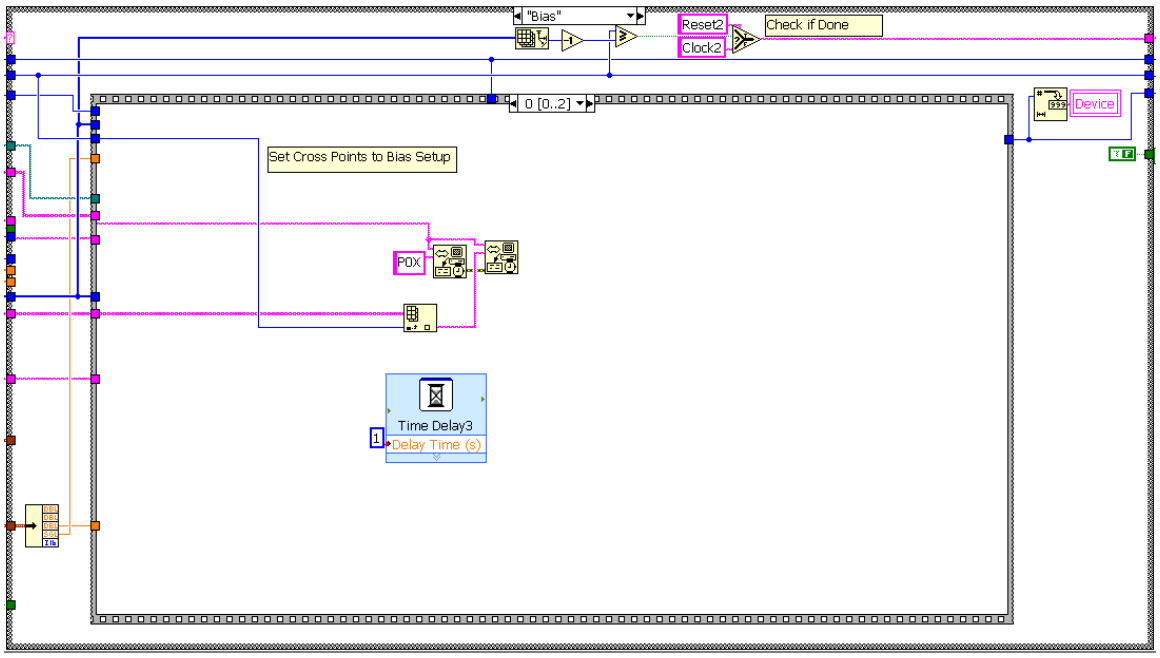

Figure 39 - Discrete Measure - Bias State with Sequence Action #0 of 2

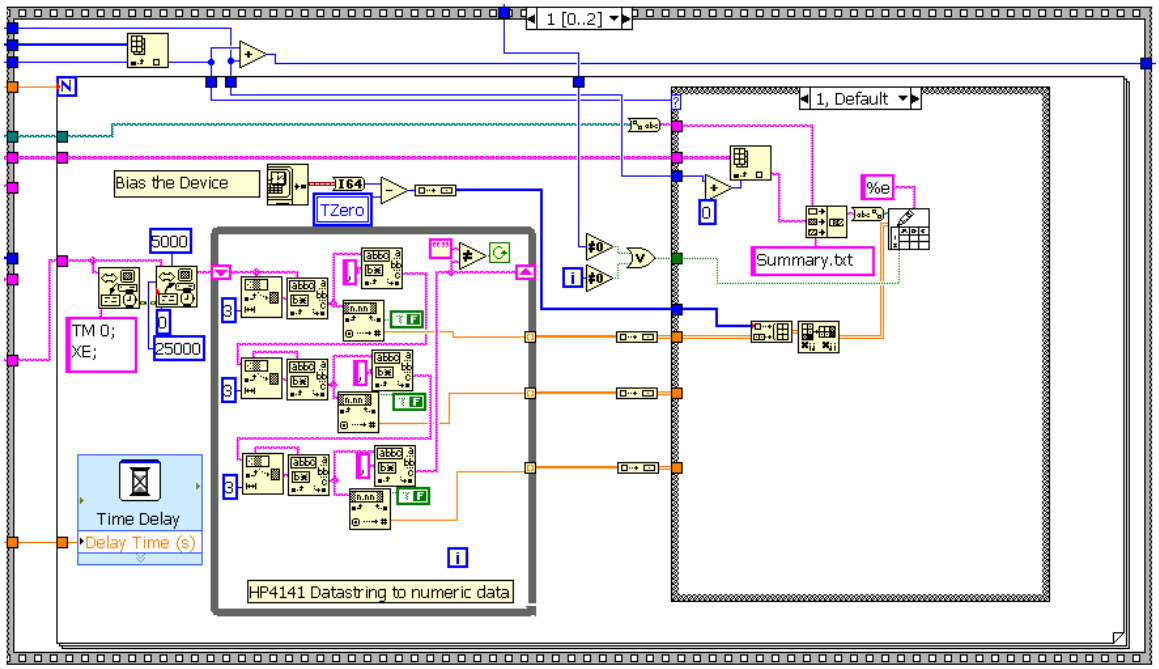

Figure 40 - Discrete Measure - Bias State – Sequence Action #1 of 2

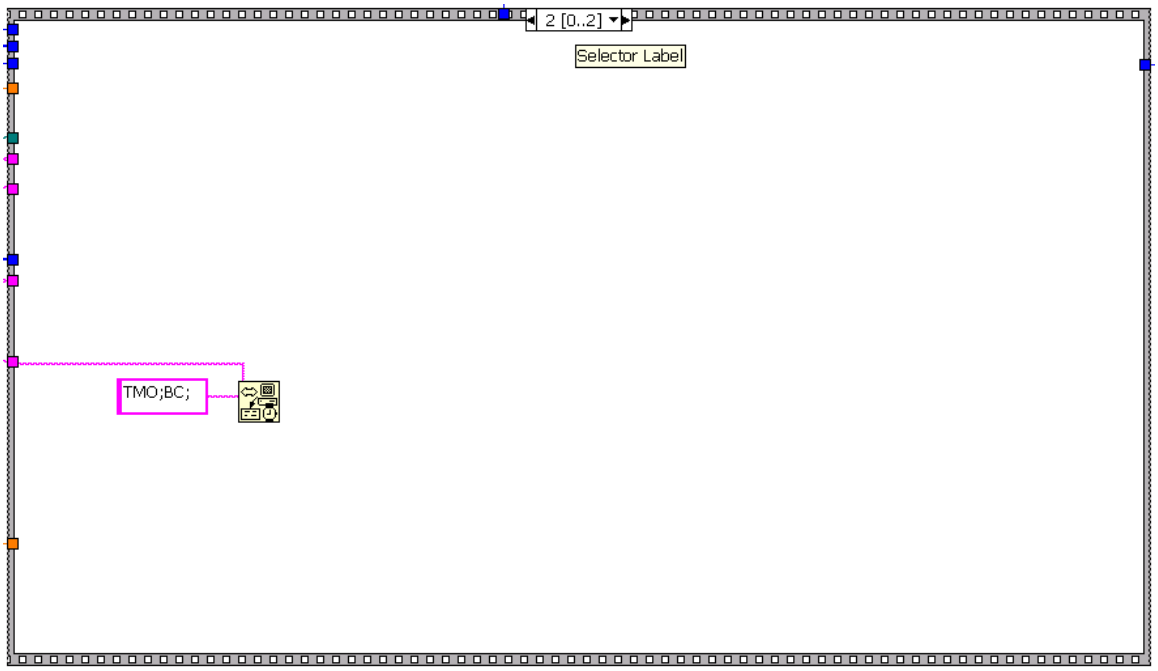

Figure 41 - Discrete Measure - Bias State - Sequence Action #2 of 2

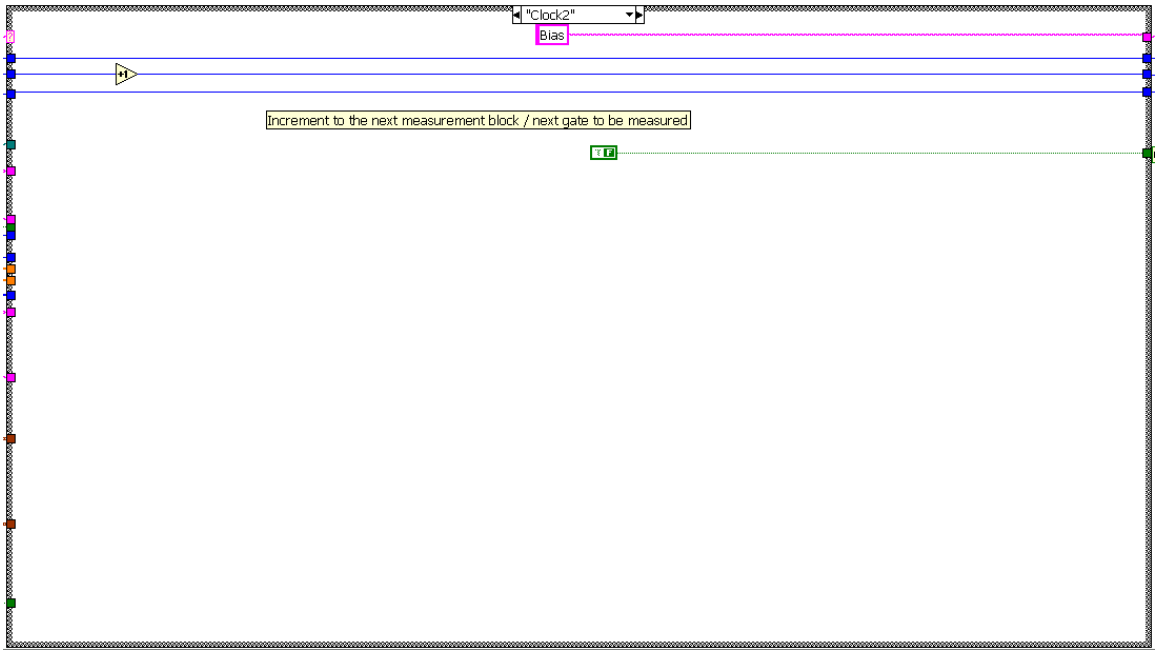

Figure 42 - Discrete Measure - Clock2 State

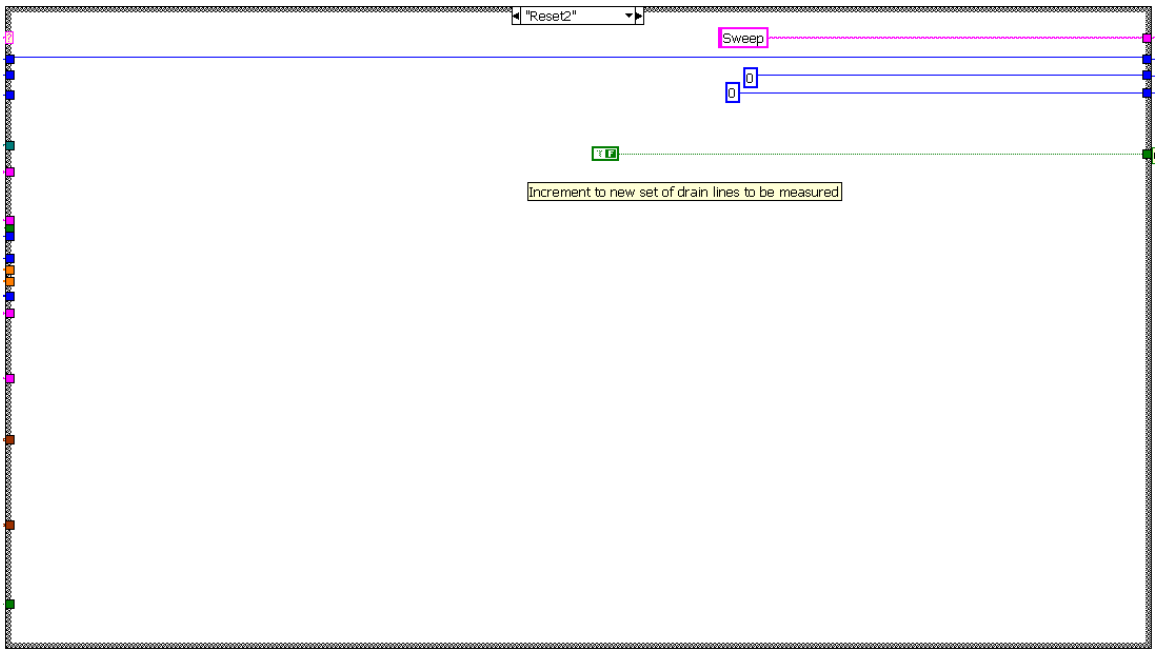

Figure 43 - Discrete Measure - Reset2 State

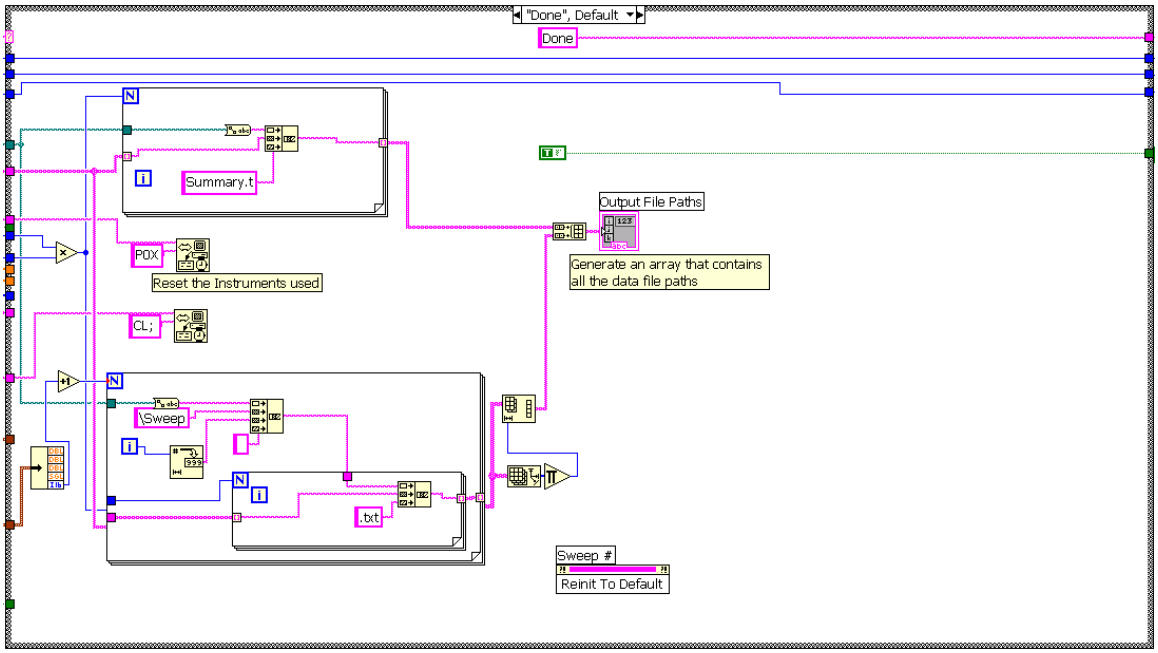

Figure 44 - Discrete Measure - Done State

A.4 File Name Creator

This program creates all the filenames to be used in Discrete Measure. The choice between discrete and array changes whether the number of file names generated will be the minimum of: (number gate lines, number drain lines), instead of the product of the number of gate lines and drain lines.

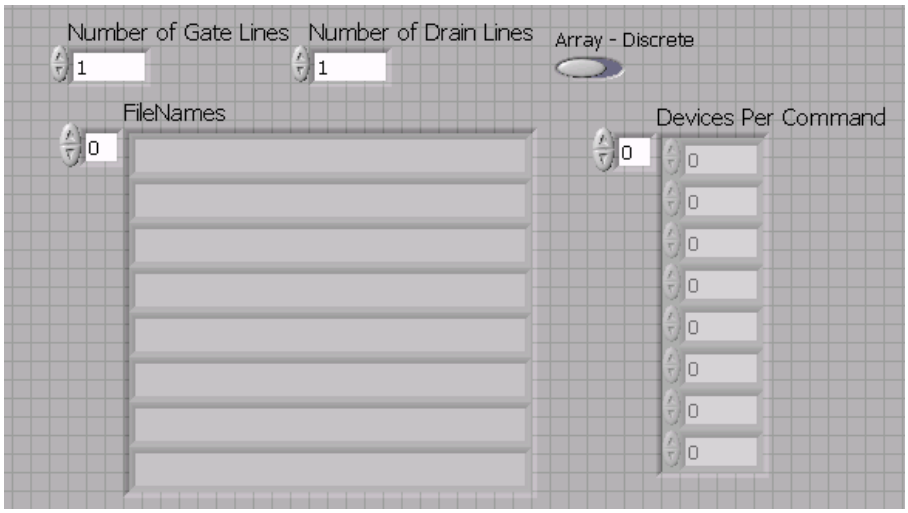

Figure 45 - File Name Creator Front Panel

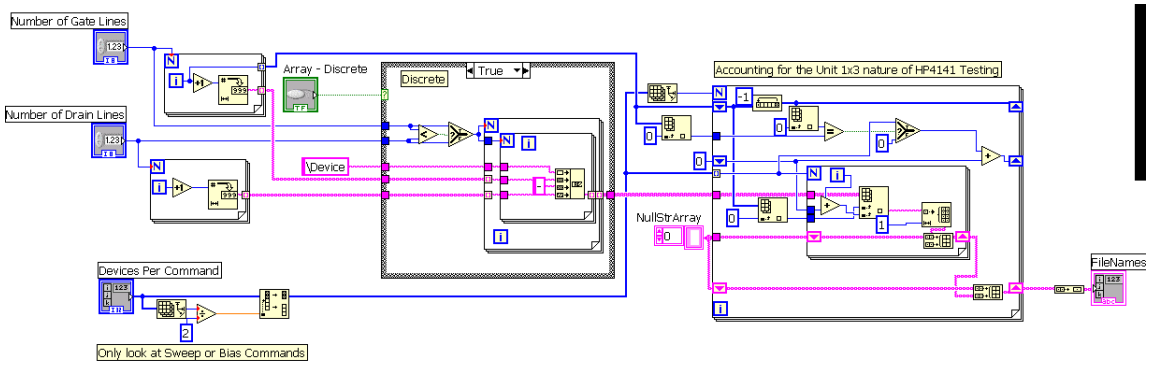

Figure 46 - File Name Creator Block Diagram

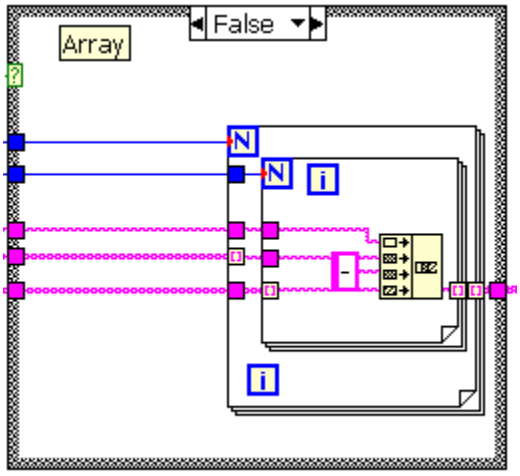

Figure 47 - File Name Creator - Array Setup

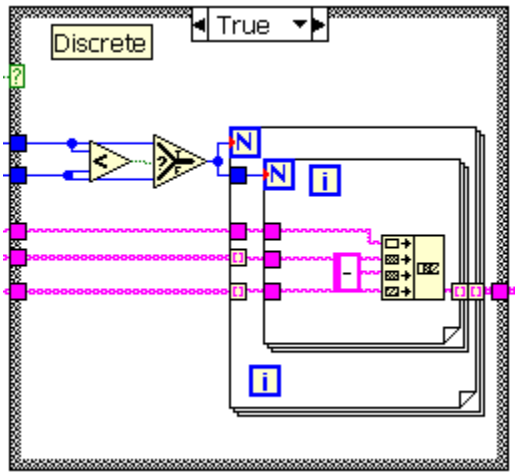

Figure 48 - File Name Creator - Discrete Setup

A.5 Cross Point Creator

This program creates the commands for the Keithley Switching matrix used in Discrete Measure. The cross points are the points in the switching matrix card that are either opened or closed to create an electrical connection between two connections on the instrument.

There are two choices that can be made in this program: the inclusion of the source pins to the cross point commands and whether the commands describe an array of devices or discretely connected devices. The choice of discrete results in cross point commands created for the minimum of (gate pins, drain pins) device instead of the product of the number of gate pins and drain pins indicated.

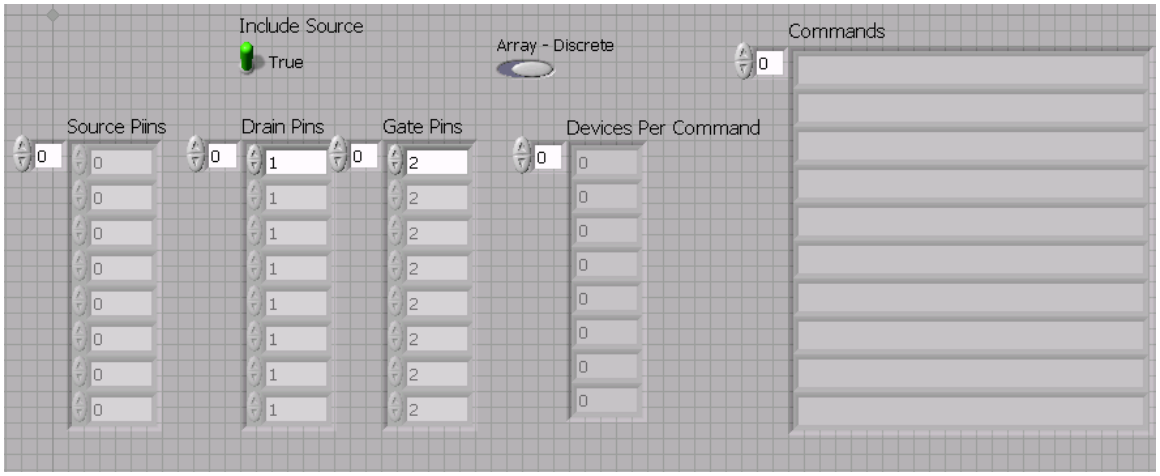

Figure 49 - Cross Point Creator Front Panel

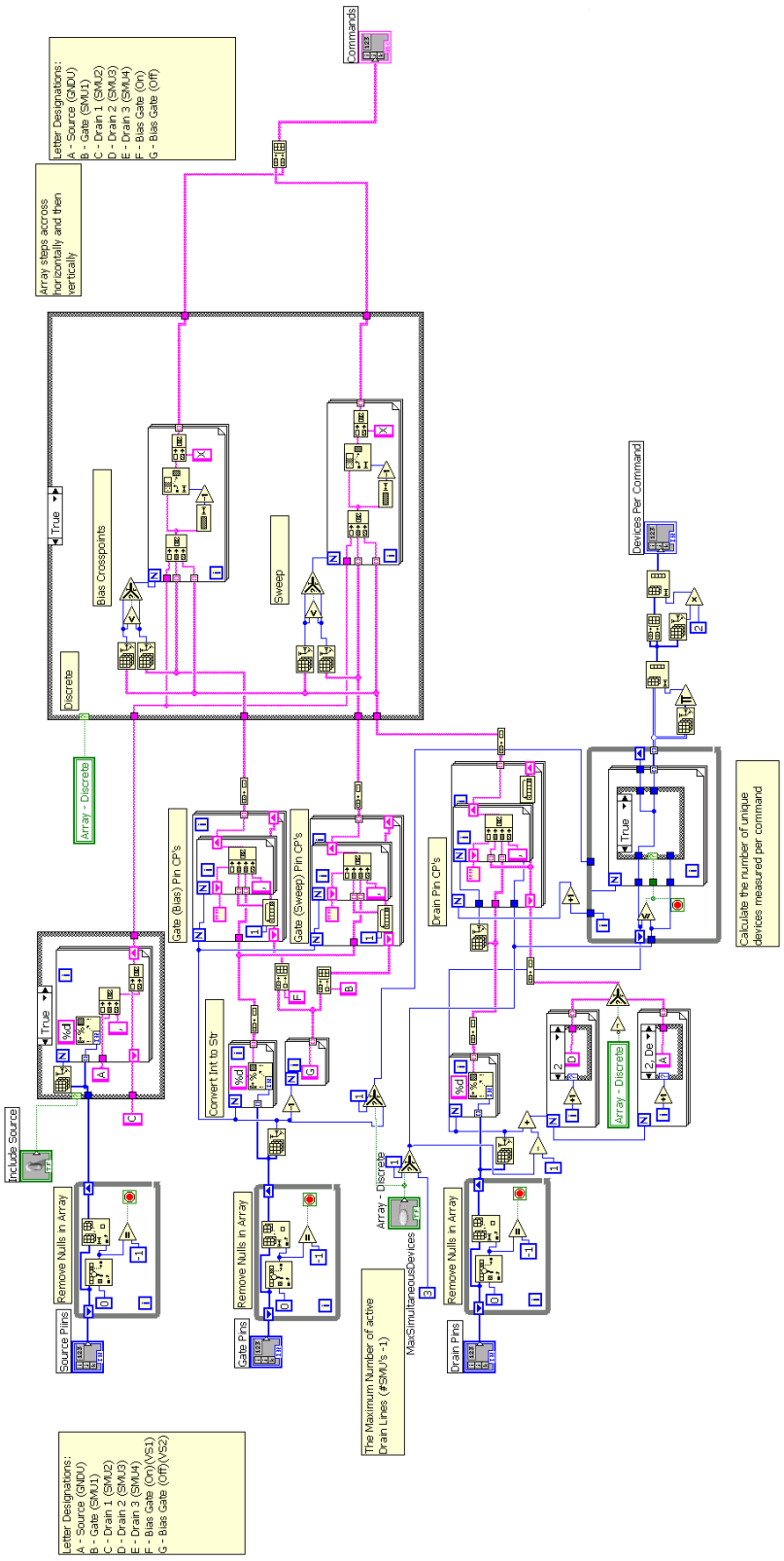

Figure 50 - Cross Point Creator Block Diagram

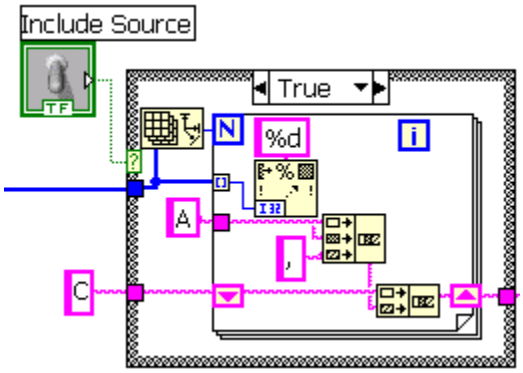

Figure 51 - Cross Point Creator - Test Pin out Includes Source = True

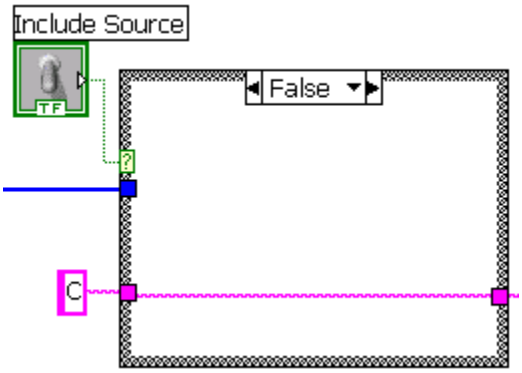

Figure 52 - Cross Point Creator - Test Pin out Includes Source = False

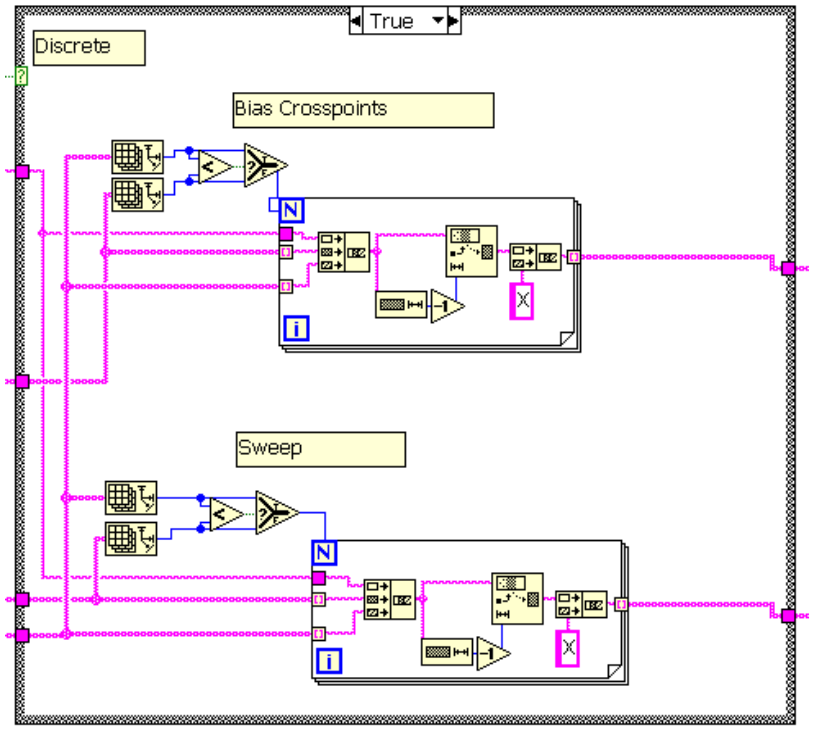

Figure 53 - Cross Point Creator - Discrete Device Pin out

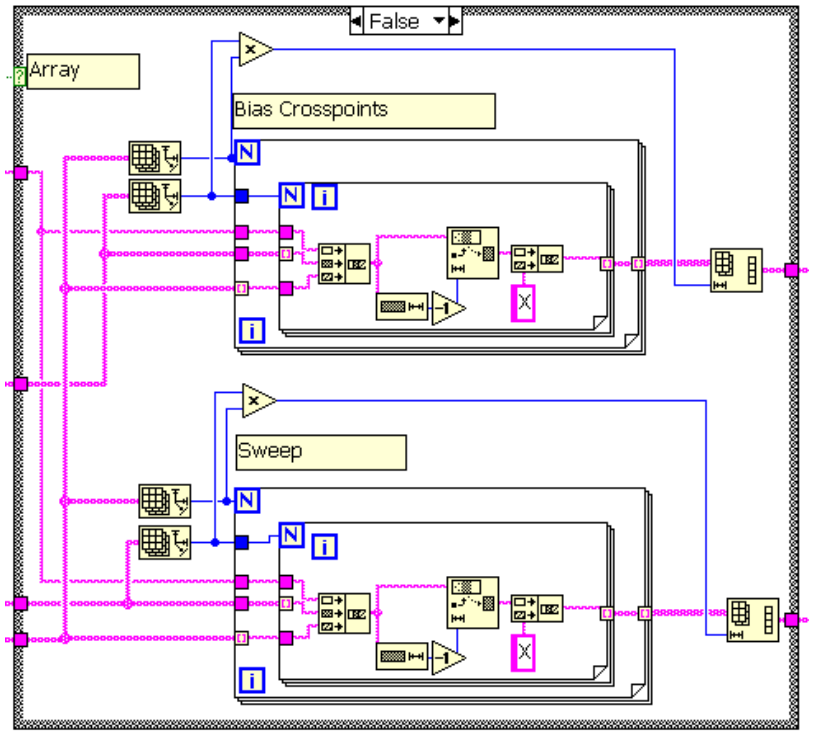

Figure 54 - Cross Point Creator - Array Device Pin out

Appendix B: Temperature Measurement System

This section describes the temperature measurement system in more detail. Section B.1 Temperature Measurement User Manual describes the setup and use of the system. Sections B.2, B.3, and B.4 go into depth about the LabView testing suite created to measure the thermal sensor array with the NI data acquisition board (6229).

B.1 Temperature Measurement User Manual

The section will describe the proper method to setup and use the temperature measurement system.

B.1.1 Temperature Measurement System Setup

1. Gather materials
   - Computer with NI 6229 installed
   - NextGen circuit Board
   - Four DC power sources
   - Two 68-Pin NI connector cables
   - Two or more blue ribbon cables
   - 9-pin serial cable (only one male adapter needed)
2. Connect the instruments to power.
3. Connect the NI 6229 to the two 68 pin to 38 pin RS-232 breakout boards
   - 68-pin Connector 0 goes to board 0
   - 68-pin Connector 1 goes to board 1
4. Plug the RS-232 cable labeled Gate into the NexGen Board in
5. Plug the RS-232 cable labeled Drain into the port labeled UIUC Output
6. Connect the NextGen Board to the DC bias sources using the 9 pin connector
   - The DC biases connected are ground, $V_{G\,On}$ & $V_{G\,Off}$.
7. Connect the Modified Bias board to the DC sources
   - The DC biases connected are ground, I_{Bias} & V_{DD}.

8. Plug the blue ribbon cables from the sample into the appropriate ports
    - Attach Drain cables to “UIUC Output” starting with the right
    - Attach Gate cables to the “Gate” connections starting with the right

B.1.2 How to use the Temperature measurement system

1. Bond the sample
    1. ACF Bond Sample to Blue Ribbon Cables
    2. ACF Bond Sample Bias Lines to modified bias board
2. Turn on computer & power supplies
3. Plug the blue ribbon cables to NextGen Board
4. Set desired bias voltages & current
5. Load SEThermalTemperatureMap(16x16).vi
6. Select the file path to save files
7. Select the reference data source
8. Select the color scales & the bounds
9. Press “Run” to start the LabView program
10. Set the switch to “array” or “row”
11. Select Single ended or Differential ended
12. Toggle “Record” to save the measurement to file
13. Press “Break” to end the LabView program

B.2 SEThermalTemperatureMap(16x16)

This is the main LabView program that interacts with the user and the NI 6229 DAQ and can handle a maximum of a 16x16 sample array.

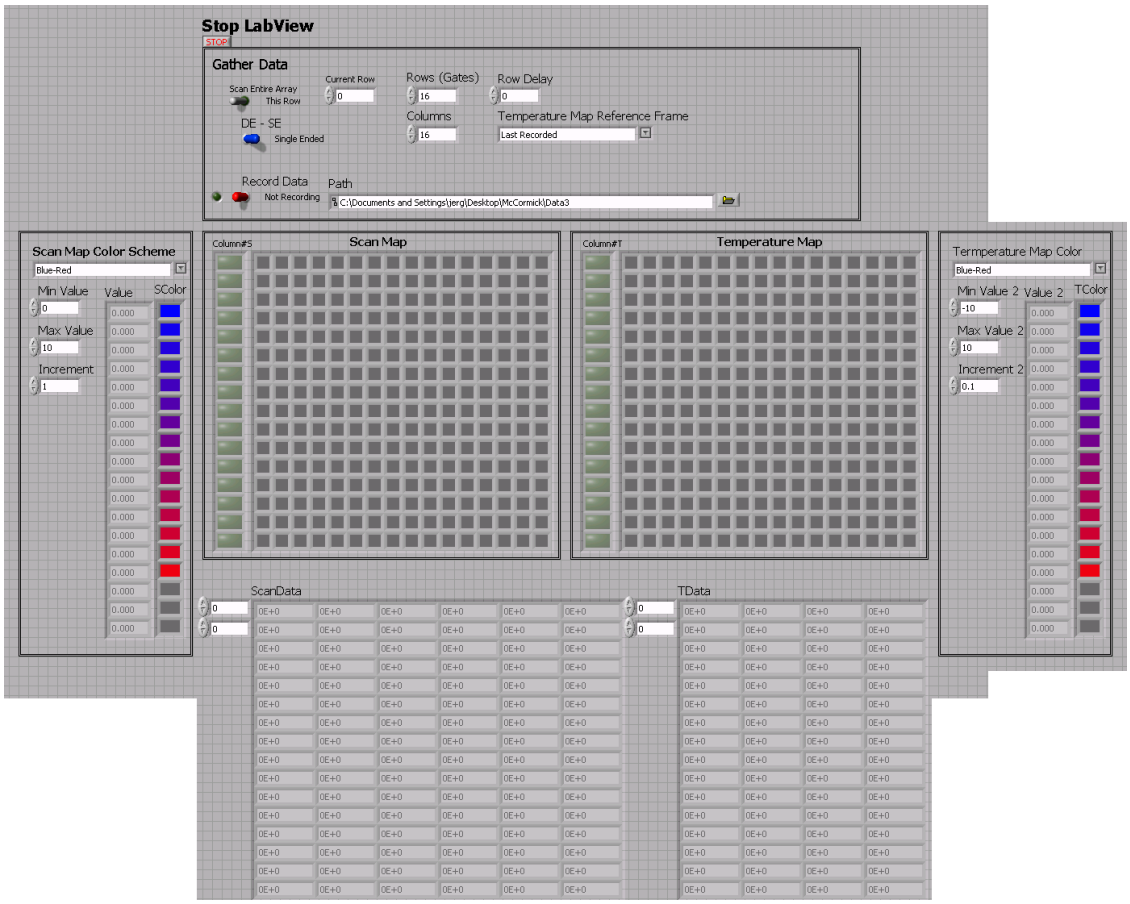

Figure 55 - SEThermalTemperatureMap(16x16) Front panel

The top box contains the controls for operating the program. The boxes on the far left and far right allow the selection of the scan map and temperature map color schemes and legends. The middle boxes provide the visual image of the scan and temperature maps with the data matrices listed below showing the actual measured values.

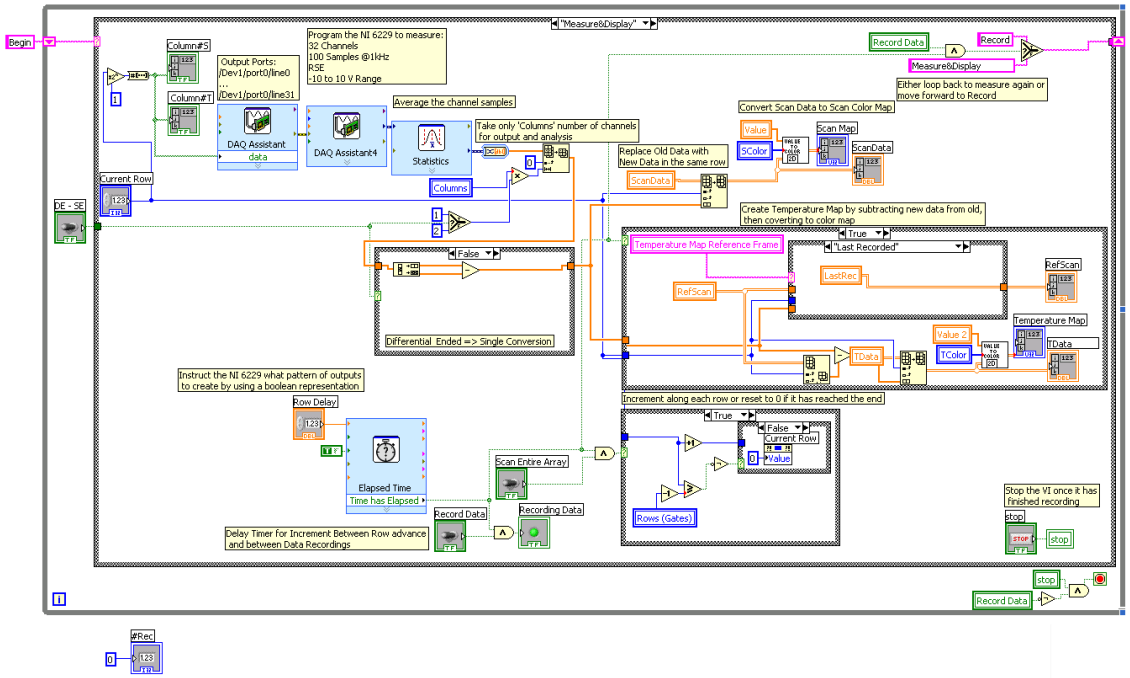

Figure 56 - SEThermalTemperatureMap(16x16) Array - Block Diagram

The structure of this program is to step through a state machine that controls the operations of the program. The general flow of the states is seen below in Figure 57.

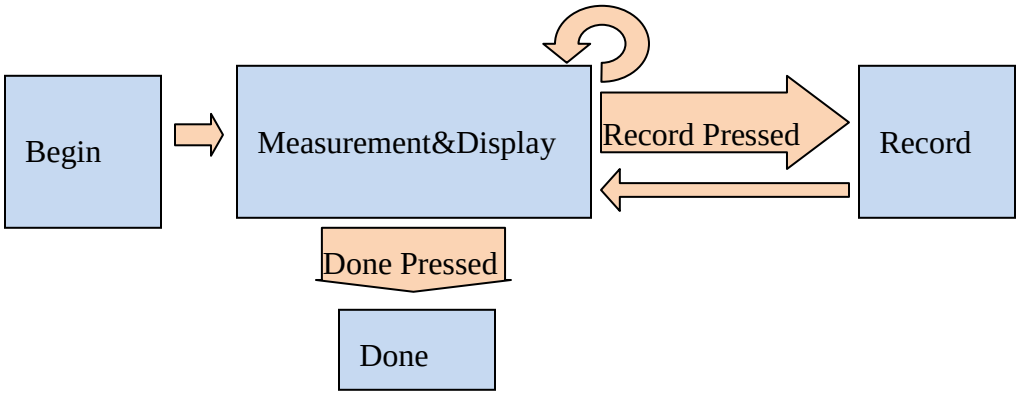

Figure 57 - SEThermalTemperatureMap(16x16) - State Diagram

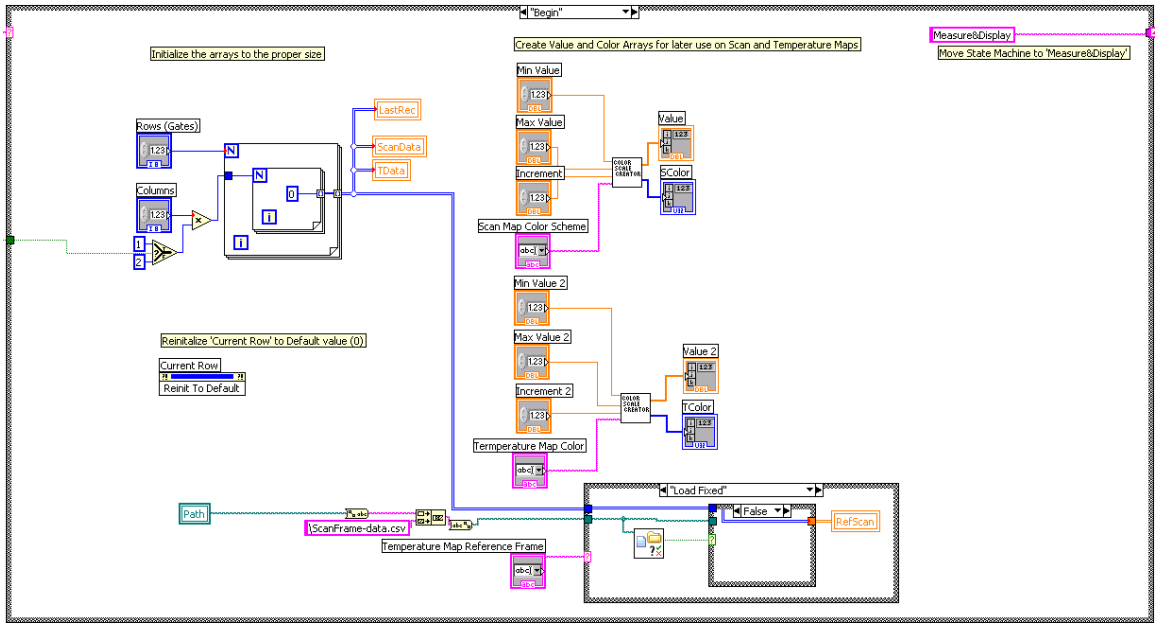

Figure 58 - SEThermalTemperatureMap(16x16) – Begin State

The Begin state is initializing and building the comparison and RGB arrays.

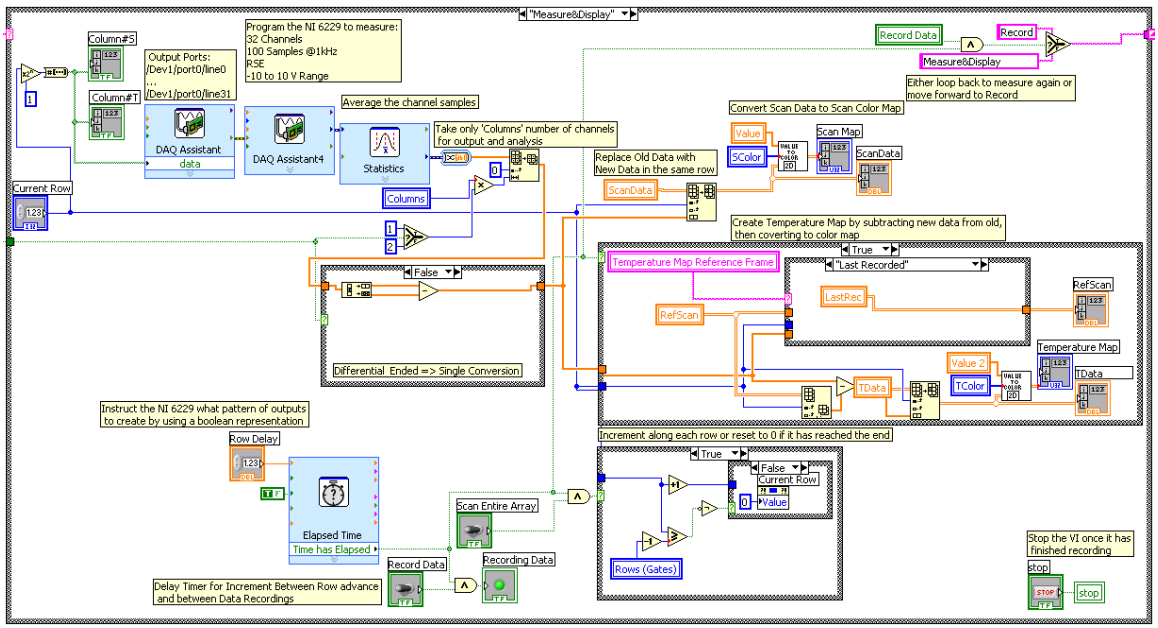

Figure 59 - SEThermalTemperatureMap(16x16) - Measure&Display State

This is the main program state. The DAQ control is in the upper left hand corner of this program frame. The case structure in the center takes care of the single ended-

differential ended data processing. The case structure in the center-right handles the temperature array mapping. The code near the bottom of this state controls which row of the array is active and amount of time taken between switching.

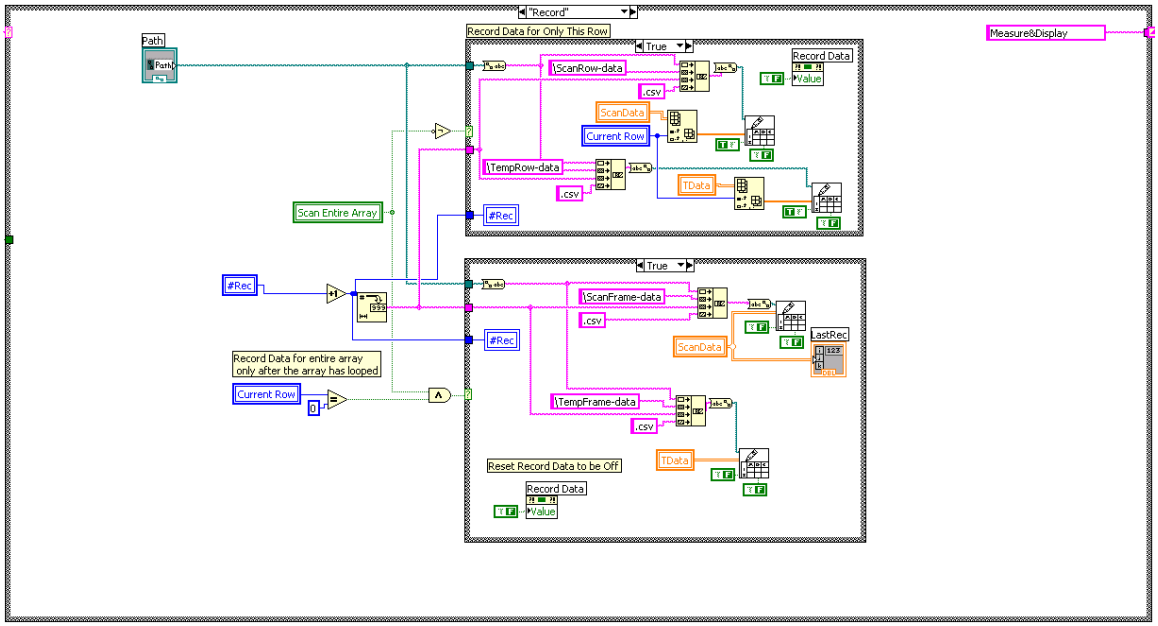

Figure 60 - SEThermalTemperatureMap(16x16) – Record State

In this state the data being recorded is saved to file. The upper case structure operates only if a single row is being recorded, while the lower case structure is only if the whole array is being measured.

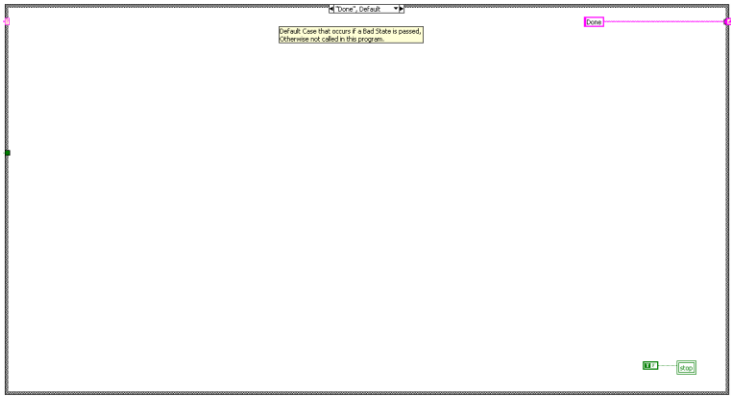

Figure 61 - SEThermalTemperatureMap(16x16) – Done State

The done state is the default error state and exits the program.

B.3 Color&ValueScaleCreator

This is the LabView program that creates the mapping between the color scale chosen and the resolution of voltages. The front panel allows you to choose the color scheme choice, the min & max values and the step size of the comparison array.

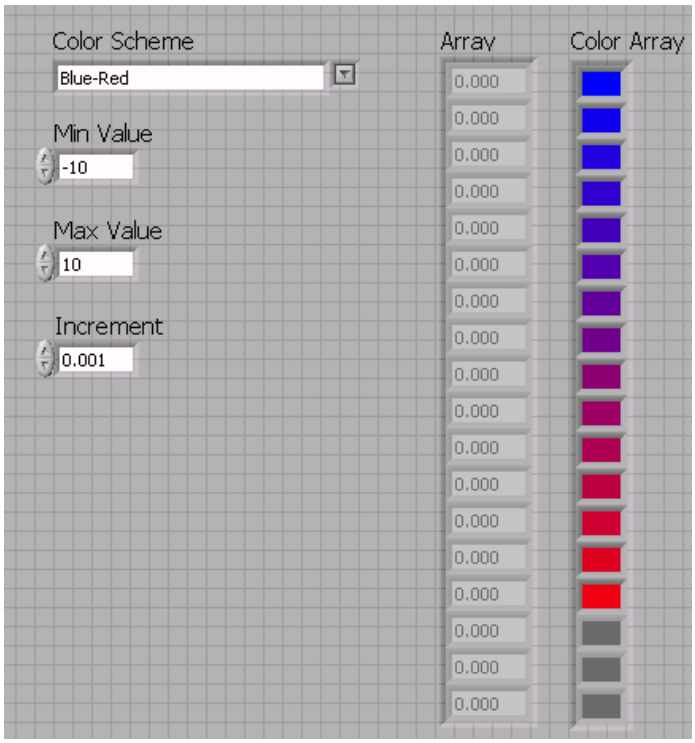

Figure 62 - Color&ValueScaleCreator Front Panel

In this program the comparison array is created by iteration. The RGB color array is create through another iterating loop with special ratios of red, blue & green depending on the color scheme chosen.

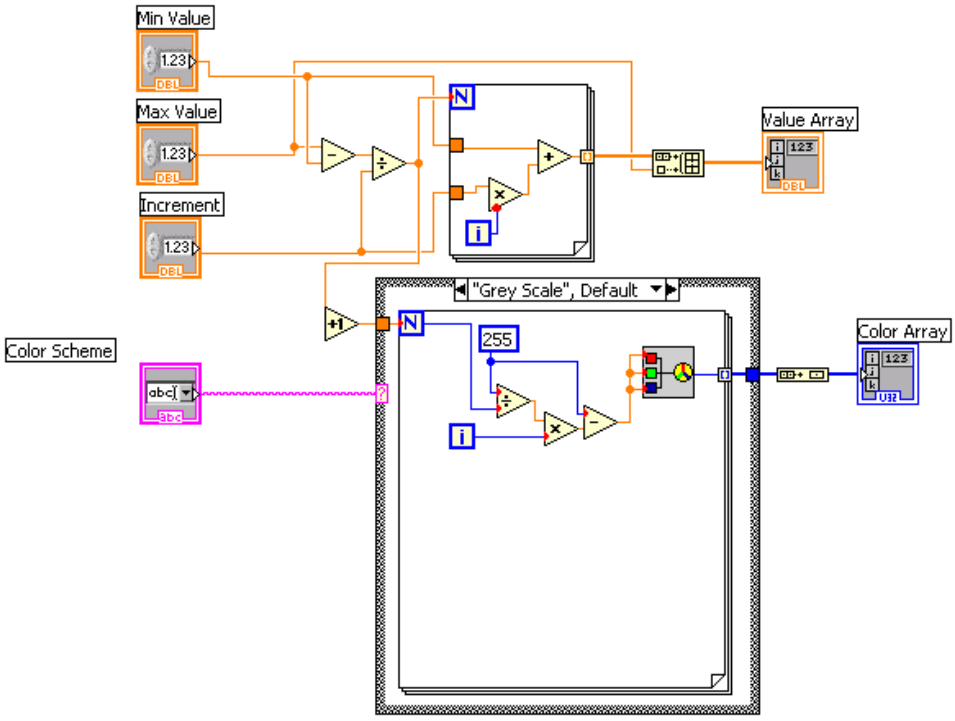

Figure 63 - Color&ValueScaleCreator Block Diagram

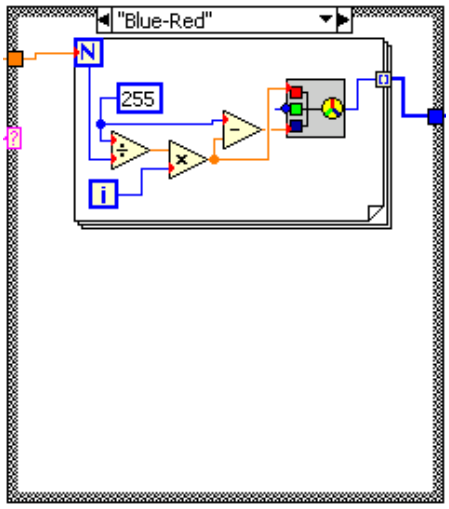

Figure 64 - Color&ValueScaleCreator - Blue-Red Palette Option

B.4 ValuetoColor2d

This program performs the conversion between voltage values and colors. This program takes in the 2-d data array, RGB color array and the comparison array. This program outputs a 2-d RGB color array.

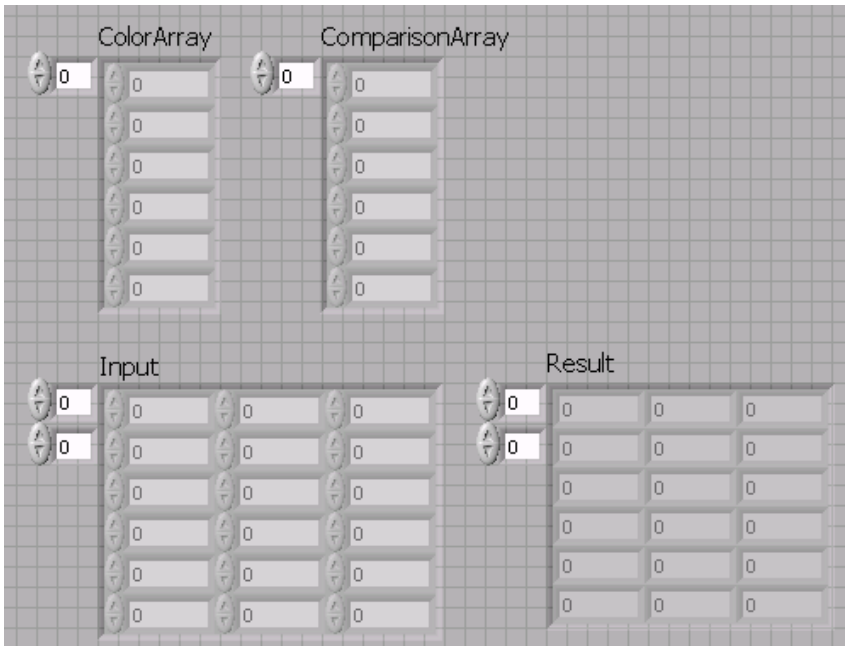

Figure 65 - ValuetoColor2d Front Panel

This program steps through all the inputs and compares each of them against the comparison array until a matching range is found or the input has been found to be out of bounds.

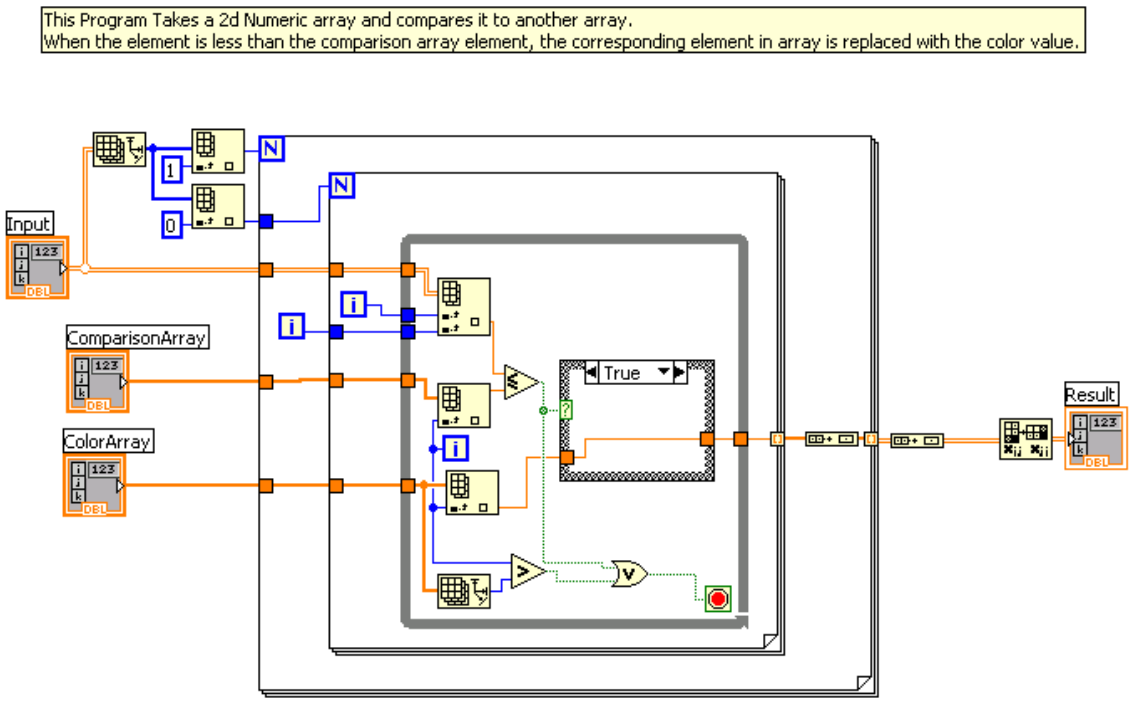

Figure 66 - ValuetoColor2d Block Diagram

Appendix C: Device Fabrication Steps

The standard procedure used in the Center for Thin Film Devices to create the passivated samples on a glass substrate used in the experiments followed these steps in their creation:

1. Clean substrate
    a. Use a high pressure DI water jet to clean visible particles off the surface
    b. Piranha (H_2SO_4:H_2O_2 to 4:1)
    c. Rinse in Acetone
    d. Rinse in IPA
    e. Use nitrogen gas to blow sample dry
2. Use Ion Mill sputtering to deposit Gate Metal onto sample (1000 Å Cr)
3. Gate Patterning
    a. Spin 1811 at 4000 RPM for 30 seconds
    b. Softbake at 90ºC for 90 seconds
    c. Expose using g-line light source until 1811 is fully exposed (20s)
    d. Develop using 351: H2O at a 1:5 ratio until fully developed (80s)
    e. Use metal etchant (ACN:HNO_3:H_2O to 1g:10 mL:100 mL)
4. Deposit PEALD Al_2O_3 (320 Å)
5. Deposit PEALD ZnO (100 Å)
6. Pattern the zinc oxide
    a. Spin 1811 at 4000 RPM for 30 seconds
    b. Softbake at 90ºC for 90 seconds
    c. Expose using g-line light source until 1811 is fully exposed (20s)
    d. Develop using 351: DI H2O at a 1:5 ratio until fully developed (80s)
    e. Etch the ZnO using Dilute HCL that has an etch rate is 10 nm/minute (HCl: H_2O is 1:4000)
7. Etch the oxide to expose the via for the gate contact
    a. Spin 1811 at 4000 RPM for 30 seconds
    b. Bake at 90ºC for 90 seconds

   c. Expose using UV light source until 1811 is fully exposed (20s)
   d. Develop using 351: DI H2O at a 1:5 ratio until fully developed (80s)
   e. Etch the Al_2O_3 using hot phosphoric acid with an etch rate of 30 nm/min (H_3PO_X at 80ºC)
8. Create Source and Drain Pattern using double layer lithography
   a. Spin PMMA onto the sample at 4000 RPM for 30 seconds
   b. Bake the sample at 160ºC for 10 minutes
   c. Allow substrate to cool
   d. Spin 1811 at 4000 RPM for 30 seconds
   e. Soft bake at 90ºC for 90 seconds
   f. Expose using g-line light source until 1811 is fully exposed (20s)
   g. Develop using 351: DI H2O at a 1:3 ratio until fully developed (80s)
   h. RIE for 7 minutes to remove mixed layer of PMMA and photoresist
   i. Expose using Deep UV for 400s
   j. Develop PMMA using Toluene until fully developed (40s)
9. RIE for 1 minute to create an n+ region on the source and drain regions
10. Sputter the contact metal (1500 Å titanium)
11. Perform lift off of the contact metal
12. Deposit a thin film (300 Å) of Al_2O_3 to passivated the sample surface.

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