PULSED LANGMUIR PROBE DEVELOPMENT FOR SMALL SATS

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ABSTRACT

Langmuir probes have a rich history in the satellite community and have found a place on many university and industry missions. The Langmuir probe, named after Irving Langmuir for his contributions to probe theory, is a prevalent electrostatic probe used to characterize plasmas. In the 1970s, research into electrode contamination revealed that Langmuir probe measurements can be severely impacted by contaminants on the probe. Several methods were developed to address contamination; however, these methods are rarely put into practice despite an improvement in performance. A pulsed method of probing was introduced in the 1970s by the Naval Research Laboratory in response to the contamination research. This work addresses the development of a pulsed Langmuir probe (pLP) for use on small satellites in the terrestrial ionosphere.

A CubeSat is a picosatellite defined by the specifications set forth by California Polytechnic State University and Stanford University. Due to their low cost, CubeSats have gained popularity among universities and industry for prototype development or for small science missions. The Orbital System for the Investigation of the Response of the Ionosphere to Stimulation and Space Weather (OSIRIS-3U) is a CubeSat mission in development by the Student Space Programs Laboratory (SSPL), a faculty-directed, student-run laboratory at The Pennsylvania State University. The pLP requirements are derived from the OSIRIS-3U mission and ensure the instrument is compatible with small satellites of CubeSat size and larger. The concept is expected to provide a low-cost, diverse instrument for the small satellite community.
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Chapter 1

INTRODUCTION

SPACE: THE FINAL FRONTIER.
—STAR TREK NARRATIVE [1]

Star Trek provided an outlet of imagination to countless children and adults, but its fictitious creations were sometimes startlingly accurate. Magnetic storms in the Star Trek universe may send the crew to a mirror universe, though they more often cause unwanted power surges in the magnetic shields or disrupt communications. Unfortunately, similar space weather events also plague Earth’s satellites and power grids. Geomagnetic storms can induce large currents into power grids and destroy transformers, resulting in widespread blackouts such as the 1989 Quebec disturbance [2], and satellites must deal with the threat of energetic particles.

As society’s infrastructure grows more complex and dependent on space systems, such as GPS and communication satellites, it also becomes more vulnerable to space weather effects. Research into space weather and heliophysics is necessary in order to address this vulnerability. Understanding the physical processes involved in weather events can lead to forecasting, mitigation techniques, and emergency plans that provide a more reliable infrastructure.

1.1 Overview

Undergraduate and graduate students are developing a CubeSat mission in the Student Space Programs Laboratory at The Pennsylvania State University in order to investigate space weather. The OSIRIS-3U (Orbital System for Investigating the Response of the Ionosphere to
Stimulation and space weather) mission will primarily investigate artificial space weather events in order to study the ionosphere’s response to natural phenomena such as coronal mass ejections. Ionospheric heaters, such as those found at HAARP, EISCAT, and Arecibo, are high-frequency (HF) band transmitters that are capable of modulating the ionosphere through direct heating and other processes. An in situ characterization of the heated region at high spatial resolution will provide entirely new data to the ionospheric sciences community. These data will further our understanding of space weather events and radio-wave interaction with the ionosphere, as well as improve current ionospheric models.

A pulsed Langmuir Probe (pLP) is developed to fulfill this need. The pLP is a plasma diagnostics instrument based upon Irving Langmuir’s probe theory. Traditional Langmuir probes are plagued by contamination effects, which results in inaccurate data. Pulsed operation, meets the low power and data rate requirements ideal for small satellites.

1.2 Contributions

This thesis covers the design and implementation of a proof-of-concept pulsed Langmuir probe (pLP) for use in ground chamber testing and onboard satellites. The pLP is designed for small satellites in the pico-satellite and nano-satellite sizes. The instrument is designed to provide low-cost, high-quality data return for these small satellites. The performance of the instrumentation is verified through simulation and partially through testing.

1.3 Thesis Organization

This thesis covers the design and implementation of the pLP by first providing a brief introduction to plasma and ionospheric fundamentals, Langmuir probe theory, and probe
Contamination in Chapter 2. This background prepares the reader for the instrument development section that relies on theory to derive instrument requirements.

Design, simulation, and preliminary test results are covered in Chapters 3 and 4. The pLP is separated into two primary subsystems: the electrometer, responsible for probe operation, and the control board that handles signal conditioning, digital-to-analog and analog-to-digital functions, logic, power regulation, and interfacing.

Chapter 5 concludes with a summary of contributions and future work required to complete the pLP.
Chapter 2

BACKGROUND

This chapter begins with an overview of plasmas and Langmuir probe theory from which the instrument requirements are derived. This is followed by an introduction to probe contamination and pulsed Langmuir probe theory.

2.1 Space Plasmas

Much of the material universe is comprised of plasma, often referred to as the fourth state of matter. While not as common on Earth, plasma comprises over 99% of ordinary matter [3]. A recognizable manifestation is our Solar System’s Sun, but plasma can be found throughout space, in Earth’s atmosphere, and in small quantities on the surface of the Earth. This thesis will focus on plasmas found in the near-Earth region of space.

2.1.1 Plasma Fundamentals

Plasma can be described as an electrically conductive gas caused by the presence of charged particles. These charged particles are in the form of ions and electrons created by ionization processes. In large volumes such as the ionosphere, plasma exhibits quasi-neutrality and collective behavior. Before continuing, it is necessary to define both quasi-neutrality and collective behavior.
Quasi-neutrality is the property of having locally charged regions while maintaining zero net charge over a sufficiently large volume. That is, the number density of negative and positive charge carriers is approximately equal within the entire volume of plasma, but small areas may develop a net charge and establish electric fields.

Electromagnetics and collisions can both govern the plasma’s behavior. Electromagnetic coupling between the charged particles allows for groups of ions and electrons to act as dynamic entities, known as collective behavior. It is necessary that the mean free path of the particles is large enough such that collisions do not dominate particle interactions, allowing long-range Coulomb forces to be significant. This behavior allows for complex phenomena such as plasma waves and has led to theories such as magnetohydrodynamics and kinetic theory.

2.1.1.1 Sheath Formation

Shielding is a necessary concept for understanding probe theory. First, consider the interaction between plasma and two spheres connected through a battery. Particles of opposite charge would be attracted to the spheres, forming a cloud of ions around the negatively charged sphere and a cloud of electrons around the positively charged sphere. Note that the assumption of no negative ions is made. The result is shown in Figure 1, where the accumulated charge in each cloud is equal and opposite of the charge within their respective spheres. The edge of the cloud occurs at the distance from the sphere where the thermal energy of the charged particles is sufficient to break free of the sphere’s reduced electric field. The thickness can be approximated by the Debye length, a characteristic length of the plasma that represents where the potential has decayed by $e^{-1}$ (to approximately 37% of its initial value).

In the one-dimensional case, the Debye length is found to be
\[
\lambda_D = \left( \frac{\varepsilon_0 K T_e}{n e^2} \right)^{1/2},
\]

where \(K T_e\) is the thermal energy of the particle, \(n\) is the charged particle number density, \(\varepsilon_0\) is the permittivity of free space, and \(e\) is the charge of an electron. Rigorous derivations of the Debye length are available in texts and lectures such as Chen [4].

Figure 1: Debye shielding of two charged spheres immersed in plasma, connected to a battery [4].

The generalized form of a Debye shield is known as a sheath, coined in Irving Langmuir’s 1923 paper on ion shielding [5]. At the boundary between the charge cloud and plasma, electrons escape faster than ions due to the electrons’ higher thermal velocity. This leaves behind a net positive charge, forming an electric field from the boundary into the plasma. The sheath’s role is to electrostatically contain the escaping electrons and it can span several Debye lengths in thickness [4]. A pre-sheath area is also formed that acts as a transition layer between the sheath and ambient plasma.
2.1.1.2 Plasma Criteria

With Debye shielding defined, it is possible to provide Chen’s [4] three criteria for a plasma:

1. The Debye length must be much less than the length, or size, of the system such that there is undisturbed plasma.
2. The number of charged particles in the sheath must be much greater than one in order to shield.
3. The plasma oscillation frequency must be greater than the collisional frequency of the atoms and/or molecules.

2.1.2 The Earth’s Ionosphere

Before covering the ionosphere, it is beneficial to review the conventions used to describe the layers of Earth’s atmosphere. The atmosphere is most commonly separated by temperature inflection points; however, it may also be described by its ionization. Note that these two methods run in parallel and therefore it is possible to be in both the thermosphere and ionosphere simultaneously. Figure 2 shows the atmospheric naming conventions side-by-side.
Figure 2: Vertical profile of Earth’s atmosphere [6].

The ionosphere is the region of Earth’s atmosphere that is composed of electrically-conductive plasma, present from about 60 km to 1000 km. Photoionization, primarily from extreme ultraviolet (EUV) and X-ray radiation from the Sun and impact ionization from the solar wind are the dominant processes in producing ionospheric plasma. While the ionosphere is generally called a plasma, its composition also contains a large concentration of neutral particles (i.e., no charge) and is sometimes referred to as a weak or partially ionized plasma.

Within the ionosphere are diurnal layers with properties that change between daytime and night time. During the night, the ionosphere is dominated by only the E and F regions, while the daytime ionosphere features the D, E, F1, and F2 layers due to the influence of the Sun. Figure 3 plots example profiles of the daytime and nighttime ionosphere that show more distinct layers and an increased amount of ionization during the daytime. The increased ionization is the cause of the increase in electron number density.
The ionosphere is host to several space weather phenomena. Due to the conductive nature of the ionosphere, many of these phenomena involve electrical currents and discharges. Examples include geomagnetic storms, red sprites, and blue jets. Other events, such as aurora, are caused by the recombination or collision of charged particles.

2.1.3 Technologies Utilizing Plasmas

Plasmas play a critical role in electric propulsion, electrodynamic tethers, and spacecraft charging systems. However, plasmas find their way into many industries beyond space. Plasma
cutters, cleaners, microelectronic etching, and fluorescent lamps are all examples of plasma on Earth.

Communication methods can take advantage of the plasma in Earth’s ionosphere. Plasma has a refractive index based on the electron number density, which causes radio wave reflection above a certain band of frequencies (usually the HF band). This allows the “bouncing” of waves off the ionosphere, allowing for long-distance communication without the use of satellites.

### 2.2 Langmuir Probe Theory

A well-known and prevalent electrostatic probe for determining plasma characteristics is the Langmuir probe, introduced by Irving Langmuir in 1926 [7]. There are two probe-geometry dependent theories depending on probe size, \( r \), with respect to sheath size, \( r_s \) (or, alternatively, Debye length): orbital-motion-limited (OML) theory for \( r_s \gg r \) and the Child–Langmuir law for \( r \gg r_s \). This application employs OML theory and thus we do not cover the Child–Langmuir law herein.

#### 2.2.1 Orbital Motion Limited Theory

The orbital-motion-limited probe theory pertains to the cylindrical geometry used for the OSIRIS-3U probe, designed by Adam Escobar for use on the ESPRIT sounding rocket mission [8]. OML theory is restricted to applications for which the probe radius is much less than the Debye length of the plasma.
2.2.2 Instrument Operation

The Langmuir probe operates by applying a potential to a conductor immersed in plasma. The conductor then collects ions and electrons, resulting in a current between the spacecraft and plasma (i.e., the plasma can both sink and source current with respect to the spacecraft). It is therefore commonly called the collector and it sustains bidirectional current flow. A current-versus-voltage plot, known as an I–V curve, can be found by sweeping the applied potential and can be used to extract information about the plasma. An example I–V curve is shown in Figure 4. The curve is separated into three regions: (1) the ion saturation region, where the only current contribution is from ions, (2) the electron retardation region, where electron collection increases, and (3) the electron saturation region, where electron collection dominates. Note that there is a current contribution from ions throughout the electron retardation and energetic or positively charged ions can contribute current in the electron saturation region.

![Figure 4: The current to voltage relationship for a cylindrical probe [8].](image)
The following is a list and explanation of parameters of interest:

- **Floating Potential**: The floating potential is defined as the potential at which there is no net current flow between the spacecraft and plasma, expressed in volts (V).
- **Plasma Potential**: The potential found in the area between charged particles, expressed in volts (V).
- **Electron and Ion Temperatures**: The thermal energy of the charged particles, expressed in units of electron-volts (eV).
- **Electron and Ion Densities**: A misnomer for the number density, or concentration, of electrons or ions. This is typically expressed as the number of molecules per cubic meter or cubic centimeter (m$^{-3}$ or cm$^{-3}$).

Using the I–V curve from the Langmuir probe sweep, all parameters except the ion temperature can be determined.

### 2.3 Probe Contamination

When a probe is exposed to gasses, it is inevitable that there will be an accumulation of particles on the collector surface. The accumulation can also be caused due to materials outgassing from the spacecraft or a dirty probe upon launch. This is known as contamination and results in a contaminant layer that changes the characteristics of the probe, thus skewing measurements. The effects of and methods for addressing contamination are discussed in this section.

#### 2.3.1 Contamination Behavior

Equivalent models offer an accurate and clear method of understanding contamination. The contaminant layer acts as a resistor–capacitor network in series between the plasma and probe. The capacitance introduces hysteresis, a dependence on previous states of the system. This means the system is no longer memory-less and the collected current depends on the path taken.
Figure 5 shows the equivalent model and the resulting hysteresis. Figure 6 shows data from a laboratory setting. Note the difference in Figure 6 between the up/down sweeps and the ideal sweep (solid line), which would yield significantly different plasma parameters.

A critical aspect of the equivalent model is the contaminant layer’s $RC$ time constant. This represents the charge/discharge rate of the voltage across the contaminant layer and comes into play when using mitigation techniques such as high frequency waveforms or pulsed methods. Formulaically, the time constant is $\tau = RC$.

![Figure 5: (a) Effective circuit equivalent model for surface contamination. (b) Hysteresis effects in conventional Langmuir probe current–voltage characteristic resulting from layering of surface contaminants [9].](image-url)
2.3.2 Mitigation Techniques

Besides the pulsed method covered below, a few options are available to mitigate contamination effects. These techniques have, at minimum, been proven in laboratory settings.

2.3.3.1 Correction Algorithms

Through the Oyama contamination model [11], Piel [10] found it possible to determine the contaminant layer’s resistance and capacitance. These can be used to determine the behavior of a clean probe using a correction algorithm. This method is more intense for data analysis and restricts the electron collection regime to within a certain potential range. It was developed specifically for spherical probes and has been test proven on the DEOS rocket campaign [10].
2.3.3.2 Probe Cleaning

A common method to address contamination is through frequent probe cleaning. The cleaning may be done by heating the probe collector or by applying a large potential. The first method, heating, requires a large amount of power to heat the collector and must be done frequently. Therefore, it is not ideal for closing a small satellite’s power budget and requires operational time beyond taking measurements or data analysis. In addition, materials must be able to withstand the high temperatures of the collector. Instead of heating, a large potential can be applied to induce ion or electron bombardment. A sufficiently negative bias (e.g., −150 V) can accelerate ions toward the probe collector, resulting in collisions that knock off the contaminants. High voltage circuitry is required for ion bombardment, which demands more board space and electromagnetic interference requirements.

2.3.3.3 High Frequency Waveforms

High frequency sweeps can also be used to remove contamination effects. It is useful to review the concept of impedance for this method. Impedance is a measure of a circuit’s opposition to current expressed as

\[ Z = \frac{V}{I} = \frac{\text{voltage}}{\text{current}} = R + jX, \tag{2} \]

where \( Z \) is a complex impedance of resistance \( R \) and reactance \( X \), which generalizes Ohm’s Law to include AC circuits. Ideal capacitors have only the reactive, or imaginary, impedance, i.e.,

\[ Z_C = \frac{1}{j\omega C}. \tag{3} \]

This impedance has frequency dependence due to the angular frequency, \( \omega \), in the denominator. As the frequency of an applied signal increases, the impedance lowers and the capacitor begins to behave similar to a short circuit. Hence, we may make use of this property to minimize the
contaminant layer’s capacitive effects by applying voltage sweeps at higher frequencies. However, this method requires the sweep period to be much less than the $RC$ time constant of the contaminant layer. The pulsed plasma probe detailed in Section 3 is capable of, but not designed for, this operation.

### 2.4 Pulsed Langmuir Probes

Probe contamination, discussed in Section 2.2.2, behaves like a resistor–capacitor element in the system’s circuit-equivalent model. In order to mitigate the capacitive effects of the contaminant layer, the pulsed plasma probe (P$^3$) was introduced by Szuzczewicz and Holmes [9] of the Naval Research Laboratory.

#### 2.4.1 Theory

The pulsed method is best explained using time constants. By making the pulse length, $\tau_{\text{on}}$, much less than the contaminant layer’s $RC$ time constant, $\tau$, no significant voltage is created across the capacitor. In other words, the technique attempts to keep a constant voltage drop across the contaminant layer, which prevents hysteresis effects. A circuit description is possible using Figure 5. Since the capacitor resists a change in voltage, the voltage drop across the contaminant layer is approximately zero and almost the entirety of the voltage drop occurs across the sheath resistance. Contrasting with the high-frequency sweeps described in Section 2.2.3, for which the period of the sweep must be less than the contaminant layer time constant, the pulsed technique requires $\tau_{\text{on}} \ll \tau$ and $\tau_{\text{off}}$ sufficiently large to allow full discharge.
2.4.2 Operation

There are two primary methods of creating pulses. Early iterations of the pulsed plasma probe used a combed triangle wave (i.e., the voltage continues to ramp during the pulse) as seen in Figure 7. Recent laboratory implementations use a fixed voltage for each pulse. The difference in technique is shown in Figure 8. The designed plasma probe, described in Chapter 3, is capable of both waveforms at a higher frequency than previous designs. The operation can be further customized by varying the duty cycle, frequency, and basis waveform (i.e., sine, triangle, or sawtooth).

Figure 7: Continuous and modulated sweep modes of Langmuir probe operation: (a) represents the conventional approach while (b) schematically represents the procedure of the P3 technique. Note that every 5th pulse is omitted for current monitoring purposes [9].
2.4.3 Documented Experiments

The pulsed technique has significant heritage in sounding rocket and satellite missions throughout the 1970s and 1980s. The P$^3$ instrument was used on several missions including a Terrier–Malemute sounding rocket [12], a Nike–Tomahawk sounding rocket [13], and an Aerobee reentry mission [14]. Little has been done using the probe since the 1980s, despite its documented benefits, until the technique reemerged in the late 2000s by Oyama [15].
Chapter 3

PULSED LANGMUIR PROBE DESIGN

This chapter details the requirements, design, and implementation of the pLP. A simplified block diagram of a Langmuir probe is shown in Figure 9. The circuitry block is the focus of this thesis and is discussed as two separate subsystems: the electrometer and the control board.

Figure 9: Block diagram of Langmuir probe.

3.1 Design Specifications

Engineering requirements must be laid out before beginning any design. These requirements are derived from a variety of sources including electronics standards, system I/O, and operating conditions. They span volume and power constraints, sampling and data rates, and minimum and maximum resolvable currents, among others. This section defines the pLP engineering requirements and their origins.

3.1.1 CubeSat Standards

CubeSats are nano-satellites designed to meet the standard developed by California Polytechnic State University and Stanford University in 1999. The standard was quickly adopted
by both industry and university programs for launching small scientific payloads because it minimizes developmental work on systems such as launchers (e.g., the Poly-PicoSatellite Orbital Deployer, or P-POD). CubeSats under this standard can consist of one to three units in order to be compatible with the P-POD system. Each unit measures 10 × 10 × 10 cm (approximately 3.9 × 3.9 × 3.9 inches) and must have a mass under 1.33 kg (2.93 lbs.).

The OSIRIS-3U is a 3U CubeSat. One unit is dedicated to science instruments including a tomography beacon and the pLP with associated boom. The beacon dimensions are defined by NRL and the OSIRIS-3U internal structure has been defined by the SSPL structures subsystem. Information regarding a proposed boom design can be found in Friedenberger [16]. These conditions drive the pLP to dimensions of less than 1.8 × 3.5 × 3.5 inches, including its RF box. (Note: United States customary units are used here to remain consistent with the board design that uses mils.) The board height of 1.8 inches allows for free space in the unit for mounting and cable routing purposes.

No specific power requirements are set forth by OSIRIS-3U due to the low duty-cycle of the instrument. However, it stands to reason that the instrument may be operated for longer periods of time by reducing power consumption and therefore it is desirable to pursue a low-power design. This comes secondary to the minimum performance requirements of the pLP, covered in Section 3.1.3.

3.1.2 Current Collection from Plasma Environment

An estimate of the collected current can be found given the probe geometry and an application of OML theory. This estimated current is used to define the dynamic range of the current sensor designed in Section 3.2.
The probe is a cylindrical collector with guard collectors on both sides, as in Figure 10.

The guards are biased to the same potential as the collector, ensuring that the electric field lines are perpendicular to the collector and thus preventing errors due to fringing fields. This probe design is meant for OML theory and is described in an M.S. thesis by Escobar [8].

![Figure 10: Cylindrical Langmuir probe with double guards.](image)

The current relationship, derived in Mott–Smith and Langmuir [7], is

\[
I_e = A n_e q \frac{2}{\sqrt{\pi}} \sqrt{\frac{qV}{2\pi m_e}} \tag{4}
\]

for electrons and

\[
I_i = A n_i q v_i \frac{1}{\sqrt{\pi}} \sqrt{\frac{1 + \frac{kT_i}{m_i v_i^2}}{m_i v_i^2} + \frac{2qV}{m_i v_i^2}} \tag{5}
\]

for ion collection, where:

- \( A \) is the surface area of the probe,
- \( q \) is a unit charge,
- \( n_x \) is the particle number density,
- \( v_x \) is the particle velocity with respect to the spacecraft,
- \( T_i \) is the particle temperature,
- \( m_i \) is the particle mass, and
- \( V \) is the applied potential with respect to the plasma potential.

Since Escobar’s design was intended for a sounding rocket mission, new probe dimensions were found using the above equations for a CubeSat operating in the F-region of the ionosphere. Table 1 lists the parameters used to find discernable current, along with the solution found using equation (4) above. A few assumptions were made. First, the ion velocity, \( v_i \), is
approximately equal to the spacecraft velocity. The ion mass, $m_i$, was found by finding the weighted mean of the dominant ion species in the F-region of the atmosphere (i.e., N$^+$ and O$^+$).

Furthermore, low ion temperatures result in the velocity term dominating current collection and thus can be neglected. Since the upper F-region decreases in ion number density, a minimum density of $10^9$ m$^{-3}$ is used. Finally, the boom design limits the entire probe length (including the collector and guards) to 5 cm.

### Table 1: Minimum Current Collection Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$r$, probe radius</td>
<td>0.3175 cm</td>
</tr>
<tr>
<td>$L_C$, collector length</td>
<td>2 cm</td>
</tr>
<tr>
<td>$L_G$, guard lengths</td>
<td>1.5 cm</td>
</tr>
<tr>
<td>$v_i \approx v_{\text{spacecraft}}$, ion velocity</td>
<td>7.5 km/s</td>
</tr>
<tr>
<td>$m_i$, average ion mass</td>
<td>$2.4 \times 10^{-26}$ kg</td>
</tr>
<tr>
<td>$n_i$, ion number density</td>
<td>$10^9$ m$^{-3}$</td>
</tr>
<tr>
<td>$V$, potential w.r.t. plasma potential</td>
<td>0 V</td>
</tr>
<tr>
<td>$I_i$, current collected</td>
<td>271 pA</td>
</tr>
</tbody>
</table>

With a 2-cm collector, a minimum collected current of 271 pA is expected. Electric field modeling is required to determine the optimum guard-to-collector ratio for this probe length; therefore, 100 pA was chosen as the minimum discernible current to allow for a shorter collector to be used.

A similar process was used to determine the maximum current collected; however, the maximum current collected is found in the electron saturation region while using plasma parameters representative of the F-region peak. Table 2 details the values used in calculating the maximum current collected. The required range of the electrometer can now be defined using the minimum and maximum currents and is ±100 pA to ±100 μA.
Table 2: Maximum Current Collection Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$r$, probe radius</td>
<td>0.3175 cm</td>
</tr>
<tr>
<td>$L_C$, collector length</td>
<td>2 cm</td>
</tr>
<tr>
<td>$L_{Gr}$, guard lengths</td>
<td>1.5 cm</td>
</tr>
<tr>
<td>$n_e$, electron number density</td>
<td>$10^{12}$ m$^{-3}$</td>
</tr>
<tr>
<td>$V$, potential w.r.t. plasma potential</td>
<td>+5 V</td>
</tr>
<tr>
<td>$I_e$, current collected</td>
<td>34.1 $\mu$A</td>
</tr>
</tbody>
</table>

3.1.3 Performance Requirements

When using a pulsed method, the length of the pulse is dependent on the contaminant layer’s $RC$ time constant as well as hardware limitations. A ratio of 1:20 for on-to-off time may work well with 1-kHz pulses (i.e., $\tau_{on} + \tau_{off} = 1$ ms), but has limited spatial resolution when used on a LEO satellite orbiting at 7 km/s. However, more power and board space are required to achieve faster operation. Furthermore, faster sweep rates may require fewer data points per sweep, increasing error during data analysis. Therefore, there is a compromise between the spatial resolution, plasma parameter accuracy, and system requirements.

Defined requirements are as follows: (1) data is output at maximum 115,200 baud over UART and (2) the instrument must be able to provide sub-10-meter resolution for electron density.

The data rate requirement severely limits the sweep rate unless data storage is on the pLP. However, a major advantage of high frequency pulsing is that the sweeps are localized. If a sweep can be completed at a 1-kHz rate then sub-10-meter accuracy can be achieved, while longer sweeps may span nearly a kilometer of space. A further benefit is seen when switching between swept- and fixed-bias operation. Fixed-bias Langmuir probes can determine changes in the electron density, known as relative electron density, and therefore can be used to acquire pseudo-
absolute measurements by first obtaining the absolute electron density through a sweep. This
method can achieve higher resolutions and provide corrections to the absolute electron density
more often by having a high frequency sweep.

The voltage sweeps can be done from −10 to +10 V. This range can be narrowed to
reduce the number of samples per sweep, but acts as the upper bound for system requirements.
The ADC resolution is dependent on the electrometer and will be discussed in Section 3.3.2.

With these considerations, the pLP is designed for 1-MHz operation. This allows for data
averaging through the use of digital filters, increasing data resolution, or for an increased number
of voltage steps for more data points along the I–V curve.

### 3.2 Electrometer

The electrometer is the circuitry responsible for setting the probe potential and converts
collected current into a measureable signal. It must sense currents between ±100 pA to ±100 μA,
a span of six decades, as shown in Section 3.1.2. Linear conversion would severely limit the
resolution at the lower currents, so a logarithmic current-to-voltage transducer was used.

#### 3.2.2 Theory of Operation

It is best to describe the circuit by tracing the signal paths chronologically, using the
schematic in Figure 11. A voltage, called the probe bias, is applied first to the non-inverting
terminal of the op-amp. Ideally, the inverting terminal of the op-amp and, thus, the probe
collector, is then set at the same potential. Due to the applied voltage, a current will flow between
the ionosphere and probe. In the ideal op-amp, this current will flow only through the diodes in
the feedback loop. The forward voltage drop across the diodes then is logarithmically related to
the current flowing through the diodes, which results in a voltage added or subtracted to the probe bias. A following in-amp stage removes the probe bias to leave only the voltage across the diodes. From this voltage, the current placed through the diodes can be backed out by comparing it to calibration data.

![Schematic of electrometer current sense circuitry.](image)

**Figure 11:** Schematic of electrometer current sense circuitry.

### 3.2.3 Implementation

Several design considerations were made when choosing components. Previous designs at The Pennsylvania State University used low bias current diodes and a Burr–Brown precision op-amp that are no longer in production. Therefore, new components were selected to ensure parts availability for future missions.

Two critical specifications for op-amp selection were the input bias current and offset current. When dealing with currents on the order of 100 pA, a large input bias current can dominate the measurements without compensation, even more so with a noisy amplifier. The ideal case assumes no voltage across the op-amp input terminals; however, they will be separated by an offset voltage in practice. Hence, offset voltage also must be considered. The selected op-
amp is the ADA4627, a precision amplifier by Analog Devices. It features low voltage noise, offset drift, and a low input bias current of 5 pA, making it a suitable option for this application.

Two bipolar junction transistors (BJT) were diode-connected in place of the diodes. The BJT component, the MMPQ3904, is a quad-pack for the purpose of thermal stabilization. To prevent base-to-emitter voltage fluctuations with temperature, the thermal feedback loop seen in Figure 12 was created using the two spare BJTs in the quad-pack, drawing inspiration from an application circuit by Williams [17]. The base and load (emitter) resistors were chosen using parameters sweeps, shown in Figure 13 and Figure 14, to maximize the power delivered to the BJT while minimizing the dissipation in the load resistor. The MATLAB file for the parameter sweeps can be found in Appendix A.

Figure 12: Thermal regulation schematic.
Figure 13: Parameter sweep showing the power dissipated in the load resistor of the heating circuitry.

Figure 14: Parameter sweep showing the power dissipated in the BJT of the heating circuitry (note that this is not the BJT used for the reference voltage).
The non-inverting terminal of the op-amp is brought out as a guard trace for any traces connected to the inverting terminal. This prevents PCB leakage currents, which may be on the order of nanoamperes, from offsetting the measured current.

The instrumentation amplifier, or in-amp, is the AD8220. The device has approximately 1.2 MHz of bandwidth at unity gain and a low input bias current. Component pads for an RFI filter at the input of the in-amp are included so that a filter may be added at a later time. The filter performs both differential and common mode filtering. Labeling the shunt capacitors as $C_D$, the center capacitor as $C_C$, and the pin capacitance as $C_G$, the filter cut-off frequencies are

$$f_c^{\text{Diff}} = \frac{1}{2\pi R(2C_D + C_C + C_G)},$$

$$f_c^{\text{Com}} = \frac{1}{2\pi R(C_D + C_G)}.$$

Mismatch in the shunt capacitors can lead to a common-mode signal being seen as a differential. Therefore, the differential cut-off frequency should be less than the common-mode to address this problem.

Two low-bias-current electromechanical relays from Teledyne provide switching between the Langmuir probe and a set of two calibration resistors. These relays are switched using MOSFET drivers that receive signals from the control board. The two resistors are used for calibration by using a calibrated voltage source as the probe bias, creating a known current through the electrometer. Testing results are included in Chapter 4.

### 3.3 Control Board

Operating the Langmuir probe and electrometer requires circuitry to provide the probe bias, to perform data acquisition, and to communicate with external systems. The control board is
responsible for the regulation, logic, and data conversion required for these tasks. In Figure 15, the control board has been broken down further to show the signal connections within the pLP.

Figure 15: Control Board block diagram. Note that power connections are not shown except for the voltage regulator inputs.

3.3.1 Command and Data Handling

Command and Data Handling (CDH) subsystem consists of the FPGA and system I/O circuitry. This includes the interfaces to memory, all components requiring communication, and external systems.

3.3.1.1 FPGA

A Xilinx Spartan 6 LX-9 is used for control and data handling. It offers 102 general-purpose input–output (GPIO) pins, which are used for parallel and serial communications, programming, and debugging. The high pin count is required due to parallel communication needing a dedicated pin for each bit (e.g., a 14-bit ADC would use 14 GPIO pins for data). The
LQFP package was chosen to allow in-house population of the components, as SSPL does not have the facilities to solder ball-grid arrays (BGA).

The Spartan 6 is configured each time upon start-up by accessing an external SPI NOR-flash IC, the Numonyx M25P. The flash memory is non-volatile and stores up to 8 Mb of data, which provides a large margin over the approximately 2-Mb maximum configuration bits required for the LX-9 series. This flash memory is supported by the Xilinx ISE for indirect programming, which allows us to program it through the FPGA using the standard JTAG programmer.

The control board’s interface allows it to be integrated with a flat-sat bus and used in ground testing with a vacuum chamber. The FPGA uses a software-implemented UART for connections, but may also use UART-to-USB. USB functionality is detailed in the debug section since it is omitted for flight models.

3.3.1.2 Clocking

Many integrated circuits, such as an FPGA, rely on accurate clocking for operation and data transfer. In this application, any clock signals required for peripheral devices are synthesized using the FPGA’s internal Digital Clock Managers (DCM), thereby decreasing the number of oscillators on the control board. In addition, common frequencies can then be chosen, which are available at lower cost and lead time.

The primary oscillator, the TDO4050, is a 20.0-MHz temperature-compensated voltage-controlled crystal oscillator (TCVCXO) from Pletronics. Temperature compensation was chosen over oven controlled to reduce package size and power consumption. A CMOS clock is made by putting the oscillator’s clipped-sine-wave output through a logic inverter. The clock is then input
to a global clock line on the FPGA. Although the inverter output may not be a 50% duty cycle square wave, it is not an issue because the FPGA will only use the rising edge of the input clock.

### 3.3.1.3 Programming

Figure 16 shows a simplified internal block diagram of the FPGA, as designed for pLP operation. Debugging sections are not shown within the diagram. The configuration section (dashed lines) contains the JTAG and memory that are responsible for creating the other blocks; hence, they are not connected on the diagram.

The code will be implemented using a top-level schematic containing VHDL and schematic modules. Programming is done using Xilinx ISE, which ensures compatibility with the Spartan 6 and allows indirect programming of the SPI flash memory. Data is output as ASCII-encoded binary to reduce UART throughput requirements. A first-in-first-out (FIFO) buffer will be included before the UART core to allow for high-data-rate operation for short periods of time.

The averaging block calculates the mean of a set number of samples by dividing the output of an accumulator controlled by the decision logic block. Note that this is not a moving or running average. In addition, a look-up table must be used to provide the necessary DAC codes for each sweep.

Spartan 6 FPGAs contain two DCM blocks, which each consist of a phase-locked loop (PLL) and two delay-locked loops (DLL). The global input clock is routed to a PLL and output to the two DLL blocks to perform multiple/divide functions and ensure the clocks are in phase. These synthesized clocks are then routed to peripheral I/O and internal logic.
3.3.2 Sampling

The sampling section of the control board is responsible for the signal conditioning and analog-to-digital conversion of the electrometer’s output signal. Due to the logarithmic conversion of the electrometer, it is likely that less than half of the 2-V input range will contain useful information. For example, the measured voltage across a diode-connected BJT may span between 300 to 700 mV in the operational range. Furthermore, any error in voltage measurement is amplified when finding current. The exact current resolution and error can be determined through testing the BJTs, but a 14-bit ADC and DAC are used to ensure the necessary resolution.
while accounting for the converters’ integral and differential nonlinearity. Removal of the LSB can be done in the FPGA to reduce throughput requirements.

The first stage is a level shifter that converts the electrometer’s output to a +1 to +3-V signal. This stage also acts as an anti-aliasing filter, which outputs the signal to be sampled by the ADC. A single op-amp, the Texas Instruments THS4071, is used as a level shifter, buffer, and anti-aliasing filter. The ADC chosen is the Analog Devices AD9244, a 14-bit 40-MSPS ADC with parallel data output. The device is pin compatible with a 65-MSPS version; however, the 40-MSPS device was chosen to minimize cost. The devices may be swapped at a later date if higher sampling rates are desired. The front-end configuration is for a 2-V peak-to-peak signal at a common-mode voltage of +2 V, resulting in the +1 to +3-V input range. The electrometer output of −1 to +1 V therefore is shifted to +1 to +3 V, the ADC’s input voltage range. A low-pass filter is included to limit wide-band noise.

3.3.3 Arbitrary Waveform Generation

The AWG subsystem is centered on the Texas Instruments THS5671A, a 14-bit, 125-MSPS DAC. The DAC input accepts parallel data and outputs a differential current output. The output current is placed through 50-Ω shunt resistors to create a differential voltage. A difference amplifier then creates a single-ended voltage output. The difference amplifier was created using the Texas Instruments THS4082, chosen for its high bandwidth and slew rate. The amplifiers can create a range of voltages of just under ±15 V; however, the output only needs to provide ±10 V to the electrometer. This keeps the amplifier well within linear operating conditions and prevents clipping. The second op-amp, the THS4082, is used to buffer the voltage output before going to the electrometer.
3.3.4 Power

The board receives external power of +5.5 V and ±15 V. Component selection was done to limit the number of supply voltages required. The resulting design has three low-dropout (LDO) regulators.

The +5.5-V rail is sent to LDO regulators to create +5-V, +3.3-V, and +1.2-V digital supply voltages. These power the CDH and Debug subsystems of the board. The power is then passed through a ferrite bead and shunt capacitors before going to the analog circuitry. This helps prevent high frequency noise from coupling between the sensitive analog components and switching logic.

The ±15-V supply is used to power the op-amps and the electrometer. These rails are already regulated before entering the board, but bulk decoupling capacitors are placed at the connector and care is taken when selecting bypass capacitors for the components.

Bypass capacitors were selected to provide low impedance over multiple harmonics of the operating frequencies. The capacitors are TDK Corporation ceramic capacitors at 330 pF, 0.1 μF, and 10 μF. Dedicated 330-pF and 0.1-μF capacitors are placed as close as possible to the component pins to limit trace inductance, while the larger 10-μF capacitors are shared between multiple pins. Figure 17 shows the total impedance of the capacitors in parallel. An impedance of less than 1 Ω is achieved between 20 kHz to 1 GHz, covering through the 20th harmonic of the peripheral device I/O clocks that run at 40 MHz.
3.3.5 Debug

A series of LEDs and a breadboard section are included on the control board. These are connected to GPIO pins of the FPGA for troubleshooting as well as rapid prototyping.

One set of UART lines is broken out into a 100-mil header for flying leads and second set interfaces with an FTDI USB-to-UART bridge, which provides USB 2.0 Full-Speed support (up to 12 Mbps). The USB capability was included with the expectation that a personal computer would handle the command and data handling for vacuum chamber testing, as shown in Figure 18, in place of the satellite bus. This feature makes the control board compatible with a larger range of systems.
Figure 18: Connection diagram of the pLP being used in a ground-test set up.

3.4 Schematic and Layout

The schematic was created as a two-tier design in Altium Circuit Designer. The top layer, shown in Figure 19, is the first tier and shows connections between the more detailed schematics. The second tier consists of the following eight schematics:

1. FPGA I/O
2. FPGA Power
3. Sampling
4. Waveform Generation
5. Power
6. Debug (LEDs and breadboard)
7. Communications (UART-to-USB functionality)
8. Electrometer
Figure 19: Screenshot of top-layer schematic in Altium Circuit Designer.

After the schematic was created, it was reviewed by student members of SSPL and by faculty. A list of action items and suggestions were used to improve the schematic before continuing onto layout. Full schematics are found in Appendix B.

A four-layer PCB layout was created in Altium using the pLP schematics. The four-layer board was possible due to the selection of the LQFP package FPGA. A BGA package would likely require a six-layer board with blind vias, which significantly increase the board’s fabrication cost, complexity, and time spent in testing. The control board, defined by the yellow rectangle in Figure 20, measures 3.4 × 3.2 inches to fit the CubeSat form factor. Area is left in the upper left corner to later integrate the electrometer. The rest of the board is left as space for debugging and includes the USB-to-UART circuitry and breadboard.
The design was again reviewed by students and resulted in changes to the ground plane to improve signal integrity. A slot (seen as green dashed lines in Figure 20) was introduced to route the ±15-V current return paths around the digital logic instead of underneath it. A design rule check was then done to confirm that the board was compliant with the prospective board manufacturer’s specifications. Figure 21 shows a 3D model of the board, with more views in Appendix B. The board design was sent for fabrication in June 2013.
Figure 21: 3D screen capture of the front side in Altium.
Chapter 4

ANALYSIS AND RESULTS

Extensive testing is necessary for characterizing a circuit’s functionality. It is critical that the system performs as expected within operating conditions, which involves circuit functional, environmental, and, often, vibrational testing. This chapter covers the preliminary testing of the pLP used to verify basic functionality.

4.1 Electrometer Simulation and Testing

The electrometer design was first verified using a SPICE simulation during schematic creation. Following board fabrication, the individual components were functionally tested and populated. The current-sensing circuitry was tested, followed by the thermal circuitry, and is currently in plasma chamber testing using a Langmuir probe.

4.1.1 SPICE Modeling

The electrometer output (red trace) shows the logarithmic behavior of the circuit. The simulation yields the expected behavior of the implemented circuit; however, the device parameters are inaccurate without full characterization of the transistors used on each board. The simulation schematic detailing excitations is included in Appendix B.
4.1.2 Current Measurement Testing

It is critical that, for accurate operation over a wide operating range, the electrometer has high linearity. A preliminary test using the electrometer’s calibration resistors and an external calibrated voltage source was done in open air conditions (i.e., the test was conducted on the lab bench without the use of an EMI box). Figure 23 shows the results of the current test. Accuracy of measurements was limited by the calibration source’s accuracy, contributing to the horizontal error bars in Figure 23. The digital multimeter (DMM) used for measuring the output voltage contributes to the vertical error bars, which are covered due to their small size relative to the data point symbols. The semi-log plot shows high linearity over five decades of operation from 100 pA to 10 μA. Higher currents require a second calibration resistor to be used. Nonlinearity is expected to occur at low current levels and begins to appear under 100 pA. Figure 24 provides a curve fit to the linear region of the electrometer’s operating range. The performance is expected to increase when the circuit is placed within an EMI box, as the output voltage fluctuated due to external stimuli (e.g., moisture in the tester’s breath).
Figure 23: Semi-log plot of output voltage versus input current for the electrometer. Nonlinearity appears under 100 pA of current

Figure 24: Operating range of electrometer with curve fit and conversion equations.
Further testing of the electrometer was done to ensure bidirectional current sensing. Since the characteristics of each diode can vary within the die, positive and negative currents will result in different transfer functions, making it necessary to calibrate for both cases. Figure 24 also shows the result of current testing in the negative regime and a comparison between the two transfer functions.

The calibration data is not accurate under all conditions. Characterization was done in a low-humidity environment at room temperature. On a particularly humid day, the non-linearity can extend to almost 1 nA, reducing the linear range of the electrometer. Figure 25 and Figure 26 present common forms of current-generating phenomena that can impact the electrometer’s performance. Testing within a vacuum or with a dry air purge is necessary to remove moisture and board cleaning is required to remove surface residue.

![Current-generating phenomena on printed circuit board](image)

**Figure 25:** Current-generating phenomena on printed circuit board [18].
4.1.3 Thermal Regulation Testing

The thermal regulation of the feedback BJTs indeed regulated the temperature of the BJT used in the thermal control loop; however, it introduced unwanted effects in the current sensing BJTs. While heating, the circuitry uses about 400 mW and maintains the collector–emitter voltage of a transistor to within 1 mV. The regulated BJT voltage can be seen in Figure 27. The issue with the design is that heating causes an increase in the output voltage as seen in Figure 28. The effect is more pronounced at lower voltages, making it probable that it is causing a change in current. If the cause is leakage currents within the die itself, it would correspond to an increase of ~ 2–3 nA in current due to heating.
Figure 27: Voltage across collector and emitter of the reference BJT during regulation.

Figure 28: Electrometer output voltage during thermal regulation.
Two changes were made to address this problem. First, the regulated BJT and heated BJT were switched; that is, the regulated BJT is placed next to the logarithmic-feedback BJTs in order to limit the voltage swing seen by them. This would ideally isolate the feedback diodes more effectively. Second, the current through the regulated BJT was reduced to approximately 10 nA, which lies within the range of the electrometer. The purpose of having low current is that the regulation would then also compensate for leakage current flowing into the regulated BJT.

These changes provided only a 3-mV decrease in the voltage swing seen at the electrometer output. This is an unsatisfactory result and the circuit may be better thermally regulated by potting the area and using a resistive heater.

### 4.1.4 Plasma Chamber Testing

To verify that the electrometer meets design requirements, the electrometer was integrated and tested with a Langmuir probe. A characterization using the Keithley 2410 SourceMeter will be used to compare the current collected.

The electrometer input was connected to a triax cable that was fed into a vacuum chamber. The purpose of the triax is to provide shielding for the center conductor that acts as a current path. The inner shield is the guard to prevent capacitive currents in the cable, whereas the outer shield is grounded to reduce EMI. The triax leads to a gold-plated cylindrical Langmuir probe of the dimensions listed in Section 3.1.2.

Voltage sweeps were applied to the probe using a Keithley 2410 SourceMeter for both linear and pulsed sweeps. Both the applied voltage and electrometer output were measured using the National Instruments MyDAQ, a 16-bit 200-kS/s DAQ. A custom LabVIEW VI sampled the voltages and output the data to comma-separated-value files and can be found in Appendix C.
The plasma environment was created using a magnetic filter plasma source developed by Colorado State University. The source ionizes an argon gas flow and is housed within a cylindrical vacuum chamber approximately 40 inches in length by in 35 inches diameter. Pictures of the operating plasma source and the vacuum chamber can be found Figure 29 respectively.

Due to EMI, the pLP requires Faraday shielding through the use of an RF box or custom housing. Without the RF box or populated RFI filter, a large amount of noise can be seen on the output. Analysis of the I–V curve is left as future work.

![Plasma chamber and plasma source](image)

**Figure 29:** Plasma chamber (left) and plasma source (right) with argon gas flow.

### 4.2 Control Board Simulation

A major concern with board layout is signal integrity. Noise and distortion both modify square waves, which signify digital bits, into a different signal. If the change is drastic enough, an error may occur (i.e., the value read is not the value sent). If signal integrity becomes an issue in a circuit, it may need to operate at slower speeds or it will fail to function entirely. Therefore, the proper layout of the ADC and DAC parallel data lines becomes a primary concern in board layout.
During layout, the data lines were routed such that the other signal traces are kept as far away as possible, and that no signal traces are being driven if they cross underneath. The internal ground plane adds additional isolation from traces on the other side of the board. In addition, sharp corners were avoided to prevent crosstalk (a sharp edge acts as a radiator). A signal integrity model was then performed to validate the board layout.

4.2.1 IBIS Model

I/O Buffer Information Specification (IBIS), introduced by Intel in the early 1990s, is a simulation technique for signal integrity analysis. SPICE analysis is time consuming and adds complexity, especially where component models may not be publicly available due to proprietary IC designs. Therefore, efficient testing instead can be done on the board layout using IBIS to determine problem areas before fabrication. Both the FPGA and ADC have IBIS models available, and a similar Texas Instruments IBIS file for the THS5061 was modified to suit the DAC.

The model analyzes the layout using impedances and an aggressor/victim excitation method for crosstalk, detailing critical information such as overshoot and rise time. Sample results of the IBIS simulation for data lines between the ADC and FPGA can be seen in Figure 30. The results show great signal integrity at and above the intended operating frequencies. Therefore, no change in the initial board layout was needed.
4.2.2 Testing

Currently, the power regulation section, FPGA, clock, and memory have been populated on the control board. The power regulation section is functional without modification and was used to power the electrometer throughout testing. The clock outputs a clipped sine wave that is
put through an inverter to create a CMOS compatible clock with approximately 50% duty cycle.

The inverter output, which acts as a global clock input for the FPGA, is shown in Figure 31.

Further testing of the control board requires the completion of VHDL programs and is detailed in Chapter 5.

![Figure 31: 20-MHz global clock input.](image)
Chapter 5

CONCLUSIONS AND FUTURE WORK

The pLP remains in testing; however, the design yields several useful results:

1. The successful redesign of a low-current electrometer capable of sensing bidirectional current from ±100 pA to ±1 mA. The updated design uses well-supported, in-production parts.
2. Testing showing that direct die heating of the feedback transistors is inadequate for low-current applications.
3. A control board design that can be adapted for signal processing applications requiring a high frequency DAC and ADC.

In order to verify the design, the remaining tasks include:

1. Current sensing while using noisy power rails
2. FPGA code completion
3. ADC functional testing
4. DAC functional testing
5. Level-shifting circuitry functional testing
6. System integration with PC and OSIRIS-3U CDH board
7. Plasma chamber testing analysis

To test the ADC and DAC, the clock synthesis and input/output configuration of the FPGA must be completed. A second revision will then be created to address concerns found in testing. The second revision will be subject to environmental testing, leading to eventual flight qualification testing.

The pLP will be enclosed within a metal case that provides brackets for mounting and shielding from other satellite subsystems. Exact box dimensions are to be defined as more information about the instrument-to-spacecraft mounting is provided.
% Calculations for Thermal Control Circuitry using Quad-pack BJT
% Timothy R. Brubaker
% SSPL
% October, 2012
% This program performs parameter sweeps for resistor selection purposes,
% with a focus on power dissipation through BJT/resistors.
%  
%        Vdd
%         |
%         |  
%         Rb  B|./ C
% Vout ---/\/\/\----|  
%    |' \  E
%    |  Re
%    "----/\/\/\---- GND
%

clear all
% Declaration of Constants and Variables
% All constants were determined using the MMPQ3904 datasheet
Vbe = 0.85;  % Base/emitter voltage of BJT, assuming ~0°C [V]
hfe = 150;  % Beta value
Vout = 5;  % Voltage from Op-amp [V]
Vdd = 5;  % Power Supply [V]

% Vbe loop equation
% Vout - Vbe - Ib*(hfe+1)*Re+Rb = 0
% Ib = (Vout - Vbe) / ((hfe+1)*Re + Rb)

% Sweep Re and Rb.
Rb = [1000,3000,5000,10000];  % Base resistor [Ohms]
Re = linspace(10,250,240);  % Emitter resistor [Ohms]
Ib = zeros(4,240);
PR = zeros(4,240);
PT = zeros(4,240);

% Power dissipation for case 1
for k=1:4
  for i=1:240
    Ib(k,i) = (Vout - Vbe) / ((hfe+1)*Re(i) + Rb(k));
    Ie(k,i) = Ib(k,i)*hfe+1;
    PR(k,i) = Ie(k,i)^2*Re(i);
    PT(k,i) = (Vdd - Ie(k,i)*Re(i))*Ie(k,i);
  end
  [C,ind] = max(PR(k,:));
  disp([C,ind+10])
end
clf
figure(1)
hold on
plot(Re,PR(1,:),’blue’)
plot(Re,PR(2,:),’black’)
plot(Re,PR(3,:),’red’)

Appendix A
Heater Optimization MATLAB Script
plot(Re,PR(4,:),'green')
title('Resistor Power Dissipation vs. Load Resistance');
ylabel('Power [W]');
xlabel('Re [Ohms]');
legend('Rb = 1 kΩ','Rb = 3 kΩ','Rb = 5 kΩ','Rb = 10 kΩ')

figure(2)
hold on
plot(Re,PT(1,:),'blue')
plot(Re,PT(2,:),'black')
plot(Re,PT(3,:),'red')
plot(Re,PT(4,:),'green')
title('BJT Power Dissipation vs. Load Resistance');
ylabel('Power [W]');
xlabel('Re [Ohms]');
legend('Rb = 1 kΩ','Rb = 3 kΩ','Rb = 5 kΩ','Rb = 10 kΩ')

figure(3)
Ptotal = PT+PR;
hold on
plot(Re,Ptotal(1,:),'blue')
plot(Re,Ptotal(2,:),'black')
plot(Re,Ptotal(3,:),'red')
plot(Re,Ptotal(4,:),'green')
title('Total Power Dissipation vs. Load Resistance');
ylabel('Power [W]');
xlabel('Re [Ohms]');
legend('Rb = 1 kΩ','Rb = 3 kΩ','Rb = 5 kΩ','Rb = 10 kΩ')

figure(4)
hold on
plot(Re,ie(1,:),'blue')
plot(Re,ie(2,:),'black')
plot(Re,ie(3,:),'red')
plot(Re,ie(4,:),'green')
title('Total Emitter Current vs. Load Resistance');
ylabel('Current [A]');
xlabel('Re [Ohms]');
legend('Rb = 1 kΩ','Rb = 3 kΩ','Rb = 5 kΩ','Rb = 10 kΩ')
Appendix B

Pulsed Langmuir Probe Schematics

Figure 32: pLP top-level schematic.
Figure 33: FPGA I/O connection schematic
Figure 34: FPGA power schematic
Figure 35: Sampling subsystem schematic
Figure 36: AWG subsystem schematic
Figure 37: Power subsystem schematic
Figure 38: Debug subsystem schematic
Figure 40: Electrometer schematic
Figure 42: 3D view of top of pLP (left) and bottom (right)
Appendix C

LabVIEW DAQ Program

Figure 43: Front panel of DAQ program

Figure 44: Block diagram of DAQ program
REFERENCES


Academic Vita

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Education

**The Pennsylvania State University**  University Park, PA  Expected Fall 2014
B.S./M.S. Electrical Engineering
Schreyer Honors College

**Coursework:** Plasmas ♦ RF Propagation in Media ♦ Analog and Digital Communications

Experience

**NASA Ames Research Center**  Electrical Engineering Intern: Summer, 2012
- Developed wireless sensor modules for wind tunnel test articles from concept to protoboard demonstration.
- Refined time of flight probing technique for velocity characterization of a small arc jet.
- Designed and built an in-line amplifier used with heat flux transducers.

**The Aerospace Corporation**  Ionospheric Studies Intern: Summer, 2011
- Developed IDL code for analyzing GPS occultation data.
- Performed ground test of GPS occultation receiver and antenna.
- Conducted vacuum chamber testing of ionization gauges.
- Researched anomalous electron density enhancements in the night-time ionosphere, and presented research at the AGU 2011 Fall Meeting.

**Student Space Programs Laboratory**  Lab Manager: Summer 2013 – present
Science/Payload Subsystem Lead: Spring, 2010 – Summer 2013
Member: Fall, 2009 – Fall, 2010
- Leading a lab of undergraduate and graduate students in learning about space systems and systems engineering.
- Designed, built, and tested a power board for the CanSat payload competition. Designed circuit for burn-wire deployment.
- Developed a COTS GPS solution for an in-development cube satellite bus, consisting of an RF front end and interface to bus.
- Led a team of students to define a CubeSat mission concept and requirements, collaborate with research scientists, and prepare a funding proposal.
- Designed electrometer circuit for 100 pA to 100 uA current sensing with thermal stabilization

### Activities and Honors

- Member, Schreyer Honors College
- Member, The Institute for Electrical and Electronics Engineers (IEEE)
- Member, American Geophysical Union (AGU)
- American Geophysical Union (AGU) Max Hammond Travel Grant for outstanding students in the Earth and space sciences – 2011 Fall Meeting
- President (2011–2013), Penn State Kendo Club
- Member, Penn State Ballroom Dance Team
- Eagle Scout, Boy Scouts of America

### Technical Skills

**Proficient**
- Altium Circuit Designer: Schematic, PCB layout, and SPICE
- LabVIEW: CLAD certified
- MATLAB

**Novice**
- C, C++
- Xilinx ISE / HDL
- IDL

### Publications and Papers