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MATERIAL PHYSICS STUDY OF SIC MOSFETS

DAVID A. RYDZEWSKI

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Reviewed and approved* by the following:

Patrick M. Lenahan
Distinguished Professor of Engineering Science and Mechanics
Thesis Supervisor

Akhlesh Lakhtakia
Charles Godfrey Binder Professor in Engineering Science and Mechanics
Honors Adviser

Judith A. Todd
P. B. Breneman Department Head Chair
Professor, Department of Engineering Science and Mechanics

* Signatures are on file in the Engineering Science and Mechanics office.

Abstract

SiC is a wide band gap semiconductor material that has a lot of potential in high power and high temperature applications. In this study, we use two types of C-V measurements, the Gray-Brown and Jenq techniques to observe the density of states and defect concentrations within SiC MOSFET samples. Comparing devices prepared with different oxide growth techniques, we observe large differences interface trap concentrations in two devices. Our results suggest the NO/NO_2 annealing step helps lower the defect concentrations and supports recent magnetic resonance measurements.

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I. Introduction

Semiconductors and semiconductor based devices have become a key component in human society. Many, if not most, tools have become integrated with such electronic devices to improve efficiency or add some additional function. Computers are an integral part and component of our advances in technology, business, and social networking. Present day electronic devices are usually made of silicon. However, silicon devices in high temperature, high power, and high frequency applications are far from ideal [1]. With a political climate encouraging the development of more efficient technologies because of environmental concerns there are good reasons to look for materials capable of making technology more environmentally friendly. In make devices capable of high temperature and high power operation a new semiconducting material is needed.

In order to find a material that has the potential to replace silicon there must be an understanding of how one operates at higher temperatures. One electrical characteristic that helps determine a maximum operating temperature is a band gap. The band gap is the energy difference between the valance band and conduction band of a semiconductor. There are quite a few semiconducting materials that possess a wide band gap. A few examples are Aluminium Nitride (AlN), Gallium Nitride (GaN), Boron Nitride (BN), and Silicon Carbide (SiC) [2]. These materials, with the exception of SiC, have native oxides grossly inferior to SiO_2, so device integration of those particular wide band gap semiconductors can be difficult.

SiC has many advantages as a semicondcutor material. The electronic properties of SiC depend upon its polytype, and of the two most utilizable polytypes (4H and 6H), 4H has the

higher mobility of the two making it attractive for electronic devices. 4H SiC has a band gap of 3.2 eV while Si possesses a band gap of 1.12 eV [3]. This larger band gap allows higher operating temperatures for SiC devices [1]. In addition to SiC's wide band gap it also has higher thermal conductivity than to silicon which is advantageous in high power operations [1,3].

SiC has many advantages in particular applications, but the things that make it so effective in high temperature and high power operations also have a tendency to make it difficult to produce [1,2]. SiC is very resistant to chemical attacks and very thermally stable. Hence, semiconductor grade SiC requires very high manufacturing temperatures, in excess of 2500 Kelvin [3]. These very high temperatures can create a higher number of defects and interface states which in turn make these SiC devices unreliable.

Just as silicon had defect problems during its development process as a semiconductor material, so does SiC. An important contributing factor to SiC defects are the relatively high temperatures that are required to make SiC. The defects are not very well understood, though they have been detected using a variety of methodologies for example, electron paramagnetic resonance (EPR), electrically detected magnetic resonance (EDMR), and deep-level-transient spectroscopy (DLTS) [4-7].

I. Literature Review

Semiconductor Operation Principles

Semiconductors devices have become critical to our society. In order to understand semiconductor physics one must have some grasp of band theory. The valance band corresponds to a range of energy values that arise from the bonding molecular orbitals between atoms of the lattice [8]. The conduction band is what its name implies. This band is a range of energy values greater than valence band where an electron is free to move around in the atomic lattice of the material, and hence conduct [8].

Between both the conduction and valance band the Fermi Energy. The Fermi Energy The fermi level is a potential energy of an electron within a solid material. This energy level will shift within the band gap of a material due to changes in doping and temperature. This can be calculated using a calculated or known doping of the material by using one of the following equations depending on the type of device in question

$$p = N_v \exp\left[-\frac{(E_f)}{kT}\right], \tag{1}$$

$$n = N_c \exp\left[-\frac{(E_g - E_f)}{kT}\right]. \tag{2}$$

A band gap is the energy gap between the valance band and the conduction band of a material where no energy states exist [8]. This lack of energy states forces an electron acquire energy equal to or in excess of the band gap in order to be excited or ‘promoted’ from the valence band to the conduction band.

A band gap in a semiconductor is usually measured in electron volts (eV). The difference between a semiconductor and an insulator in terms of a band gap is related in terms of magnitude. Depending on the other electrical characteristics of a material, it will considered a semiconductor with a band gap less than 3.5 eV, while if the material has a band gap greater than 5 eV it will be considered an insulator. A semiconductor material with a very high band gap essentially acts like insulator due to the high energy requirement to excite an electron to a conduction band essentially inhibiting conduction.

Semiconductors conductivity can be altered by doping the semiconductor material with acceptors or donors. For example, if one wants to make p-type silicon one would add an element from the Group III of the Periodic Table [8]. This can be an element such as, Boron or Aluminum. When added to Si, it will effectively take an electron from the base semiconductor material as it tries to form bonds between all of its neighbors. However due to the lack of a fourth electron, a hole is formed. A hole is acts like positive charge carrier that emerges from an acceptor doping of the semiconductor material.

This process is different for an n-type semiconductor, in which the majority carriers are electrons. When adding a donor doping material (a Group V element for Si) to the donor adds, an electron to the silicon conduction band [8]. In silicon, due to the five valence electrons in the impurity atom, while forming bonds with the neighboring Si there will be an extra electron. This electron is then free to act as charge carrier for the semiconductor.

The type of majority charge carrier determines the type of semiconductor material. For example, if the material uses holes as the primary charge carrier then the material will be considered p-type.

MOSFET Principles and Operation

One of the most important devices in modern day technology is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The basic structure of a MOSFET is exactly as the name implies. The metal on a MOSFET refers to the gate which is separated from the doped semiconductor by an oxide layer. For silicon devices, native oxide is SiO_2 [9].

MOSFET operation is a moderately complex process. For the sake of argument we will be assuming that the semiconductor is a p-type and the source and drain have n+ doping. The n+ doping indicates very high concentration of donors. The channel regions of high doping must be opposite than that of the semiconductor material, and these regions are referred to as the source and the drain.

In order to understand MOSFET operation, one must consider the two voltages that are applied to the material. A voltage is applied to both the gate and the drain. With a p-type semiconductor with n+ source and drain the majority carrier in the body of the semiconductor are holes. Hence, in order to turn the device 'on,' a positive gate voltage is required to invert the channel, that is to fill it with charge carriers in opposition that of the majority carriers. Positive voltage creates an electric field that penetrates through the oxide. The resulting electric field repels the holes which will form a depletion region in the semiconductor material and an inversion region at the oxide interface.

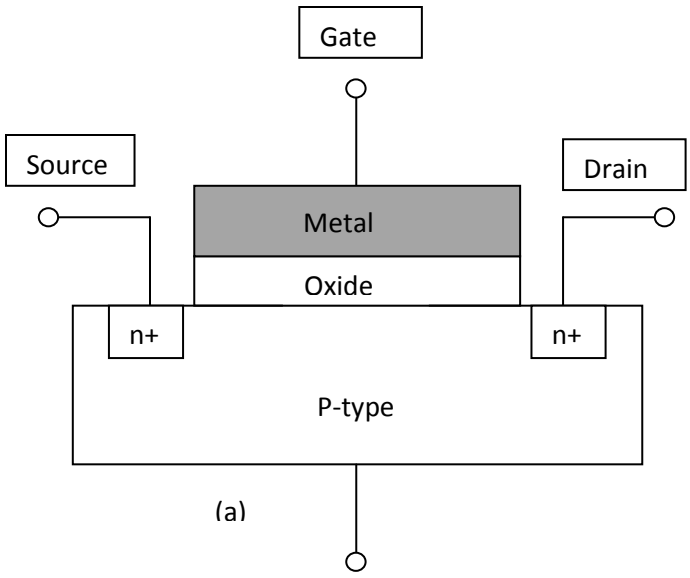

Fig 1. Diagram of MOSFET for illustrative purposes.

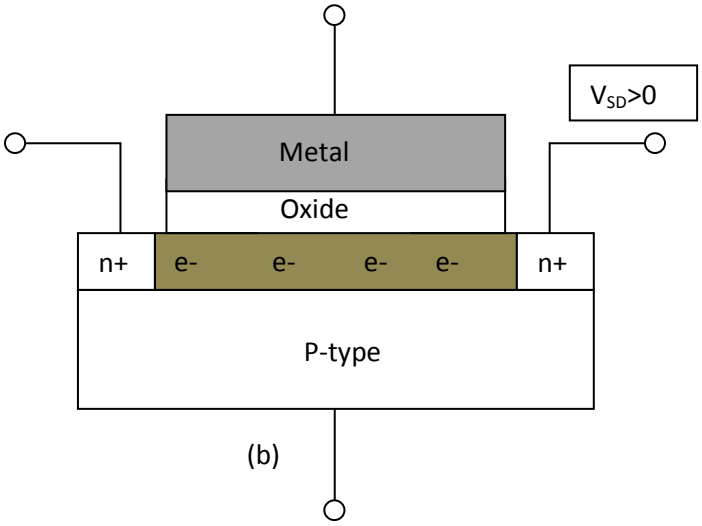

Fig. 2 - MOSFET in the 'on' state. This condition occurs with an applied gate voltage greater than the threshold voltage and with a voltage applied to the source and drain.

When the threshold voltage is reached the minority carriers of the p-type material will appear in at the semiconductor/insulator interface. Applying a voltage between the source and the drain, current will flow between the source and the drain. When current is flowing the device is considered to be 'on.' The magnitude and stability of this current can be limited by

defects within a semiconducting material, and especially by defects on the semiconductor/insulator boundary.

Potential of SiC

Silicon devices in power switching applications were reaching have limitation at high temperature and high power conditions [3]. Electronic devices made of silicon are usually unable to operate at temperature in excess of 250 ^{o}C [2].There are high temperature applications in aerospace field which would require device operation in the realm of 350 ^{o}C to 500 ^{o}C for turbine engines and other electric aircraft [2]. Other applications that benefit from SiC development would be nuclear reactors, high-power microwave transistors, power semiconductors and rectifiers, and LEDs [1-3]. All of these applications would have far reaching impacts, including green technologies, high power situations systems in windmill power generation. Table 2, provides a comparison of potential wide band gap with silicon [3].

Property/Material	4H SiC	6H SiC	GaN	Si	GaAs	AlN
Thermal Conductivity (W/cm K)	4.9	4.9	1.3	1.3	.5	2.0
Bandgap (eV)	3.2	3.0	3.44	1.12	1.42	6.2
Available doping	n,p	n,p	n,p	n,p	n,p	Insulator
Electron Mobility (cm^2/(V s))	1000	600	900	2050	8500	---
E_b(MV/cm)	9.7	10.0	12.2	11.8	12.8	8.9

Table. 1 - Electronic properties of Si, SiC poltypes, and other wide band gap materials [3].

As mentioned previously, 4H SiC has a band gap of 3.23 eV, and many other favorable electronic characteristics that places it ahead of the other wide band gap materials. The wide

band gap increases the operating temperature since increases in temperature cause semiconductors to act more intrinsic, which in turn causes a p-n junction to fail.

Looking at Table 1, it can be seen that 4H SiC has an electron mobility of 1000 $cm^2/(V\ s)$ and a high thermal conductivity of 4.9 W/cm K [3]. A higher thermal conductivity means that for an equal power going through a SiC and Si devices, the SiC device will dissipate heat more effectively resulting in more efficient devices [2]. Conductivity is essentially proportional to electron mobility and as such keeping this value high allows is of considerable important when picking a semiconductor material. While the electron mobility for SiC is inferior to Si (2050 $cm^2/(V\ s)$) it can still be considered a good value [3]. The greater electron mobility of the 4H SiC over 6H SiC, makes it more attractive in power MOSFET applications.

SiC has a few other potential advantages. It possesses a high saturated electron velocity of $2.0x10^7$ m/s which is twice the value of silicon, twice that of silicon, this makes SiC attractive for high frequency applications. Also SiC has very high critical breakdown field of 2.2 MV cm^{-1} (4H SiC) which is slightly less than ten times the breakdown field of Si, which is 0.25 MV cm^{-1}[1]. When high power loads and situations are applied this material property keeps the device from avalanche failure. SiC also exhibits high hardness value, a high resistance to chemical attack, and its high temperature survivability [3]. However, one of the most appealing characteristics is that SiC's natural thermally grown oxide is SiO_2, which is known for superior dielectric properties in MOS applications [1-3,10].

Arguably, the greatest manufacturing concerns with SiC involve the very characteristics that make it appealing in all of these applications. The high thermal stability and chemical

stability make SiC fabrication difficult [2]. Also the diffusion coefficients for the dopant atoms at the Si device processing temperatures are very low, forcing manufacturers to use an ion implantation method, which require a post implantation temperature of up to 1700 ^{o}C [2].

Silicon Carbide Defects and Defect Concentrations

SiC may seem like a very advantageous material over silicon; however in 4H SiC MOSFETs the SiC/SiO_2 interface is plagued with a high interface trap densities. Interface traps are defects that reside on the edge between the semiconductor and insulator [11]. These interface traps (roughly 10^{11} to 10^{12} cm^{-2} eV^{-1} for SiC/SiO_2) are roughly two orders of magnitudes greater than what is seen in Si/SiO_2 interfaces [10]. The critical issue with these defects is the downgraded effective channel mobility due to their presence. The charged interface traps affect the performance by decreasing the number of carrier in the channel, reducing the true channel mobility, increasing the threshold voltage, and causing leakage current to arise [10].

All of the issues above can have large effect on MOSFET and device operation. Decreased channel mobility makes it difficult to move charges through the channel making it less efficient. The noticed decreases in mobility can be attributed to the interface and near interface traps [11, 14]. These traps can capture charge carriers inhibiting conduction, but also can act as recombination center [12]. Near interface charge defects can scatter charge carriers moving through the channel by columbic scattering effects [11].

Manufacturing techniques are being developed in an attempt to reduce the number of defects and hence improve reliability of SiC devices. NO annealing at the moment

seems to provide a step in the right direction as devices that undergo this process seem to show better channel mobility values and lower densities of states near the band edges [6,13].

4H SiC MOSFETs exhibits particularly low channel mobility after dry oxide growth which resulting in marginal drain currents. Under these oxidation conditions 6H silicon MOSFETs share significant mobility issues, though not to the same degree [6]. An important advance in SiC MOSFET manufacturing is the NO/NO_2 annealing process. Through the use of C-V measurements and Deep Level Transient Spectroscopy (DLTS) this process has been showed to provide a significant reduction of the interface trapping [6, 14].

There is a lot of study into what exactly the defects are in silicon carbide. Some papers suggest that the defects are present in the oxide [15], while others suggest that the defects reside on both sides of the SiC/SiO_2 interface [5]. However, there seems to much complexity in the defects and their causes in SiC as compared to Si [5]. There are at least three different defects that have been detected using electrically detected magnetic resonance (EDMR) [5]. Of these three defects two seem to appear at the SiC/SiO_2 interface or on the SiC side of the interface. The first two defects, a silicon vacancy and a 'dangling bond' seem to be present at the semiconductor-oxide interface while the third appears to correlate with oxygen deficient silicon with a hydrogen atom located on the SiO_2 side of the SiC/SiO_2 interface [5].

C-V Measurements and Technique to Measure Defect Density

A particularly useful class of electrical measurements for SiC MOSFETs are capacitance-voltage (C-V) measurements. C-V measurements are performed on metal oxide semiconductor capacitors (MOS-C) or MOSFET devices. A MOS-C is somewhat different from a MOSFET. While

it contains the metal-oxide-semiconductor layers like the MOSFET, there is no source and drain and hence channel on the device. With the C-V technique, one sweeps a voltage through a range of voltages to bring a device under analysis into three types of biasing conditions: accumulation, depletion, and inversion, which will explained in the following paragraphs. For the sake of simplicity and illustration one will assume analysis on a p-type MOS-C device.

The accumulation region of a C-V curve occurs when a gate voltage is supplied which accumulates majority carriers in the semiconductor. For a p-type MOS-C device this would be a negative voltage [11]. This voltage causes the majority carriers (holes) to accumulate at the semiconductor/oxide interface since the oxide is an insulator. When making capacitance measurements in accumulation the capacitance is that of the oxide itself. Therfore one can find the oxide thickness from the measured capacitance. The accumulation oxide capacitance can be calculated as,

$$C_{ox} = \frac{\epsilon_o \, \epsilon_k}{t}, \tag{3}$$

where $\epsilon_o$is the permittivity of free space, ϵ_k is the dielectric constant of the oxide, and t is the thickness of the separation.

The depletion region occurs as one sweeps towards the opposite voltage from which one started in accumulation [11]. Keeping with the p-type example, the gate voltage would be swept from negative values to positive values. As this occurs the holes will be driven from the Si/SiO_2 interface [8]. This lack of charge carriers will then cause a depletion and insulting region to appear beneath the dielectric. This can be modeled in terms of a second depletion layer capacitance in series with the accumulation capacitance. Measurements taken under these

conditions will detect an oxide capacitance and a depletion capacitance in series [16]. Two capacitors in series act like resistors in parallel; the total capacitance is given by summing the reciprocals of the capacitances.

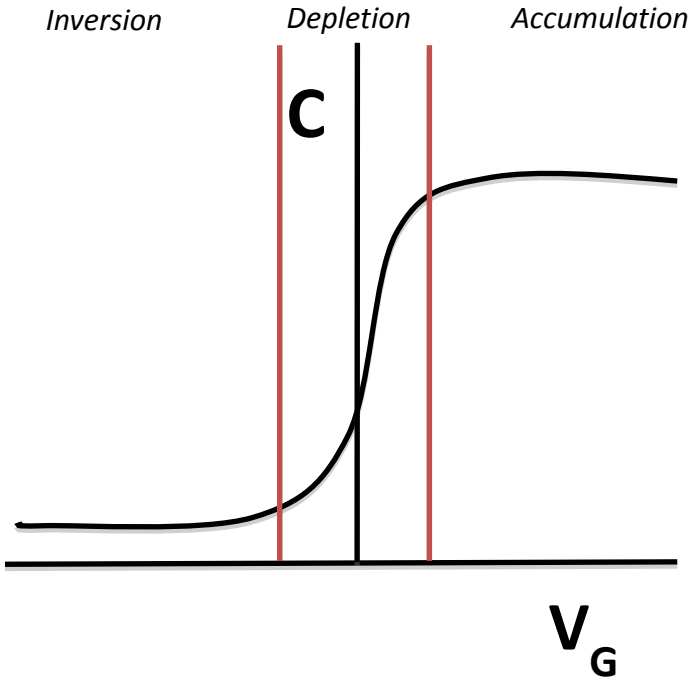

Fig. 3 - Illustration of the regions of a C-V curve.

The more positive the voltages that are applied to gate, the more the majority carriers will be driven away from the oxide. This widens the depletion region and further decreases the depletion capacitance and thus the total measured capacitance.

As the gate voltages reach sufficiently large positive values the threshold voltage will be reached; the is minority carriers will be drawn to the semiconductor/insulator interface. The electrons will gather at the substrate-to-oxide/well-to-oxide interface. This is called the

inversion layer due to the reversed polarity. Beyond the inversion gate voltage further increases in the positive voltage cannot draw any more minority carriers. Thus the capacitance reaches a minimum value.

The Gray-Brown Technique for Finding the Density of States

This methodology was first used by Peter Gray and Dale Brown to study defects in Si/SiO_2 system when the system was still plagued with performance limiting defects (hence the methodology has been named the Gray-Brown technique) [17]. This technique adds a temperature variable to the C-V measurement. The reason for this is that there is a temperature relationship between the Fermi energy, which changes with temperature. As temperature is changed the Fermi energy will change as well. To illustrate if one lowers the temperature in a p-type device the Fermi energy will move towards the valance band edge. C-V measurements can be taken at a variety of higher and lower temperatures to cover a range of values that can then be analyzed. This methodology can be used to acquire a multitude of information depending on the device in question.

When applying the Gray-Brown technique to an n-type device one would take a C-V measurement at a sampling of temperatures. When overlaying the results a hysteresis would form between the curves. This hysteresis represents a shift in voltage that arises due to the number of interface traps at the band edges. By changing the temperature of the device the Fermi Energy is moved, which changes the number of interface states that can be occupied.

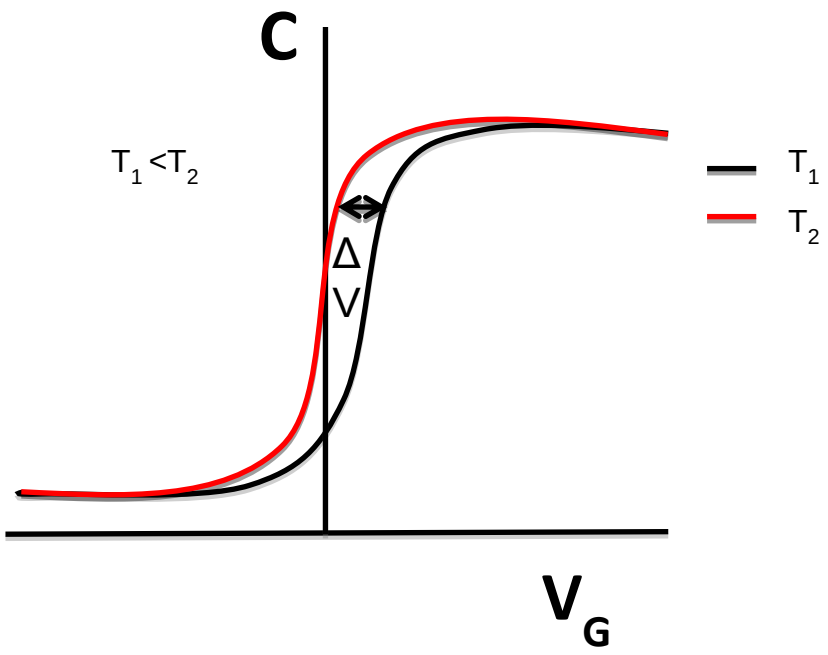

Fig.4- An illustration of a C-V curve of a n-type MOS-C device occurring at different temperatures and hysteresis that arises.

From this shift in voltage one can find the density of states. Since the Gray-Brown technique calls for the voltage shift to be taken at the flat band capacitance this provides an advantageous point for calculations as there is a lack of band bending at this point. This is due fact that the surface potential is equal to the Fermi Energy. However, the flat band capacitance must be calculated, which requires the calculated Debye length [16, 18]

$$\lambda_D = \sqrt{\frac{\epsilon_k kT}{q^2 N_x}}. \tag{4}$$

The equation above represents a Debye Length [18], where ϵ_k is the dielectric constant of the oxide, kT is the Boltzmann constant multiplied by the temperature (in Kelvin), q is the electron charge, and N_x is the local density of doping [16,18]. The Debye length gives the range

of an electrical interaction within the semiconductor material [16]. The flat band capacitance can be found using,

$$C_{FB} = \frac{\frac{C_{ox}\epsilon_k A}{1\times10^{-12}\lambda_D}}{(1\times10^{-12})C_{ox}+\frac{\epsilon_k A}{1\times10^{-12}\lambda_D}}. \quad (5)$$

Capacitance is known to be a function of the change in charge and voltage, where Δq is the change is charge, and ΔV is the change in voltage [19], as visualized below

$$C_{FB} = \frac{\Delta q}{\Delta V}. \quad (6)$$

. Using the known values of the capacitance and the change in voltage the charge of the interface states can be calculated

$$Q_{it} = C_{ox} \times \Delta V \quad (5)$$

Since an interface trap can only affect one electron or hole one can calculate the number of interface states, N_{it}, by dividing by the detected charge by the known charge of an electron

$$\frac{Q_{it}}{e} = N_{it}. \quad (6)$$

From here the density of states, D_{it}, is desired. However, this term is the number of interfaces states per area per unit energy

$$\frac{N_{it}}{\Delta E} = D_{it}. \quad (7)$$

In order to find this, one must calculate the change in energy that would be due to the change in the temperature

$$\Delta E = E_{f,2} - E_{f,1}. \quad (8)$$

The flat band condition in an n type device would give the density of defects near the conduction band edge, which is of interest in SiC MOSFETs as it suspected location of the majority of the performance limiting defects. However, the curves of a p-type device would give the density of defects near the valence band edge. While this measurement still holds importance, it is not of as much interest as the conduction band edge for SiC devices [20,5,6].

Jenq Technique for Finding Density of Defects in the Midgap Range

Another tool available to analyze the density of states in SiC MOSFETs is called the Jenq technique. This technique requires very little variation from the standard C-V measurement techniques already described. The Jenq technique detects at the density of states in the mid-gap range.

It is important to keep in mind the accumulation, depletion, and inversion region concepts for this measurement. In accumulation the majority carriers fill the interface states. For the sake of illustration assume a p-type device. Thus, the interface states under an accumulation voltage will be filled with holes. Thus as the voltage is swept towards depletion the interface states will still contain the holes, assuming that they are not emitted more quickly than the time the voltage sweep takes to get to the inversion region [21].

There is a variation on the Jenq technique, which changes based upon the device under investigations. For example, a MOS-C does not have a ready supply of additional minority carriers from which to form the inversion condition in a reasonable amount of time in SiC. As such an external excitation method must be applied. This can be due to thermal excitation

(raising the temperature, which is not desirable) or light stimulation. Since the energy of a wavelength of light is known by the equation below, the wavelength chosen for excitation must have energy greater than the band gap of the material. The energy of the wavelength of light is known to be,

$$E = \frac{hc}{\lambda}. \tag{9}$$

This value can then be related to the band gap to ensure optical stimulation of the minority carrier. Thus optical excitation during the deep depletion region of the graph, will excite minority carriers allowing recombination and allowing an inversion layer to form. Thus on the sweep back from inversion to accumulation the hysteresis that will arise, will be due to the non-equilibrium response of the mid-gap interface traps.

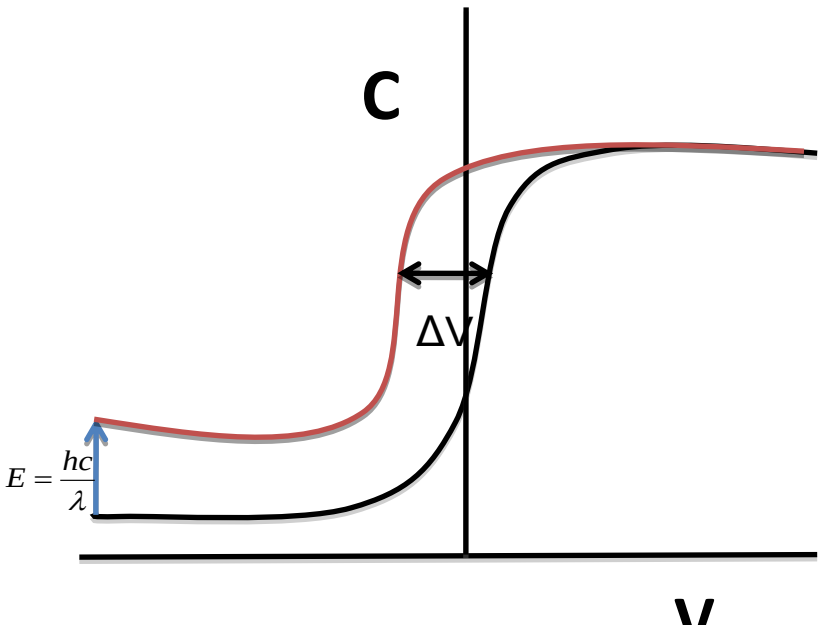

Fig. 4 - An example C-V curve for MOS-C n-type device.

Applying the Jenq technique a MOSFET is simpler due to the doping of the source and drain. The source and drain regions supply an abundance of the minority carriers for the body

of the semiconductor. As the gate voltages reaches sufficiently high appropriate values minority carriers will be drawn from the source and drain to fill the interface states. The hysteresis arises since the interface traps were filled with majority carrier in the forward sweep from accumulation to inversion, and filled with the minority carrier during the reverse sweep from inversion to accumulation [21].

II. Experimental Setup

The first series of devices for analysis were thin-film MOS-C devices. These devices had five nanometers thick oxides, and due to the thin oxide gave numerous problems with the C-V measurements.

The first sample of the second round of devices was a MOSFET produced by General Electric on 4H SiC substrate with p-type epitaxy and a doping of $1 \times 10^{17} \text{cm}^{-3}$. The 50 nm gate oxide was grown using a N_2O precursor at 1250^{o} C followed by a NO anneal at 1175^{o} C. Finally, Mo/Au was deposited as a bond pad metal. The sample's dimensions were 100 μm by 100 μm. The device was mounted on a 'tee,' which can be seen in Figure 6.

The second sample was a MOSFET produced by General Electric and was produced in a manner similar to the first with the exception that it did not undergo NO annealing.

Fig. 5 - A picture of a mounted device on a 'tee.'

Experimental lab equipment used in taking the C-V measurements included a HP Parameter Analyzer, a Booton Model 72C Capacitance Bridge, an IBM Variable Temperature

unit, and an Omega Platinum Thermometer. The HP Parameter Analyzer is a piece of equipment programmed in Basic to run the needed calculations. It is capable of outputting $\pm 20V$ in a desired step size. One would want to have a constant linear curve when taking C-V measurement but applying a very small step size and measuring the capacitance at each step will work. The 100 kHz Boonton Model 72C Capacitance Bridge provided the needed capacitance measurements.

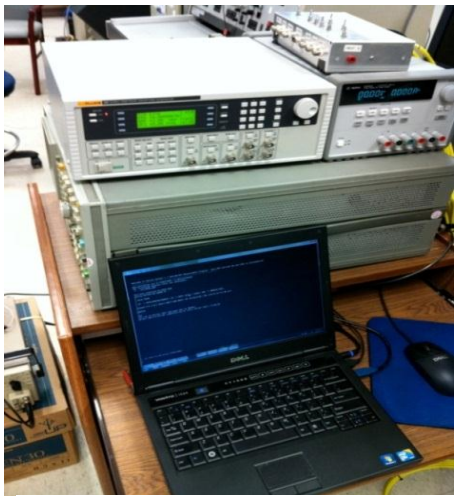

Fig.6 – The HP Parameter Analyzer.

Fig.7 – The Boonton Capacitance Bridge.

In order to control the temperature, multiple temperature systems were used. For lower temperature copper tube was immersed in liquid nitrogen. The temperature here was a function of the amount of liquid nitrogen in the dewar due to the fixed location of the device within the copper tube. Here the temperature was measured with the platinum thermometer which has an accuracy of 1^{o}C for temperatures ranging from -233 ^{o}C to 904 ^{o}C and an accuracy of 0.1 ^{o}C for temperatures ranging from 102.9 ^{o}C to 203.5 ^{o}C. By allowing for temperature stabilization over time there was very little variation (~$\pm 1^{o}$) over the course of the measurement.

Fig. 8 - The IBM Variable Temperature Unit

The HP Parameter analyzer was programmed to run C-V measurements over a range of ± 18 V and using a step size of 50 mV. The Capacitance Bridge provided a 100 kHz test signal, and the temperatures in this experiment ranged from 150 K to 400 K. The IBM Variable Temperature system has temperature range of about 95 K to about 400 K. The system uses liquid nitrogen to for the lower temperatures and can be adjusted to higher temperatures through the use of heated air.

III. Calculation Methodology

Analysis of the C-V curves using the Gray-Brown technique requires a series of calculations that will result in the density of states at either the valance or conduction band edge.

Since the equation to find a capacitance is known to be, $C = \frac{dq}{dV}$, where C is the capacitance and *dV* is the change in the voltage, one can solve for the change in charge, which is *dq*. When dividing this value by the charge of an electron one will get the number of interface states, $N_{it} = \frac{\Delta Q}{e}$. However, the desired value is the density of states which will be the number of states per unit area per unit energy. One must calculate the Fermi Energy at the respective measurement temperatures since the Fermi Energy will change as a function temperature. This can be calculated using equation 1 for a p-type MOSFET. After the change in energy is calculated for the respective temperatures one can divide the number of interface states by the change in the energy, $D_{it} = \frac{N_{it}}{\Delta E}$ [17].

The Jenq technique can be applied to the measurements with a little variation from the technique outlined above. The hysteresis that arises in the Jenq technique is used to calculate the number of interface states in the mid-gap range. Though observation one can see a parallel region between the forward and reverse sweeps of the C-V measurement for a specific temperature. Here the voltage shift used for the calculation is taken at the point at which the two regions change from parallel to not so. The same calculation methodology can then be applied with the exception of the change in energy. As the Gray-Brown is looking at the edges of the bands, while the Jenq looks at a widening range of the mid gap range as changes in

temperature occur. Hence, our ΔE must reflect this by finding the mid gap fermi energy and then calculating the fermi level for the temperature under analysis to get the energy over which the number of states are being detected.

IV. Results

C-V measurements were initially taken on thin film oxides, but there were multiple problems were found with using this data. While the curves generated looked similar to what would be expected from C-V measurements there were a few problems that invalidated the data from and calculating a density of states or applying the Jenq technique to the devices.

If one looks at the graph in Figure 9, it is fairly obvious that there is no leveling off of the curve in the accumulation region of the C-V curve. This prevents one from getting a reasonable answer using the Gray-Brown technique as the flat band capacitance value would be unknown. The reason for this is due to the thin film devices themselves. Thin films have problems providing reliable C-V measurements. When trying to identify the problem it was discovered that the oxides were also very 'leaky,' which could have been invalidated the capacitance measurements from the Boonton Capacitance Bridge. Another problem with the thin film MOS-C devices was due to the devices being fully metalized. The metalized surface prevented optically stimulated recombination to assist in reaching a full inversion region in the MOS-C devices.

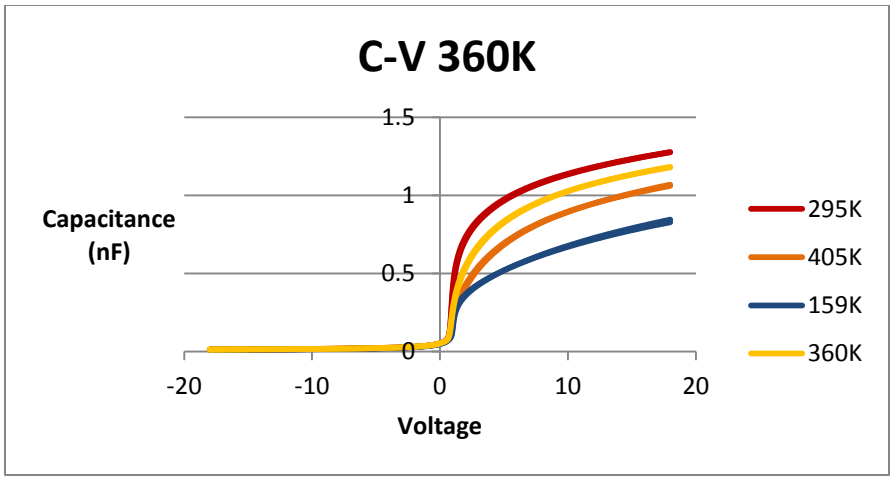

Fig. 9 - The collected C-V measurements of the thin film MOS-C at the temperatures on the graph.

The second set of devices involved MOSFETs with different oxide growth techniques. The MOSFETs allowed for simple application of the Jenq technique. Running through the methodology outlined, the densities of states for the various temperatures. The calculated density of states for the NO anneal MOSFET at 155 K was 8.4×10^{11} $cm^2 eV^{-1}$ while the dry oxide MOSFET had a density of states of 1.51×10^{12} $cm^2 eV^{-1}$ at 155 K. This shows a decrease by roughly a factor of two in the density of states due to the NO annealing process. This is supported by other electrical measurements in the lab and in the research world there are fewer detected defects in the NO annealed MOSFETs in comparison to the dry oxide MOSFETs.

The data displayed in Table 2 shows the density of states is decreasing with increasing temperature. This is supported by theory as the lower temperatures sample more of the band gap and part of the edges. A higher temperature encompasses a smaller energy range in midgap range. The higher temperatures show defects in the midgap range, but at lower temperatures where parts of the band edges are beginning to be sampled the density of states significantly increases. This increase indicates much higher defect concentrations at the band

edges as the density of states is a measurement of the average number of states per unit area per unit energy and an increase would be due to a higher concentration in those areas. This result is also supported by other measurements taken in the semiconductor laboratory.

	NO Anneal P-Type MOSFET		Dry Oxide P-Type MOSFET	
Temp. (K)	N_{it}, cm^2	$D_{it,}$ $cm^2\,eV^{-1}$	N_{it}, cm^2	$D_{it,}$ $cm^2\,eV^{-1}$
155	2.63191E+12	8.40629E+11	4.74499E+12	1.51E+12
200	2.02741E+12	6.55963E+11	3.51561E+12	1.15E+12
250	1.94113E+12	6.34058E+11	3.01954E+12	9.86E+11
300	1.85486E+12	6.16168E+11	2.3725E+12	7.88E+11
350	1.25095E+12	4.18489E+11	2.19995E+12	7.36E+11
400	1.20311E+12	3.8942E+11	1.85486E+12	6.32E+11

Table 2. Jenq data

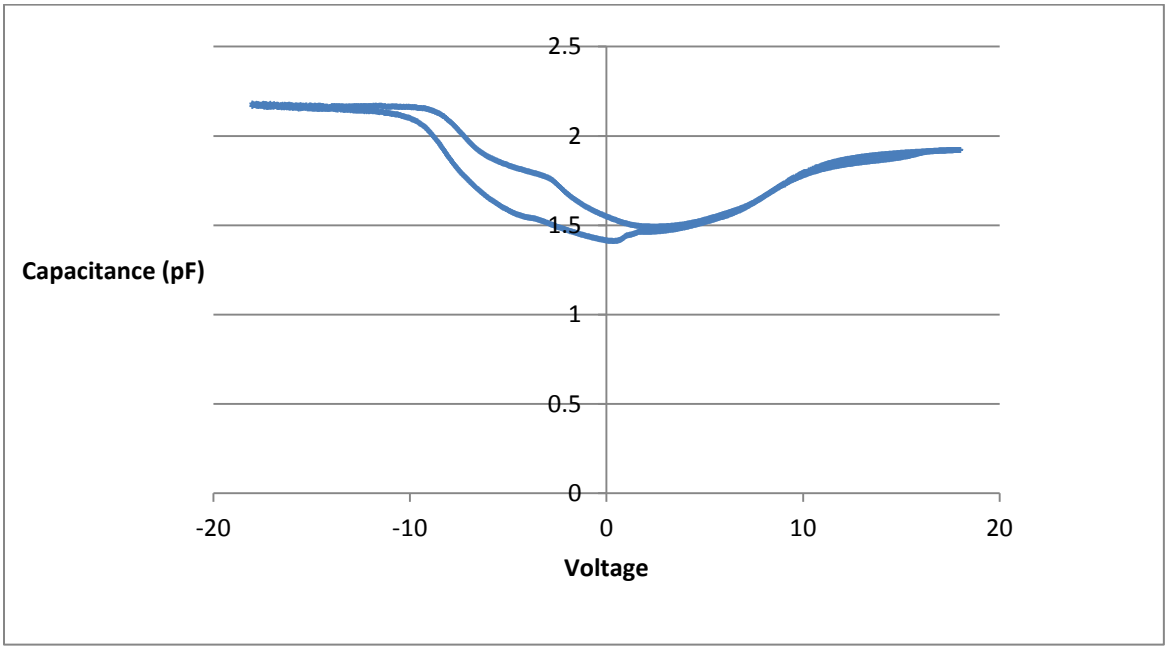

Fig. 9. NO Anneal MOSFET Jenq technique data at 155K.

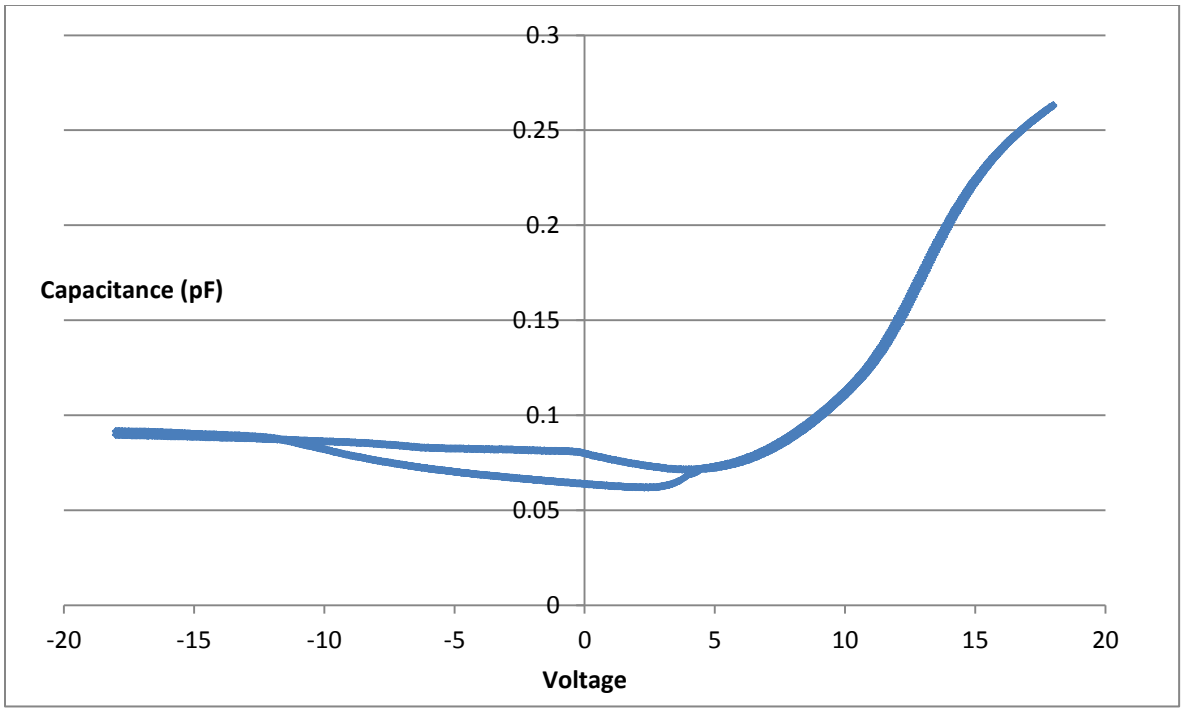

Fig. 10. Dry Oxide MOSFET Jenq technique data at 155K**.**

The Gray-Brown technique normally for the p-type MOSFET devices would yield the density of states near the valance band edge, however due some artifacts in the data collection a number of anomalies have arisen preventing meaningful data analysis. When looking at both graphs (Fig. 11 and Fig. 12) it is noticed that the accumulation capacitance is decreasing with temperature. Unfortunately, this observation is not supported by theory as the accumulation capacitance is a function of the materials used, the area of the capacitor, and as well as the thickness of the oxide. Another anomaly that prevents analysis on both MOSFET devices using the Gray-Brown technique is the fact that the inversion region capacitance is greater than that of the accumulation capacitance, which again, is not supported by theory or has any correlation from similar experiments [6]. This is an object of curiosity as no immediate reasoning comes to

mind to explain this. In the coming weeks additional testing will be completed to attempt to eliminate any potential error or artifacts in the data collection.

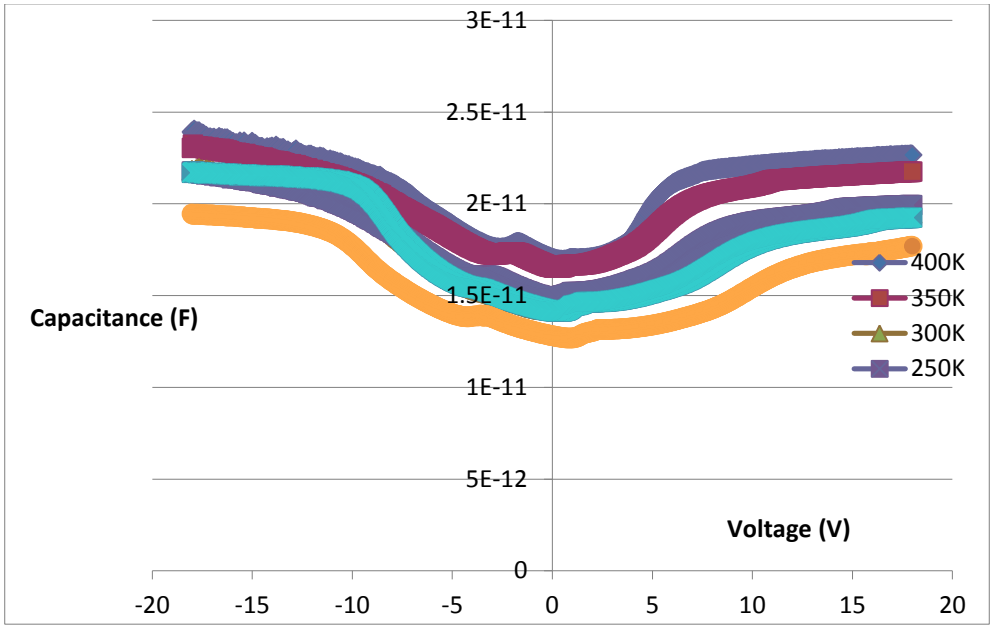

Fig. 11. NO Anneal MOSFET Gray-Brown technique data.

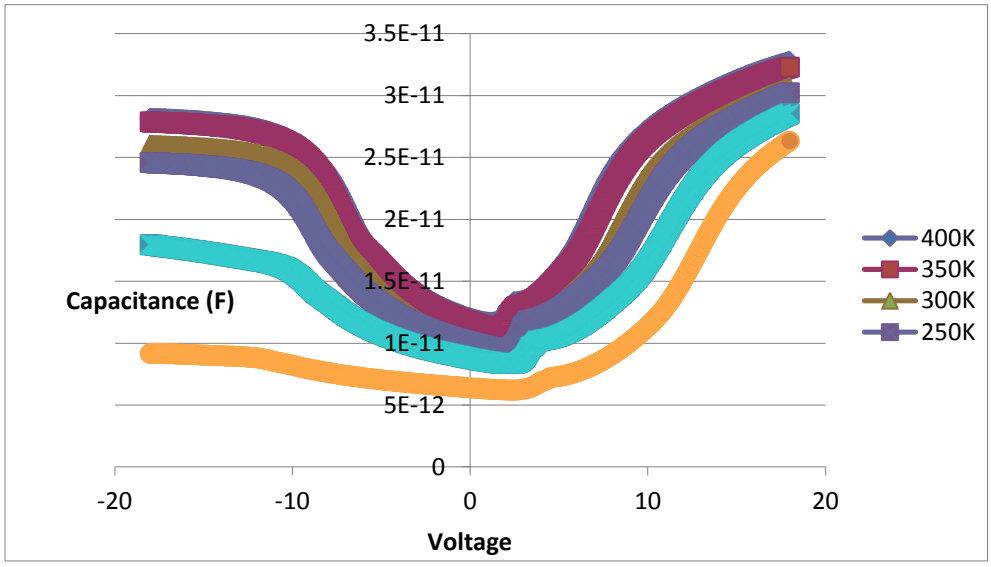

Fig. 12. Dry Oxide MOSFET Jenq technique data at 155K.

V. Future Work

There is much future work and additional work that can be added to this project and thesis. Adding C-V measurements to working and effective thick oxide MOS-C n-type devices could be used to find the density of states near the conduction band edge. As much research is interested in the defect concentrations near the conduction band edge one would have the opportunity to compare and combine the electrical measurements with other techniques such as electrically detected magnetic resonance (EDMR) to attempt to see a correlation between the number of measured defects and what exactly the EDMR measurements see.

Continuing this avenue of thought, additional thick oxide MOS-C devices without fully metalized surfaces would allow for full application of the Jenq technique. This would add another degree of completeness to the measurements as a greater range of defects could be accounted for. This could help affirm or refute any current thought processes on defects in SiC, as most defects are suspected to reside near the conduction band edge.

Another part of the project that additional work could be done on is the variable temperature system. Using an IBM stainless steel container donated to the lab by IBM over the summer, there is a goal to provide a computer controlled temperature system. Inside the stainless steel container there a heating element, which can could be connected to a power supply or to a LabView card. By using a digital thermometer with the ability to ‘talk’ with LabView, a feedback loop can be established so as to monitor and adjust power to the heating element to, in turn, adjust the temperature. The container can be immersed into liquid nitrogen for desired temperatures below room temperature and for temperatures significantly under

freezing dry nitrogen can be blown into the container to prevent freezing of the moisture that is present in the air. Hence the system has temperature and, to a small degree, environmental control. Current obstacles include the programming and figuring out a way of device integration with the 'tee' mounting that the lab currently uses.

Fig. 15- A picture of the stainless steel container supplied by IBM.

VI. Summary

SiC is a wide band gap semiconductor material that has the potential to replace silicon in high temperature and high power applications. The currently high interface trap densities in SiC prevent it from taking its place as a new mass produced wide band gap semiconductor material. While great steps have been made and new processes are being developed to attempt to reduce the defect densities there is still not a firm understanding of what exactly the defects are with the SiC material. While there are papers that suggest possible answers and locations of these defects [4-7] the full answer has yet to be discovered.

With the Gray-Brown and Jenq technique applied the p-type SiC MOSFET devices a comparison was drawn between the defect densities and the different oxide preparations for the SiC devices.

VII. Conclusions

Data analysis of the C-V curves using the Jenq technique on the p-type SiC MOSFET devices yielded the densities of states in mid-gap range. One object of interest is the difference of the densities of states of the dry oxide MOSFET device and the NO/NO_2 anneal MOSFET device. We found that there was a higher density of states in the mid gap range in the dry oxide SiC MOSFET than the MOSFET with the NO annealing with the Jenq technique. This observation is supported by other evidence and measurements from other lab personnel.

When looking at the Gray-Brown data, due to some artifact in our measurements or devices there was some observed data that is not supported by theory as outlined in the results section. The noticed unsupported theory activity prevents meaningful numerical analysis from being performed to get the densities of states at the valence band edge for the SiC MOSFETs. The measurements will be attempted again to in order to get meaningful data through the use of the Gray-Brown technique.

Overall, the experiments did show a correlation and affirmation of current thought processes regarding defects and their locations with SiC MOSFET devices. A lower density of states was recorded for the MOSFET that underwent the NO annealing process and a greater concentration was seen in the dry oxide MOSFET supporting other electrical measurements taken by the lab.

VIII. Appendix

```
config HP4205:03 RANGE:0
! DCIV UPDO
! HI -> GATE/DRAIN/SOURCE; LO -> BULK (VS1 -> BIAS; VM1 -> ANALOG OUT)
!sweep0 UPDO i=2 L=1e-2 s1(-5;.1;5) v4=0.0 YL=-20 Y=-1 M1 M4 o=4
!WARTEN
sweep0 i=3 L=0.1 MSW=2 MWT1=100 MSB1=18 s5(-18;0.05;18) LIN YL=0 Y=3 M5 o=4
WARTEN
!sweep0 i=3 L=0.1 MSW=2 MWT1=300 MSB1=-18 s5(18;0.05;-18) LIN YL=0 Y=1 M5 o=3
!WARTEN
!sweep0 i=1 L=0.1 MSW=2 MWT1=200 MSB1=-18 s5(18;0.1;-18) LIN YL=0 Y=2 M5 o=1
!WARTEN
!sweep0 i=1 L=0.1 MSW=2 MWT1=100 MSB1=0 s5(18;0.05;0) LIN YL=0 Y=2 M5 o=2
!WARTEN
!sweep0 i=1 L=5e-3 s1(-18;.1;18) v4=0.0 YL=-20 Y=-1 M1 M4 o=4
End
```

IX. Acknowledgements

I would like to thank the many people who helped make this thesis come about. First of all, I would like to thank Dr. Lenahan for providing so much support and opening up his lab to let me work with all the other smart and helpful people that make up his lab. Brad Bittle provided a great deal of support in terms of finding devices, wire bonding, and helping with general knowledge. Thomas Aichinger also helped out considerably as he taught me, not only the HP parameter analyzer, but also how to code for it. Thomas also helped by helping to troubleshoot the devices and thin film capacitors. Corey Cochrane and Jake Follman also helped set up the project in terms of equipment explanation and as a source of general knowledge. I would like to thank Matthew Storey, who worked with me with whom it was enjoyable working with in the semiconductor laboratory.

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Vita

David A. Rydzewski

Permanent Address
196 Kohlers Hill Road
Kutztown, PA 19530
(610)-295-2267

Schreyer Honors College

Local Address
200 Bradley Ave, TV-04
State College, PA 16801
dar5184@psu.edu

Education

The Pennsylvania State University, University Park, PA
Bachelor of Science in *Engineering Science* Expected Graduation: Fall 2011

Related Coursework

Analysis of Engineering Science
Engineering Thermodynamics
Computer Methods of Engineering Design
Mechanics of Fluids
Engineering Applications of Wave Concepts
Electronic Properties of Materials
Material Engineering
Effective Speech

Achievements

2010 P.B. Breneman Award in Engineering Science Fall 2010
Dean's List Fall 2008 - Present

Experience

Engineering Technician May 2010 - Present
Aberdeen Test Center, Aberdeen, MD

- Worked in a multidisciplinary team to achieve mission objectives for a variety of projects.
- Simplified data entry processes while adding error checking to ensure quality data input.
- Automated data entry processes saving hundreds of man hours.
- Provided data collection support during WIN-T testing for C4ISR.

Achievements

2010 P.B. Breneman Award in Engineering Science Fall 2010
Tau Beta Pi Member and Co-Activities Chair Spring 2010 – Present

Research Interests

There are many broad range of topics in the sciences and engineering realms that hold much interest to me. For example, carbon nanotube manufacturing techniques and carbon nanotube use as an artificial muscle are two more specific topics that I am interested in. However, there are many realms in the fields of physics and nanotechnology that I am excited to pursue.

Current Research

Engaged in research with semiconductors and more specifically SiC devices. Looking to further its potential in high power and high temperature applications through the use of electrical measurements to help locate the defects and defect concentrations that prevent SiC becoming a true force in the semiconductor world.