THE PENNSYLVANIA STATE UNIVERSITY
SCHREYER HONORS COLLEGE

DEPARTMENT OF PHYSICS

CHARGE CARRIER TRANSMISSION IN BILAYER GRAPHENE

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ABSTRACT

This thesis focuses upon experimentally deriving transmission rates of electrons as a function of angular incidence upon a potential barrier within bilayer graphene. This was achieved by creating a bilayer graphene device set atop a split gate that would allow for the establishment of a potential barrier; this process included exfoliation, transfer, and lithographic techniques. Due to the advanced and expansive nature of device fabrication and the testing process, my contribution to the project focused on three related tasks: the initial exfoliation of a suitable bilayer sample, modeling potential split gate geometries to examine electronic properties using simulation software, and imaging and analyzing a sample split gate edge contour. Ultimately, the experimental results that were obtained were not sufficient to make quantitative analysis possible. However, the work that I conducted to simulate gate geometries and also the analysis of a gate edge contour both yielded results that are useful for the ongoing study of bilayer charge carrier transmission rates; my simulation results provide computational models for various electronic characteristics of various split gate geometries, and my edge contour work provides a cursory treatment of a problem that can arise in experimentally derived transmission rates, as a result of the jagged nature of the gate surface.

TABLE OF CONTENTS

LIST OF FIGURES

ACKNOWLEDGEMENTS

This thesis was made possible by the contributions of many individuals, both in and out of the lab. In the lab, I was aided considerably by Jing Li; he made significant contributions to my own development of lab techniques, and he allowed me to draw upon his wealth of experience on numerous occasions, especially for the method of analyzing the data for the gate profile. He is the individual who performed the electron beam lithography work, as well as the electronic measurements of the device; he was assisted by Yevhen Tupikov, another graduate student, taking the electronic measurements. I would also like to acknowledge Zhenxi Yin, a fellow undergraduate, for his role in the device fabrication; he was responsible for the transfer of the bilayer graphene I exfoliated. Finally, Jake Shevrin was very helpful as he showed me the basic functions of the atomic force microscope.

I would also like to acknowledge the support of the physics department, particularly Prof. Robinett and Prof. Zhu, both of whom were instrumental to my choosing and sticking with physics as a major. Their dedication to science cannot be understated, and neither can their dedication to helping students grow.

I would finally like to thank my family and Leah for their unceasing encouragement, love and common sense; without these three aspects of their support working in concert, I don't know where I would be, both as a scientist and as a human being.

Chapter 1 Introduction

The motivation for my work was the theoretical predictions of the transmission of electrons at a potential boundary that were made for bilayer graphene [1]. Unlike monolayer graphene, which has an experimentally verified electron transmission rate of 100% at normal incidence upon a potential boundary, bilayer graphene is predicted to have an electron transmission rate of approximately 0% with normal incidence [1]. The difference in the predicted transmission rate for bilayer graphene is suspected to be a result of the electrons behaving as massive, chiral fermions, in contrast to their massless behavior in single layer graphene [1]. This thesis was designed to test the angular dependence of electron transmission in a two-terminal, bilayer device at a potential boundary, using a magnetic field to tune the angle of incidence of the incoming electrons at the barrier.

This experiment involved the fabrication of a bilayer, split-gate device using a combination of exfoliation, transfer and lithographic techniques. To supplement the experiment, I added two other facets to my research. First, I performed a series of simulations using COMSOL Multiphysics to study the potential distributions and charge distributions associated with various split-gate geometries. Second, I began analyzing the roughness of an old device's gate edge profile with an atomic force microscope, in order to test the assumption that it could be considered perfectly smooth for calculations.

My thesis is laid out into six distinct chapters, including this introduction. The second chapter provides background information regarding graphene and its properties, and the third chapter discusses the fabrication of the split-gate device. The fourth chapter focuses on the modeling process with COMSOL, as well as analyzes the results of my simulations. The fifth chapter discusses the gate roughness analysis I was able to perform, and my thesis ends with chapter six, which includes my conclusions, ongoing work, and future possibilities for the experiment.

Chapter 2

Background Information

This chapter provides background information on graphene, with special emphasis given to the differences between monolayer graphene and bilayer graphene. The electronic properties are treated separately, as they are most pertinent to the experiment and require greater detail. Finally, the chapter concludes with an overview of p-n junctions, which are not unique to graphene but whose understanding is critical for understanding utility of the split gate and my simulation work.

2.1 Graphene Basics

Graphene is a single, atomic layer of carbon atoms, arranged in a honeycomb lattice [2]. Alternatively, graphene can be thought of as being composed of two triangular sub-lattices, A and B, overlaid according to Figure 2-1.

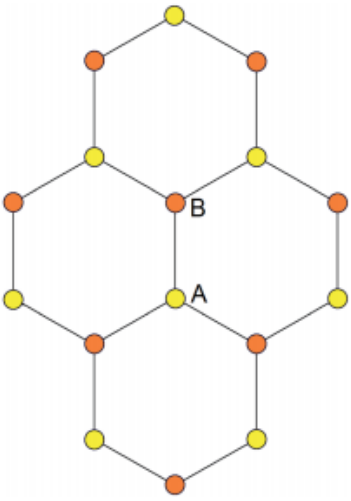

Figure 2-1: Graphene Structure and Sublattices, [4]

Graphene can be thought of as a single layer of graphite, another allotrope of carbon, from which it was first isolated in 2004 [2]. Graphene is a unique material, and it possesses several characteristics that warrant attention; one such characteristic is graphene's reactivity. As each carbon atom is exposed on at least two sides, graphene is extremely chemically sensitive and is the most reactive form of carbon [3]. While the term graphene is typically used to refer to a single, two dimensional sheet, it can also be used with stacks of a few sheets of graphene, such as bilayer and trilayer graphene, though these will be prefaced as such. An example of how graphene is stacked in multilayer configurations is shown in Figure 2-2.

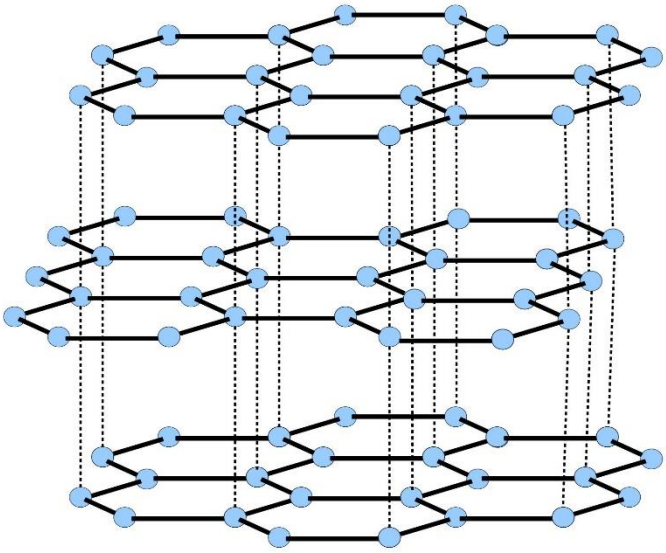

Figure 2-2: Stacked Graphene Configuration, [6]

In addition to graphene's interesting electrical properties, which will be discussed below, graphene touts a high thermal conductivity, an extremely high tensile strength, and a small spin-orbit interaction [3]. Once the sheets of stacked graphene exceeds ten layers, it is more accurately considered to be three dimensional graphite [2].

In my work, I collected graphene via mechanical exfoliation on silicon dioxide substrates (SiO2) using a process that was pioneered by Geim and Novoselov [5]. In addition to mechanical exfoliation,

graphene is currently being produced via chemical vapor deposition, epitaxy, and dispersion. Of the four, exfoliation and deposition were initially dominant, however there is major growth in all techniques, as outlined in Figure 2-3 [7]. The graphic illustrates the number of patents assigned to each method as of 2012; it is worthwhile to note that the chemical vapor deposition methods are often employed to produce high-quality, large samples for industrial applications, and that exfoliation methods are more commonly used by academic institutions who wish to explore graphene's properties on a smaller scale [7].

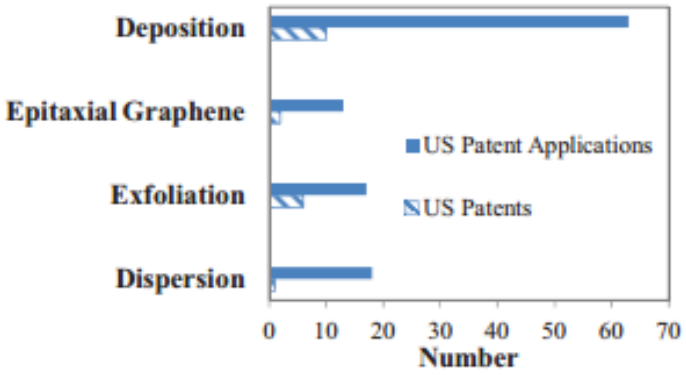

Figure 2-3: Graphene Patents and Patent Applications as of January 2012, [7]

2.2 Electronic Properties of Graphene

The electronic properties of graphene are the qualities that will be explored in this thesis, and sufficient attention should be paid to the cause of graphene's novel electrical behavior. Typically, electrons in materials obey a dispersion relation, or energy-momentum relation, that is quadratic [8]. This is easily observed in quantum mechanics, by the expression $E= \hbar^2k^2/2m$ [9]. This means that, if you look at a graph of allowable k-states within a 1-D material, relative to the energy of that electron state, you observe graphs like the one in Figure 2-4.

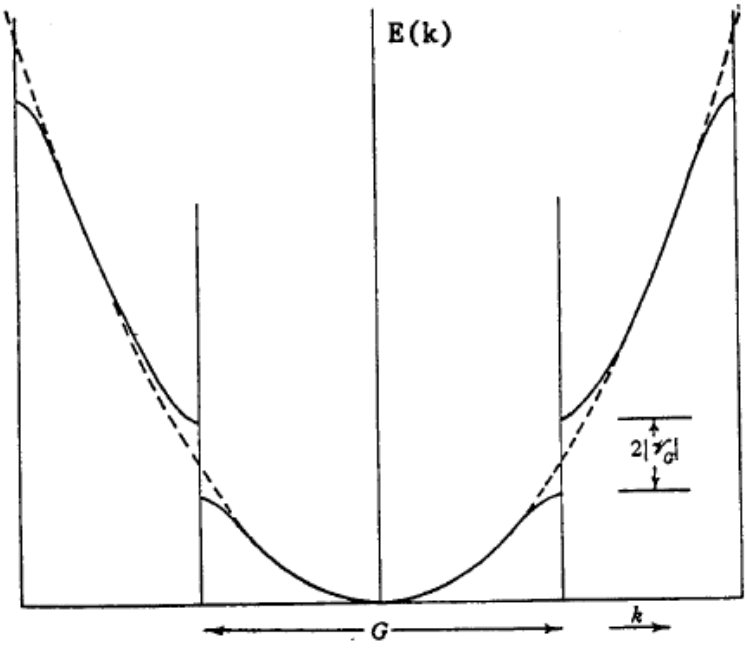

Figure 2-4: 1-D Nearly Free Electron Dispersion Relation, [8]

Such dispersion relations have band gaps, which are energy regions that hold forbidden states for electrons [10]. Graphene on the other hand produces a dispersion relation that is linear, in addition to having no band gap, at least for low energy excitations [11]. This dispersion relation is pictured in Figure 2-5:

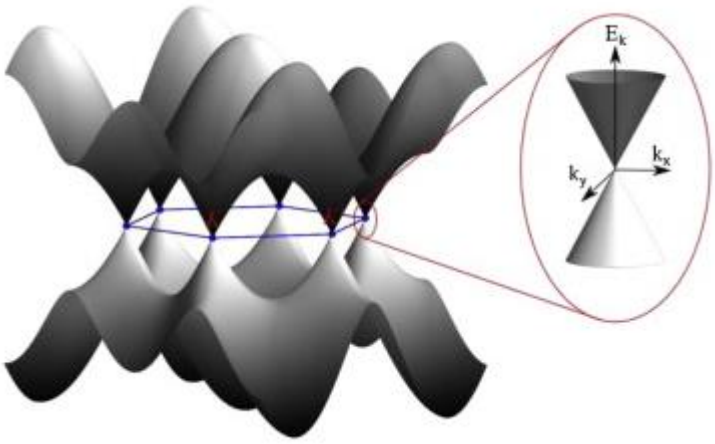

Figure 2-5: Linear Dispersion Relation at Dirac Points in k-space, [3]

This linear dispersion relation is typically exhibited by a massless particle, such as the phonon, with E=pc [12]. The reason for graphene's unique dispersion relation and lack of band gap stems from the unique feature of double pi bands that arise from sp^2 orbital hybridization in the lattice, which is a result of the two sub-lattices that comprise the honeycomb structure [12]. Graphene's unique orbital hybridization and corresponding Brillouin zone in reciprocal space create six points in the Brillouin zone where the valence and conduction bands touch at the Fermi level [3]. Since the Fermi level denotes the level at which all electron energy states below are filled and all states above are empty, the regions surrounding these points have zero band gap [8]. The electrons in these regions are described as massless Dirac fermions, which are governed by the Dirac equation and not the Schrodinger equation as one would expect of massive particles [2].

In addition to the linear dispersion relation with no band gap, electron mobility within graphene is extraordinarily high. At room temperatures, on a silicon dioxide substrate, graphene mobility is limited to approximately 40,000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [13]; however, when graphene is suspended between boron nitride pieces, the mobility can reach approximately 80,000 to 200,000 $cm^2 \cdot V^{-1} \cdot s^{-1}$; this means that the electrons are in the ballistic regime, and can be thought of as traveling in a straight, non-scattered path over a distance on the order of magnitude of a micrometer [14].

2.3 Differences Between Monolayer and Bilayer Graphene

In the previous section, I highlighted the novel aspects of graphene that make it such a significant material for modern research. In this section, the differences between monolayer and bilayer graphene will be discussed, to better illuminate the motivation behind this experiment. As previously discussed, monolayer graphene has electrons that behave as massless, Dirac fermions, governed by a dispersion relation that resembles that of a photon [11]. In bilayer graphene, the superposition of two lattices changes the behavior of electrons markedly; an illustration bilayer stacking is displayed in Figure 2-6:

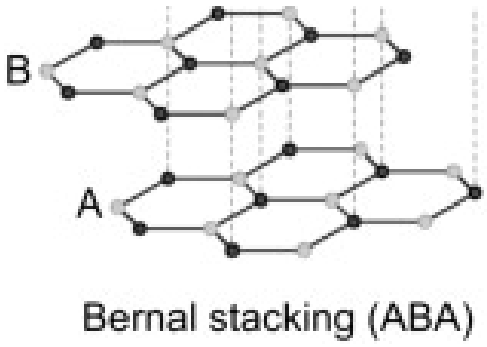

Figure 2-6: Bilayer graphene with Bernal stacking, [3]

This particular stacking configuration is known as Bernal stacking, and it changes the behavior of the band structure in the low energy regime to be quadratic, although again with zero bandgap; this means that instead of acting as massless Dirac fermions, the charge carriers once again adhere to a dispersion relation that is typically obeyed by massive particles [12].

2.4 p-n Junctions

P-n junctions are a specific semiconductor configuration that occurs when two different types of semiconductors are in contact with each other at an interface. The letters "p" and "n" correspond to the sign of the dominant charge carrier in each semiconductor; holes are positive charge carriers, and electrons are negative charge carriers. Typically, semiconductors do not have significant concentrations of either charge carrier intrinsically, and are doped with certain elements in order to increase these concentrations [15]. By creating this interface between the p-region and the n-region, a p-n junction introduces a potential gradient as electrons from the n-doped region diffuse into the p-doped region, leaving this area full of ions and no free charge carriers; this region is called the depletion layer [16].

The split-gate device is designed to create a potential barrier in the middle of the bilayer piece without chemical doping; this is established by having opposite voltages applied to the gates on either side of the gap. This established potential difference across the material results with each side being

electrostatically doped with a different charge carrier; electrons are the majority carrier for the sample segment that corresponds to the positive potential and holes are the majority carrier for the sample segment that corresponds to the negative potential relative to ground. The density of the charge carriers is also tunable, and can be changed with the voltage established on each gate. In this way, a p-n junction is established electrostatically via the split gates [16]. This barrier's establishment is critical to the experiment, because the predicted transmission rate of charge carriers incident on the barrier is fundamentally different for bilayer devices as opposed to monolayer graphene devices, and it is what we wish to test. The theory predictions for the charge carrier transmission rates as a function of incident angle are displayed in Figure 2-7. Notice the profound difference of transmission probability at 0°; for monolayer it is 100%, and for bilayer it is 0%.

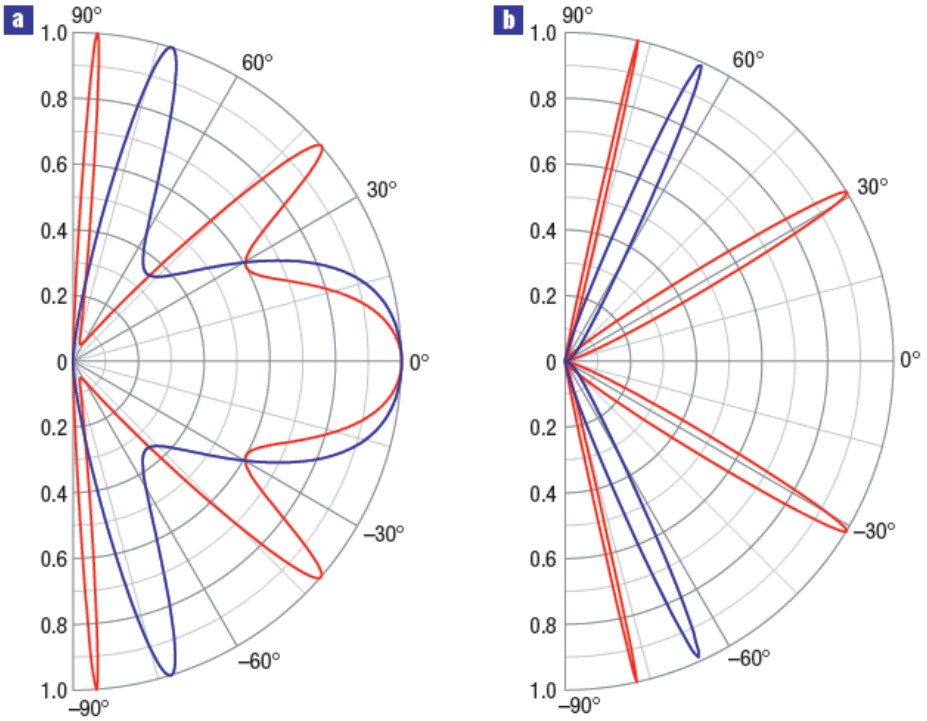

Figure 2-7: Transmission Rates of Incident Charge Carriers. Monolayer on the left and Bilayer on the right. The different colored curves represent different barrier heights, with blue representing a higher barrier, [1]

Chapter 3

Device Preparation and Fabrication

The process of obtaining a suitable, bilayer piece of graphene is arduous, due to the difficult nature of the exfoliation, identification and transfer processes. The meticulous and detailed procedure was essential for obtaining the pristine sample that could later be employed in our gated device, and is outlined in the first section of this chapter. The second section within this chapter focuses on the device fabrication process.

3.1 Device Preparation

As discussed in the previous chapter, graphene can be obtained through several different methods, and my own work involved mechanical exfoliation. This is a laborious process, and obtaining a suitable bilayer graphene flake and successfully transferring it took a great deal of time. Obtaining suitable flake candidates was my biggest contribution to the fabrication steps of the split gate device. My procedure for exfoliation is akin to the initial process that was employed by the Nobel Laureates who pioneered the process [5]. Before any exfoliation could be performed, a silicon dioxide coated silicon wafer needs to be cleaned. This process consists of washes with both IPA and ethanol within a sonicator, as well as an ozone cleaning step. I followed the overall cleaning process that is a standard procedure in the current graphene literature [5]. Substrates must be exceptionally clean in order to produce high quality graphene samples, like the ones sought for the device.

Once a suitable substrate was available, I could attempt to mechanically exfoliate graphene from flakes of highly ordered pyrolytic graphite, or HOPG. To summarize, the process consists of pulling a small flake of HOPG apart with a single piece of tape. If done correctly, the folding and unfolding

process allows for a uniform, thin layer of graphite on the adhesive surface of the scotch tape. After this layer is created, a small wafer of silicon dioxide coated silicon that was previously cleaned is placed beneath the area of most uniform graphite coverage, and the tape gently placed atop the wafer. This is followed by rubbing the piece of tape with a plastic tweezer, using minimal pressure, to ensure that all air has been pushed out of the area between the graphite layer and the substrate; this was always performed from one corner to the opposite, to ensure no bubbles were trapped beneath the surface of the tape. Finally, the tape was removed gently, using a rocking motion that lasted approximately one or two minutes. Besides coating the tape with a graphite layer of the proper thickness, this is the most critical step in the process. If the tape was pulled too quickly, very few pieces of graphene were ever deposited on the sample. If the tape was pulled too slowly, there would be excessive tape residue that contaminated pieces of graphene, rendering them useless for devices. After exfoliation onto a substrate was completed, the next step in obtaining a sample was to place the substrate under an optical microscope and search for bilayer graphene candidates.

Graphene on the SiO2 layer only absorbs 2.3% of incident light's intensity [17]. This is enough to be visible, but only barely as illustrated by Figure 3-1:

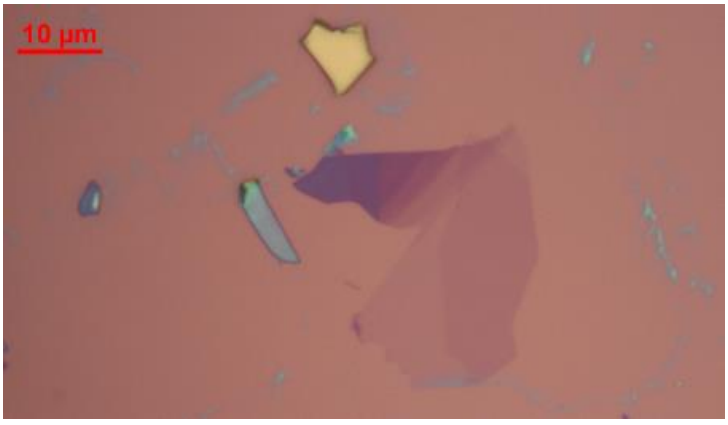

Figure 3-1: Graphene Layer Comparison on SiO2, Exfoliated by Zach Zern Oct. 2014

I used an optical microscope in lab with 10x and 100x lenses; 10x was useful for general scanning of large areas, while 100x was necessary for confirmation of layer numbers. The thickness of

graphite flakes is indicated by color when using an optical microscope [18]. For thick graphite flakes, the color is usually a golden yellow; for graphene, the color is a nearly transparent purple, as is illustrated in Figure 3-1. Multi-layer graphene flakes are slightly darker in color, although establishing what color represents bilayer is often difficult. The method that we established for my search involved having a control piece of graphene on a separate substrate that included a piece that had monolayer, bilayer and trilayer graphene all on one flake that had been broken at an angle. This allowed for consistent comparisons at any given light setting, which must be kept constant for each search, lest the coloration of the flakes change with the varying intensity of the incident light.

After suitable bilayer pieces were identified, they were checked for size and condition. For the device required for this experiment, there were no real size constraints, and most of the pieces we found were of adequate dimensions. The condition of the sample was the deciding factor, as we needed a piece without any cracks or tape residue in order to achieve electron mobility in the ballistic regime. Examples of these defects are illustrated in Figure 3-2:

Figure 3-2: Graphene Defects, Image Obtained by Zach Zern Oct. 2014

The transfer process employed in this thesis was selected because it produces extremely clean graphene devices due to the lack of potential polymer residue [19]. This is advantageous and produces superior cleanliness when contrasted with alternative methods [20]. It required first obtaining a graphene sample on a silicon dioxide coated silicon substrate, followed by

exfoliating two flakes of boron nitride onto poly-propylene carbonate, or PPC, which coated a silicon substrate. Once the dimensions of the graphene sample were known, two pieces of boron nitride that were larger than the graphene piece were exfoliated on the two new prepared substrates. Once the boron nitride flakes were obtained and identified, the thin PPC layers were removed from their respective substrates. Each of these separate PPC layers were affixed atop another transparent polymer called Polydimethylsiloxane, or PDMS. Ultimately, the boron nitride flake was placed flake-side down on the mount, and was positioned beneath an optical microscope such that the graphene piece and the boron nitride piece are visible. They were then aligned, and the boron nitride slowly lowered so that it "stamps" the graphene piece. This stamping process allows the more powerful Van der Waals interaction between the boron nitride and graphene to overpower the interaction between graphene and silicon dioxide, thus allowing the graphene to be lifted off of the surface cleanly [19]. This process is repeated, except the graphene serves as the stamp and another boron nitride flake acts as the graphene did previously. In this fashion, a heterogeneous, boron nitride – graphene – boron nitride structure is formed, with extremely clean interfaces between layers. A graphic to describe this complete process is pictured in Figure 3-3.

Figure 3-3: Dry Transfer Process, Courtesy of Jing Li

3.2 Device Fabrication

Device fabrication is an extensive process, and much of the work for creating the desired split-gate geometry relied upon lithographic work. Jing Li was the individual who conducted all of our lithographic and deposition work. While I was unable to contribute in this regard due to my lack of training, I have outlined the general process in order to provide a clear picture of the complete fabrication steps involved in our device's construction. Electron beam lithography is a patterning technique that allows for a resolution on the order of nanometers [21]. In this process, a highly focused beam of electrons is fired at a material surface that is masked, or coated, with a polymer called a resist. Typically, the resist is applied uniformly to the surface of the material to be patterned via a high rpm spinning process, called spin coating [22]. Centrifugal force allows for a centered amount of resist to be spread evenly in each direction on the substrate surface as it spins at several thousand revolutions per minute. Resists come in two primary classes: positive tone and negative tone [21]. Both classes of resists undergo chemical changes when the electron beam ionizes the affected area that affect their solubility in certain solvents, however the nature of the change is what gives rise to their differentiation. Positive tone resists, such as poly(methyl methacrylate) (PMMA), that are patterned by the electron beam transition from low solubility to high solubility. Negative tone resists such as hydrogen silsesquioxane, or HSQ, transition from high solubility to low solubility when patterned by the electron beam [21]. Once the device has finished being exposed by the electron beam, it is placed in a solvent, known as a developer. This development process removes the high-solubility polymer area, and preserves the low-solubility polymer segments.

There are a variety of parameters that affect the outcome of patterning a resist: these range from beam energy and exposure time, resist material and thickness, and the developer used. All of these parameters work in concert to affect the resolution of the pattern [23]. Especially on the nanoscale, several processes serve to limit the resolution of the patterning. Two of the major limiting mechanisms are the proximity effect and electron scattering. The proximity effect is the consequence of beam

electrons depositing energy to areas adjacent to their initial collision site. Due to this effect, very small, dense patterns can sometimes suffer from overexposure. The second major limiting mechanism of electron beam lithography is electron scattering, both in the forward and backward direction [23]. When the incident electron beam strikes the resist, the electrons interact both with the resist's nuclei and electrons, forming a series of elastic and inelastic collisions respectively [23]. These series of collisions constitute an individual, random trajectory for each electron.

Laying metal contacts on the device also employs an electron beam, however the process is fundamentally different from the lithographic techniques previously discussed. Initially, an electron beam is applied to a target material, a metal in our case, within a vacuum chamber. Enough energy is applied to the material in this process to cause the metal to evaporate. This metal vapor is then free to adhere to the substrate, which is also present in the chamber; typically, the substrate is protected by a mask, so that only the exposed area accumulates the metal vapor, which then precipitates onto the desired contact regions of the substrate [24].

Chapter 4

Potential and Charge Density Distribution Simulations

This chapter focuses on the computer simulations of various split gate geometries that I constructed. It begins with an overview of the simulation design process. I then discuss the results of the simulations, and examine the differences in the electric field distributions as a result of changing the distance between the gates.

4.1 Simulation Design and Construction

Each of my simulations was created with COMSOL Multiphysics, a physics-oriented simulation software package. I was able to access this program via the Penn State's high-performance computing resources; all of my work was done via a virtual desktop I installed on my computer that allowed me to communicate with the Hammer computer system, which houses the software I employed. This subchapter will include a basic walkthrough of my simulation model construction and it consists of the following steps: defining the study, defining the geometry, assigning materials, meshing the model geometry, and computing the study.

When designing a COMSOL study, the first steps are handled through the Model Wizard. This tool loads on the starting screen, and allows for the selection of such things as dimensionality, the type of physics you wish to study, and the physical quantities you'd like to assign. In my case, I worked on a 3D model, studying electrostatics, with the ability to assign electric potentials. Once this was completed, I initialized my study, which opened a master panel and graphics window.

Once the master panel was available, I could create the desired geometry for my study. This involved working through a series of sub menus that were accessed via right-clicking the geometry tab

and finding the shapes I wished to construct. Each of these has individual parameters, such as position and dimensions, which are set individually as each one is created. A sample geometry for my split gate device is pictured in Figure 4-1.

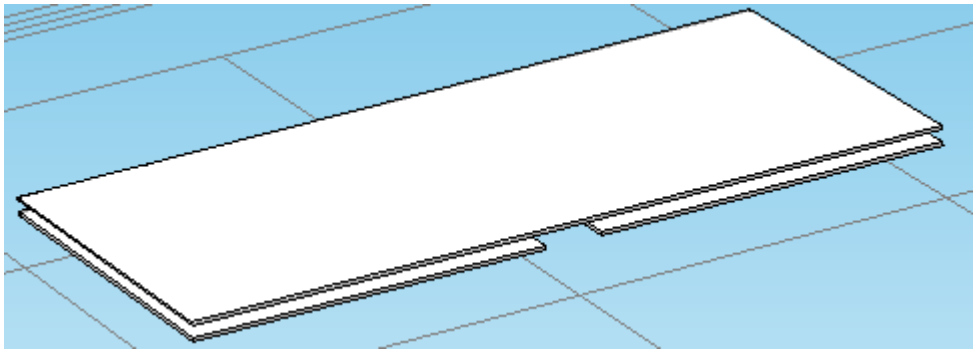

Figure 4-1: Example Split Gate Geometry in COMSOL

Once the split gate was constructed, and the entire structure encapsulated in a big cube that would become the ambient environment, I could assign materials. COMSOL has a built-in materials library that is quite extensive, and I made use of it in all of my studies. To assign materials, the Materials tab in the master panel had to be right-clicked, and each material individually added to the study. Adding materials opened a sub-menu, exactly like the geometry sub-menus, which allowed for assigning a material to the objects; this was accomplished with a simple left click when the object was highlighted by the cursor. Once each object was assigned a material, the software would check to see that all values relevant to the study, such as the dielectric constant in my case, were assigned. If this cleared, the study could move on to assign new values associated with the physics being studied; in my case, this was electrostatic potentials. This was exactly like assigning the objects their respective materials. The critical difference is that assigning materials affects a domain; this means the entire object. For assigning values of electrostatic potentials, object edges and surfaces were distinct from one another. This means that the model had to be manipulated in the graphics window in order to expose only the surfaces that were desired to have potential values while they were being assigned. Once everything was assigned the relevant values for the study, I was able to mesh the geometry.

Meshing the geometry is essentially the process that breaks the model into a set of finite, discrete components on which the software can perform its mathematical analysis. The Meshing submenu on the master panel allows for the level of fineness in the mesh; a smaller mesh size requires greater time and memory to compute, however it increases the resolution of the study in the same way more pixels allow for a sharper image on a screen. This could be a time consuming process, and for graphene simulations it is difficult to use anything larger than a very fine mesh, because the aspect ratio of very thin sheets requires high mesh resolution and therefore a long computation time. An example of my simulation geometry after a successful free tetrahedral mesh is pictured in Figure 4-2:

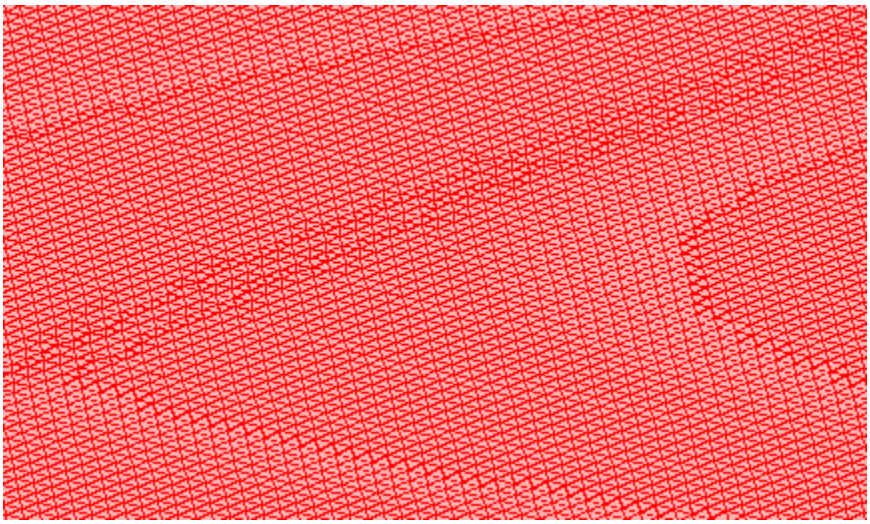

Figure 4-2: Example of Successful Mesh with Free Tetrahedrals, Close-Up of Top Plate

The final step after meshing was computing the study. This was as simple as clicking the study button on the master panel and clicking the compute button in the study submenu. Often, this step took at least as long as the meshing process. Once the study computations were complete, meaningful information can be gleaned with the post-processing tools built into the software.

The three models that I constructed adhered to this process outline. Each model consisted of three thin plates, all encompassed by a solid block that acts as an ambient environment between them. This simulation geometry is directly motivated by the split gate geometry of the bilayer device. The top plate, which is set with a potential of 0V, acts as the bilayer sample we obtained; the two bottom plates

resemble the graphite split gates and the space between the sample and gates is filled by the block that encompasses the plates, representing the boron nitride flake used in the transfer process which acts as a dielectric. The bottom two plates are set at 5V and -5V respectively, which is what creates the p-n junction within our bilayer sample as desired. The distance between the top and bottom plates was set to 30nm, which is a reasonable thickness for our boron nitride flakes obtained via mechanical exfoliation, and each plate was set to 10nm of thickness; the boron nitride dielectric had its relative permittivity set to $\varepsilon = 3$, which is in line with empirically obtained values. I used the extremely fine mesh, the smallest available, in order to maximize the resolution of my post-processing graphs.

4.2 Simulation Specifications and Results

I created three distinct split gate simulations, each with a different gap distance between the bottom gates: 30nm, 90nm, and 150nm. Once I computed the studies, I went on to examine the electric potential distribution very close to the split gates, as well as the charge density distribution along the top plate. Each data set that I plotted was derived from a solid line cut that ran parallel to the plate surface being studied; the potential distribution is taken 1nm above the bottom plates, and the charge carrier density line cut was taken one nanometer below the top plate. I made composite graphs of the data, which include each of the three data sets, to highlight the differences in electronic characteristics created by changing the gap distance between the split gates; this can be seen in Figures 4-3 and 4-4. It is worth noting that by convention, electrons are considered the normal carriers in graphene research, and thus are often thought of as being positive; this is reflected in Figure 4-4, where the n-doped region of the top plate has a positive value for signed charge carrier density, and the p-doped region has a negative value for signed charge carrier density.

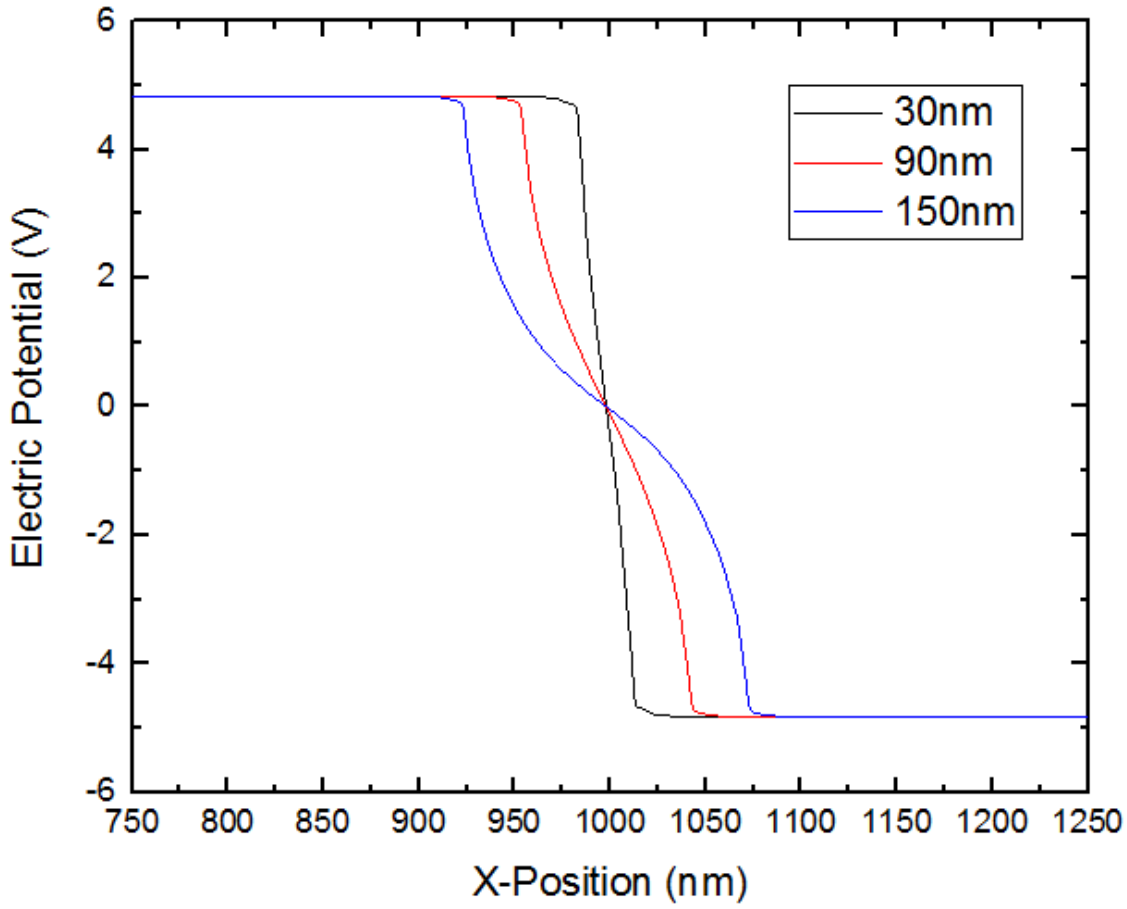

Figure 4-3: Electric Potential Distribution for Split Gate Geometries

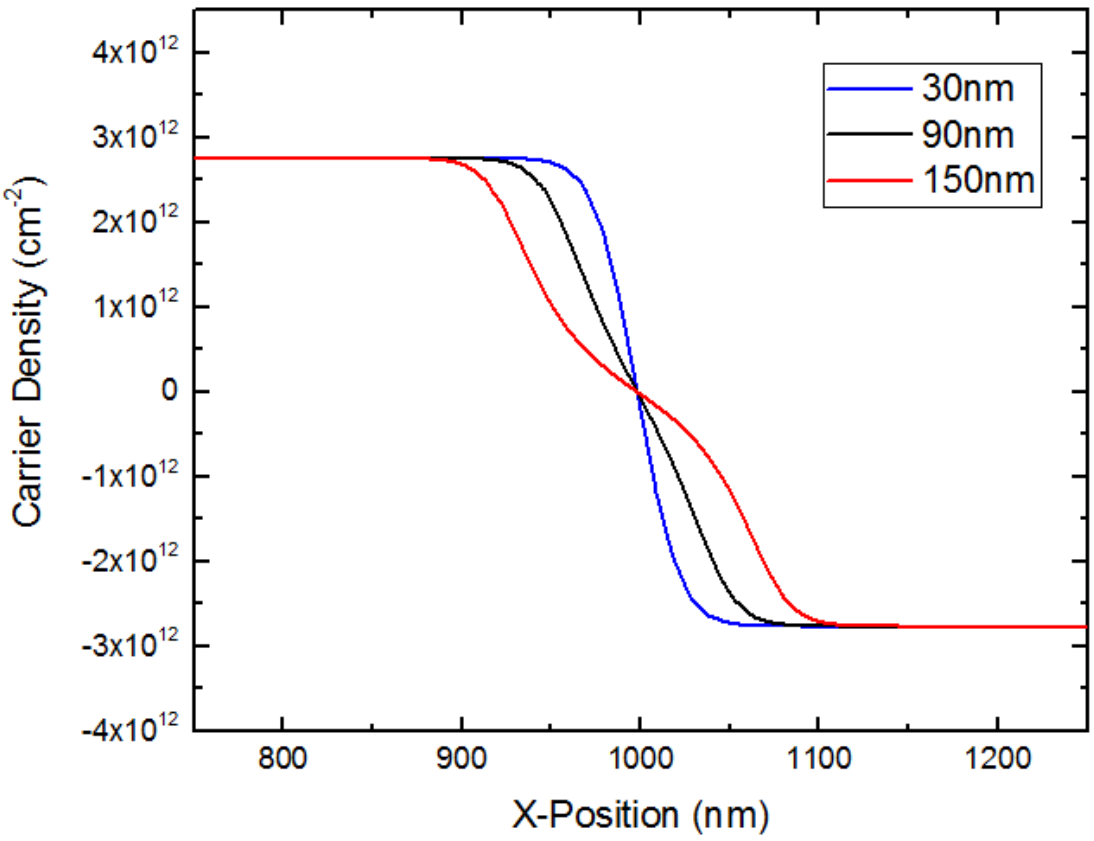

Figure 4-4: Charge Density Distribution for Split Gate Geometries

It is clearly evident that expanding the gap between the charged plates changes the distribution of several electronic characteristics of the model, which correspondingly illuminates the effect of gate distance on such quantities as charge distribution and potential distribution. This is useful information for our experiment, and provides insight into the nature of the region that, analytically, is not well described. To better illustrate the expansion of the region with a lower density of charge carriers, I constructed a plot of this distance as a function of the split gate gap size. I chose the point where the magnitude of the carrier density was at 90% its maximum value, which is relatively constant along the top plate at regions approximately 100nm horizontally distant from the edges of the bottom plates, and measured the distance in nanometers between these points on either side of the gap. This is pictured in Figure 4-5.

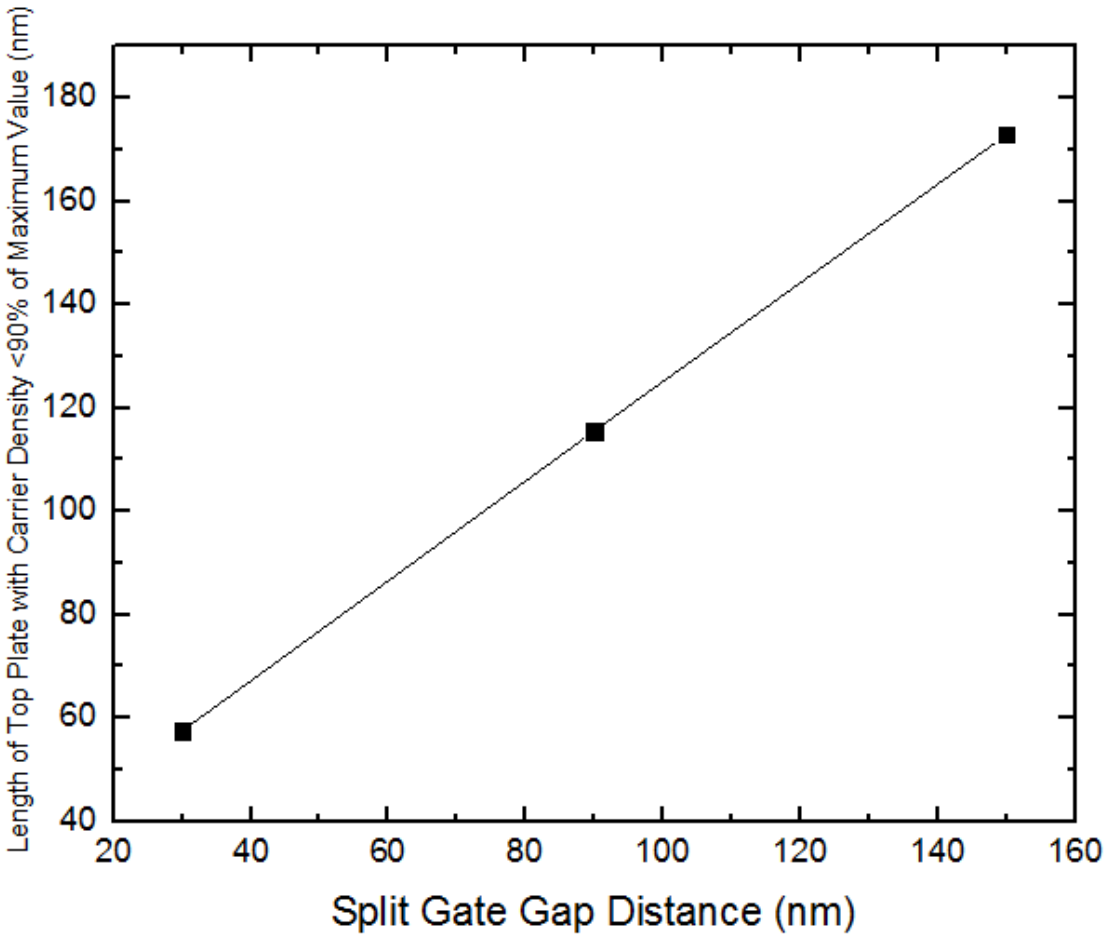

Figure 4-5: Region Length on Top Plate with Carrier Density < 90% of Maximum Value

To check the validity of the results, the charge distribution far from the gap was considered. Values of charge carriers per square centimeter, for these sorts of two dimensional materials, should be within a 10^{11} to 10^{13} range. A charge carrier concentration on the order of 10^{12} is what is predicted by the equation of capacitance for this configuration of graphene and boron nitride with our applied gate voltages. This is precisely the value computed by the study on the top plate at a reasonable distance from the split between the bottom gates. The voltage behavior is more easily seen to be quite reasonable, and fits expectations given the non-discontinuous transition from the region directly above the positively charged plate to the region directly above the negatively charged plate.

Chapter 5

Gate Roughness Analysis

This section discusses my initial work on gate profile analysis; it begins with the motivation for the work, discusses the obtaining a suitable image for analysis via atomic force microscopy, and concludes with the method I used to begin analyzing the images.

5.1 Motivation

This aspect of my research was a late addition, but non-trivial. The prevailing simplification in the analysis of data collected in the ballistic regime of charge-carrier transport is that the gate surfaces in devices are perfectly smooth. For a device with our gate geometry, it means that they are considered in the presence of no magnetic field to be perfectly normal to the potential barrier upon incidence. If the gate were not in fact smooth, but rough and with some non-zero average, angular offset, it would affect the charge carrier transmission results, as there is an established theoretical angular dependence for transmission rates [1].

5.2 Atomic Force Microscopy

In order to acquire gate profiles, an atomic force microscope, or AFM, was used. An atomic force microscope employs a nanoscale cantilever, which oscillates about its resonant frequency, to acquire topographical information about the object beneath it. The Van der Waals forces between the cantilever tip and the surface of the object beneath the tip cause variations in the resonance of the tip, which provides information to the software about the topography of the surface [25]. My work used the non-contact, tapping mode to image the surface of a graphite gate that was typical among graphite gates employed in the research conducted within my lab group. In order to obtain the images, I used the AFM

to image the entire gate, at several microns scale. This allowed me to establish the spatial coordinates of every point on the gate, so I could zoom in on specific areas with precision at will. Once I found the edge of the gate from which carrier were transported, I used contact mode to remove residual contaminants that were evident. I proceeded to image several $700nm^2$ spans along the edge to find the cleanest area. After progressively taking smaller and smaller area images, I finished by scanning the edge at approximately $350nm^2$ as this seemed to be both above noise level and contain sufficient data points for analysis. I proceeded to take several scans at this resolution, adjusting the angle of the scan to try and make the image of the edge contour horizontal; I did this to simplify my later analysis by not needing to account for an angle imparted to the data from the scan itself. This final scan provided a clear image of the edge contour of the graphite gate, which was clearly jagged.

5.3 Gate Profile Processing and Analysis

Once a suitable AFM image was obtained of the gate region, I needed to extract the coordinate data of the contour so that I could analyze it directly. This proved to be at least as difficult as obtaining a good image. Using a built-in function of the AFM software, I was able to extract a layer of data from my image that corresponded to the height value at each point in the scan. This data could be directly input into OriginLab graphing analysis software. I then needed to convert the data into a matrix, which is an Origin feature, and set the physical dimensions of the matrix to match those of the image.
Once the matrix was created, I created a topographical height map, pictured in figure 5-1.

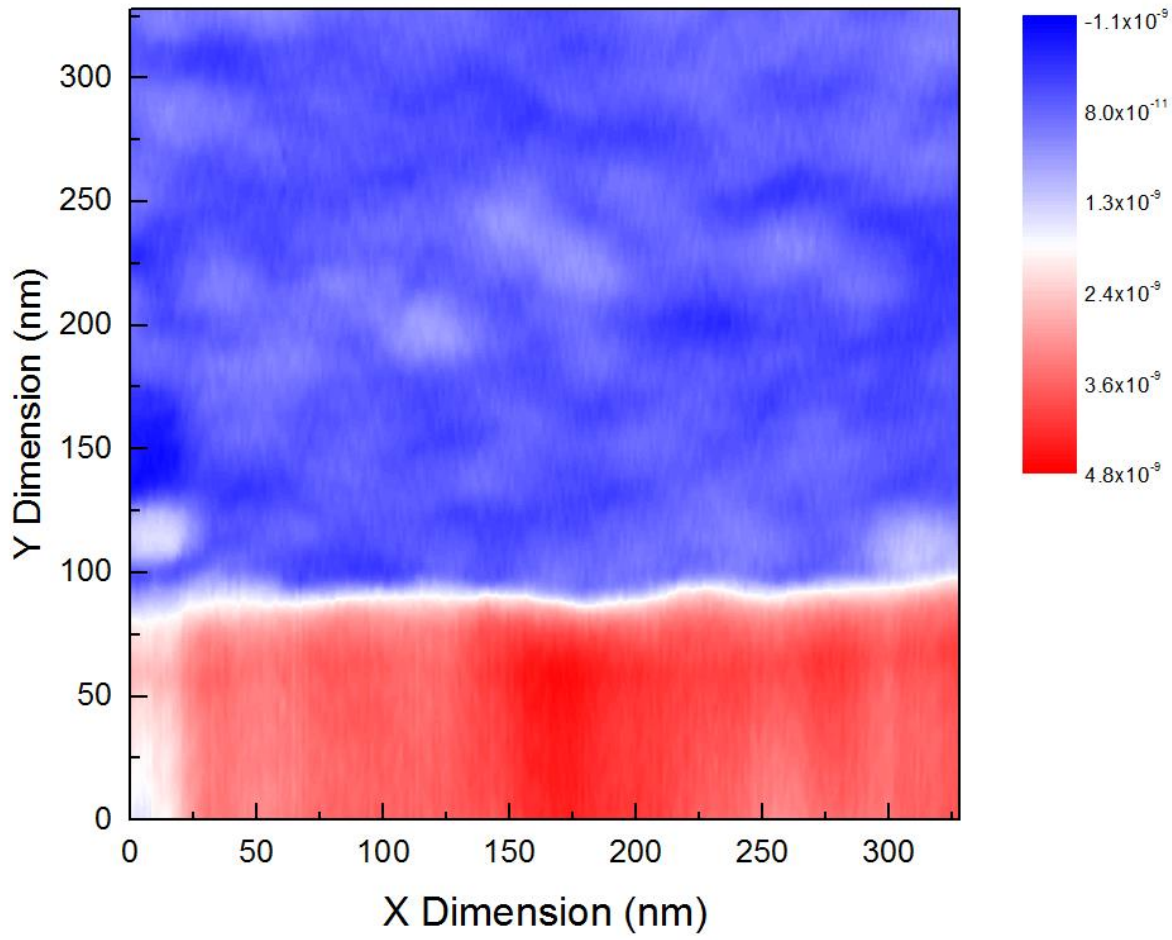

Figure 5-1: Topographical Height Map of Edge Contour

This allowed me to observe various contour lines at different uniform heights along the edge; chose the middle contour line along the edge profile, that of the 1.85×10^{-9}m height marker, corresponding to the white edge in Figure 5-1. It was reasonable to assume that halfway between the highest and lowest points of the edge contour, there was a true representation of the edge profile for the gate. I extracted the coordinates of this curve, and plotted them separately. I was able to smooth this extracted edge profile to reduce the noise associated with high resolution, small area AFM scans. I took the derivative of each point along the curve, and then calculated the arctangent of the derivate of each point. As the derivative is analogous to the tangent at each point along the curve, taking the arctangent allowed me to find the angle from normal to the gate surface in radians at each point. I converted these angles from radians to

degrees, which I used to create a frequency plot. This plot groups the angles along the edge contour into increments and counts their frequency and is shown in Figure 5-2:

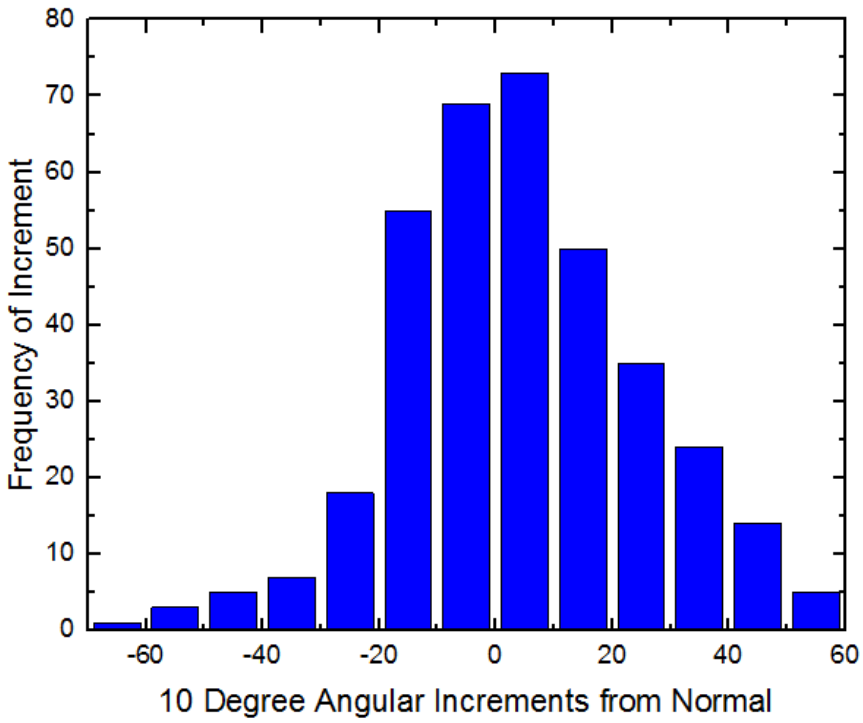

Figure 5-2: Frequency of Angles Occurring in 10° Increments Along Edge Contour

It is evident that the edge of the gate is not smooth, and that the angles are not symmetrically distributed around 0°. While angles within -10° to 10° of a line normal to the surface of the gate were the most common, the distribution shows that there is significant deviation from the simplification that a gate edge can be considered perfectly smooth. Regarding the implications of this result for experiments such as ours, there would be an explanation for deviation from 0% transmission of charge carriers when no magnetic field was applied. Referring back to Figure 2-7, there is almost 100% transmission for electrons incident upon the potential barrier at 30° from normal. On the gate I analyzed, 30 degrees is represented non-trivially; this could result in observing a transmission rate that seems to contradict the model. This is a relevant consideration, and may need to be accounted for when conducting future studies.

Chapter 6

Conclusion

This chapter summarizes the results of the experiment, describes the role of my simulations and analysis in shaping the current project, and ends with a brief outlook on future research.

6.1 Conclusions

While the data collection process is still ongoing for the device, preliminary tests suggest that it will not be usable for our intended study, due to its inability to exhibit the characteristic patterns that indicate the location of the charge neutrality point, which is analogous to the Dirac point in monolayer graphene. This charge neutrality point should manifest itself by the appearance of regions of high and low resistance as the split gate voltages are swept between positive and negative values, each sweep occurring while the other gate is held constant. These regions should form a plus sign type region of high resistance that establishes quadrants on a composite graph. Our data is pictured in Figure 6-1.

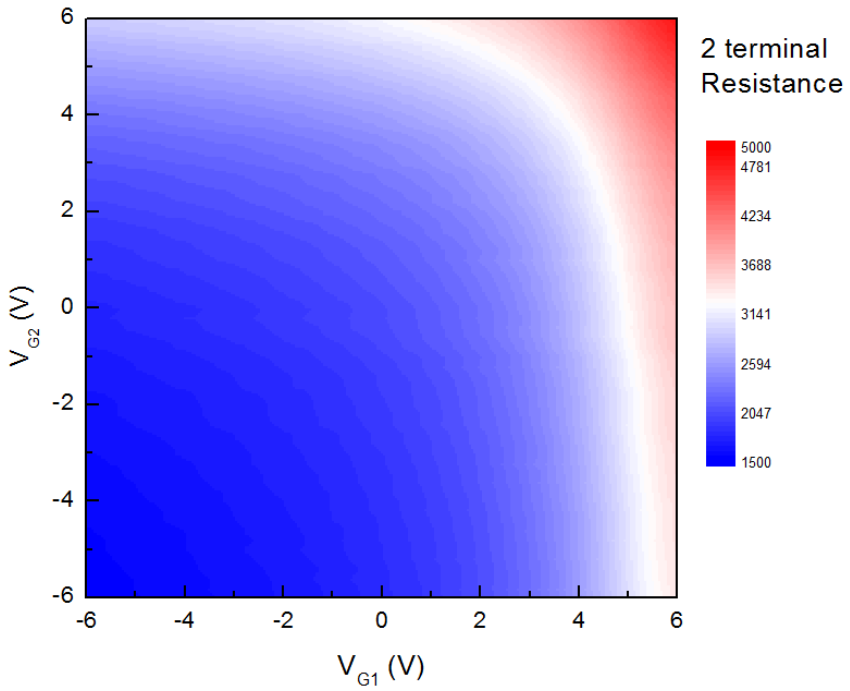

Figure 6-1: Gate Voltage Sweeps and Terminal Resistance Plot of Bilayer Device

It is evident from Figure 6-1 that only one quadrant was observed. Without observing a charge neutrality point and the four quadrants, we can conclude that we aren't establishing a proper p-n junction.

Still, my simulations and gate edge analysis are useful for future research; both of them illuminate the nature of split gate devices; the simulations provide computational solutions for comparison with theoretical predictions and potential results, and the gate analysis is relevant for interpreting the transmission rate measurements that might initially seem to contradict theory predictions. Additionally, we can conclude that 30nm is an adequate split gate gap distance for establishing a relatively sharp potential drop, which is required for our work. We also know more about the nature of the depletion regions we could establish as a function of split gate gap distance. Finally, we know that the simplification of perfectly smooth gate profiles is an approximation that may need to be accounted for, due to the pronounced angular distribution and its subsequent potential impact on transmission rates.

6.2 Current and Future Work

As mentioned previously, tests are still underway on the device to determine if it can serve some function beyond that of testing transmission rates of electrons incident upon a potential barrier. Another device will likely be constructed and examined in the future, in order to test the theory predictions that initially motivated the work. This repeated experiment would take into account my simulation results, regarding expected charge carrier concentrations and the electric potential distributions of various gate geometries. Additionally, more research could be done regarding gate edge roughness, such as comparing gate edge contours of different lithographic recipes. The assumption of perfectly smooth gate edges is common in analysis of data in similar experiments, and a greater understanding of the role rough gate edges play in transmission rates would be a worthwhile avenue of inquiry.

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