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ASSESSMENT OF SURFACE DAMAGE OF SILICON UNDER LASER PROCESSING FOR USE IN PHOTOVOLTAICS

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ABSTRACT

The integration of laser processing techniques in solar cell production holds enormous potential enhancements in both cell performance and manufacturability. However, with all the potential benefits, there are also downsides. This thesis focuses on examining the surface electrical damage that occur after laser processing has taken place over a given area, under various power and frequency levels. This is done by examining the current-voltage characteristics of surface barriers formed by Schottky metal deposition. The change in Schottky barrier height of the samples is evaluated for a qualitative assessment of surface damage and general trends in behavior are noted. This thesis is designed to offer insight into the surface lattice damage effects and investigate the causes of the Schottky barrier height alterations. Ultimately this work will add to the knowledge of how lasers impact solar cell performance and efficiency within the photovoltaic industry.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

Recently, the need for alternative energy sources to counteract the depleting fossil fuel resources has generated a rapid increase in research and development in the field of photovoltaics. These efforts have given rise to major improvements in photovoltaic efficiencies and manufacturing technologies, specifically in the silicon solar cell industry. However, there is still much room for improvement, in particular with the manufacturing processes.

Implementing laser technology to aide in the manufacturing process holds enormous potential to benefit photovoltaics. Lasers offer a non-contact way of transferring power and heat to the wafers *in very specific locations* at high intensity levels. Additionally, lasers offer a wide variety of applications including cutting, scribing, drilling, doping and alloying.

However, in addition to the benefits which lasers have to offer, there are also several potential consequences. Since the laser heats up the surface of the processed material, the surface atoms are melted and when they re-crystallize, they do not form as accurate of a lattice structure as that which was originally grown, creating lattice defects. The defects then result in electrical damage of the cells.

The ideal way to measure the electrical damage at the surface of a semiconductor is to create a Schottky barrier on the cell. Schottky barriers are formed when metals with an appropriate work function come into contact with a semiconductor. The result is that the Fermi levels of both the metal and the semiconductor equilibrate, and a potential

barrier is created between the materials. This barrier makes it more difficult for electrons to travel to and from the semiconductor for n-type materials, and it applies to holes for p-type materials. It can be observed through non-ohmic current-voltage behavior at sufficiently low voltages.

This thesis serves as an investigation into the electrical damage which can occur at the surface level of Silicon wafer cells which have been subjected to laser processing. Ultimately, these results may have use within the photovoltaic field, particularly in the fabrication of Si solar cells. Any electrical damage created at the surface level may have an impact into the cell's overall efficiency which is why the subject material should be studied.

CHAPTER 2

LITERATURE REVIEW

Introduction to Photovoltaics

The photovoltaic effect was first discovered by Alexandre-Edmond Becquerel in 1839 with his research of electrolytic cells. [1] However, it was not until over a century later, in 1955, that researchers at the Bell Telephone Laboratories created the first Si photovoltaic cell that used sunlight to generate electrical power. [2] Unfortunately the realization of economically viable photovoltaic cells has remained a difficult challenge. High costs and low energy conversion efficiency have continually plagued the industry, but with the increasing threat of global warming, and inevitable decline in the quantity of non-renewable energy sources, greater emphasis has been placed on improving solar cell performance and manufacturing techniques.

Solar energy has an enormous potential to solve many of the global energy needs. The sun provides a continuous source of energy with a spectral distribution approximating that of a blackbody at around 6000K. About 28% of this energy actually reaches Earth; and of this, only 18% is absorbed while the remaining is scattered by the atmosphere. [1] Most of the ultraviolet rays and X-rays are scattered within this region. [1] Additional losses occur when photons from the sun come in contact with molecules within the air and are absorbed. These loses are most potent when the sun moves lower in the sky, allowing the light to pass through a greater thickness of air and hence losing more energy.

History of Photovoltaic Power Generation

The photovoltaic industrial development can generally be broken down into three major generations. The first and earliest generation involved photovoltaic cells from mono and polycrystalline wafers cut from ingots. These cells were quite thick (100μm - 300μm), with relatively high energy conversion efficiencies (within theoretical limits) but were extremely costly due to the large amounts of high-quality crystalline silicon used. [1] The next generation sought to eliminate some of the major costs by creating thin film single layer cells. These new cells were only 1-10μm thick, thereby offering dramatic reduction in material usage and cost, but as a tradeoff, the corresponding efficiency values were also lower. [1] The third generation, and the current one, is attempting to create a balance between the greater efficiency of the first generation, and the lower cost of the second. One way this is being done is by using thin-film tandem cells. Tandem cells are multi-layered cells, which consist of materials with varying energy gaps, allow for a greater overall absorption of the solar spectrum. [1]

There are several factors which contribute to the relatively low efficiencies of solar cells. Reflection losses at the surface and incomplete absorption of the varying photon energies contribute the major loses, that are rather fundamental; however, there are also losses associated with incomplete collection of photo-generated electron hole pairs and internal series resistance. [1] Series resistance reduces the short-circuit current, which in turn reduces the maximum power available from the device. [3] It is because of these reasons that the theoretical maximum efficiency and the experimental efficiency differ. To decrease this discrepancy, direct band gap semiconductor materials should be chosen with an energy gap between 1.1 and 1.7eV for peak efficiency. [1] Additionally

stable materials with lower recombination times and easy fabrication methods should be chosen.

Design Principles of Photovoltaics

The general goal of a photovoltaic cell is to harness and convert the energy from the sun into electrical current that can be used to power a load. Typically, semiconductors such as silicon are used and large-area p-n junctions are formed. In such a junction, there is a natural built in electric field, as shown in Figure 1. The n-type corresponds to the negative charge arising from the abundance of electrons, whereas the p-type contains an abundance of positively charged ‘holes’.

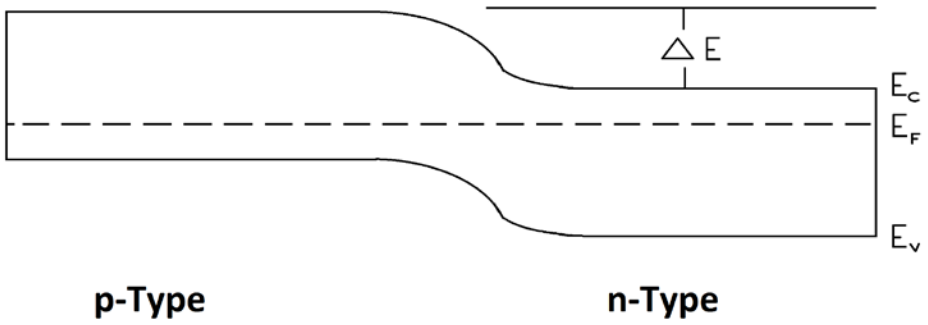

Figure 1: p-n Junction Formation of a Semiconductor

When the two different types of doped semiconductors are joined together, an interesting phenomenon occurs. Since thermal equilibrium dictates that the Fermi level remains constant throughout the junction, band bending occurs in both the conduction band and the valance band. This bending results in some of the excess electrons from the n-type material to flow into the p-type; and correspondingly, holes from the p-type material move in the opposite direction towards the n-type. This charge-exchange process creates a built in electric field at the junction, and it is ultimately this electric field which gives rise to a photovoltage under illumination. [3]

The photovoltaic cell design exploits this built in electric field and the charge-exchange process. Here, the p-type region of the cell faces direct sunlight, and incident solar photons are either reflected or absorbed. In order for a photon to be absorbed in an efficient manner, it should have the proper wavelength with its corresponding energy. If the energy of the photon is equal to or greater than the semiconductor energy bandgap level, then the photon is absorbed. [3] This absorption allows an electron in the p-type material to excite itself from the valance band to the conduction band. From here, the electron is transported by the electric field to the opposite side. The result is that the electron flows from the p-type to the n-type material, generating a current flow. Similarly there will be a transport of photogenerated holes from the n-side to the p-side. This flow of electrons and holes is translated into direct current and can then be used to generate electricity and power a given load. [3]

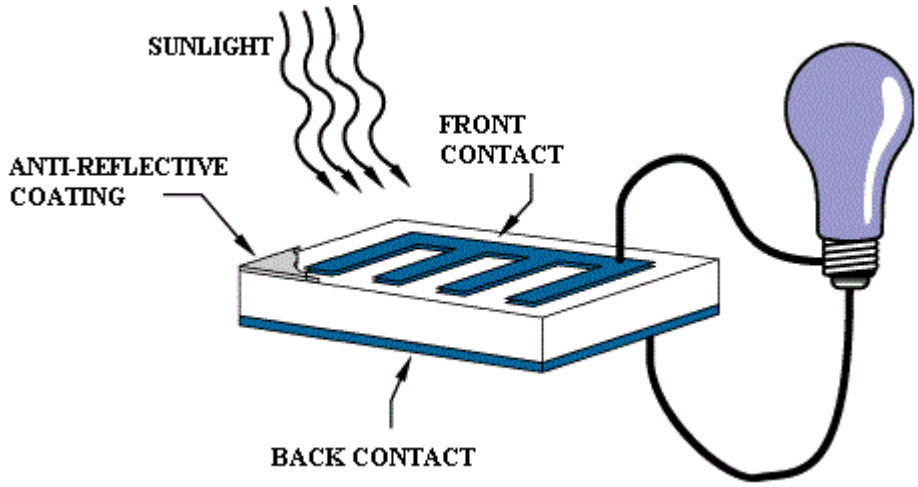

Figure 2: Solar Cell Load Representation [4]

The current and voltage generated from a single solar cell are quite small; therefore, in practice, a number of cells are electrically connected in series-parallel in order to increase the current and voltage. These cells are mounted together in a support structure called a module and each module is designed to supply a certain voltage. [4] However, it is important to realize that the current produced by the system is directly dependent on how many absorbable photons strike the module, not just how many cells there are within the system. Modules are they typically wired together to form a large array to produce any desired current and voltage combination.

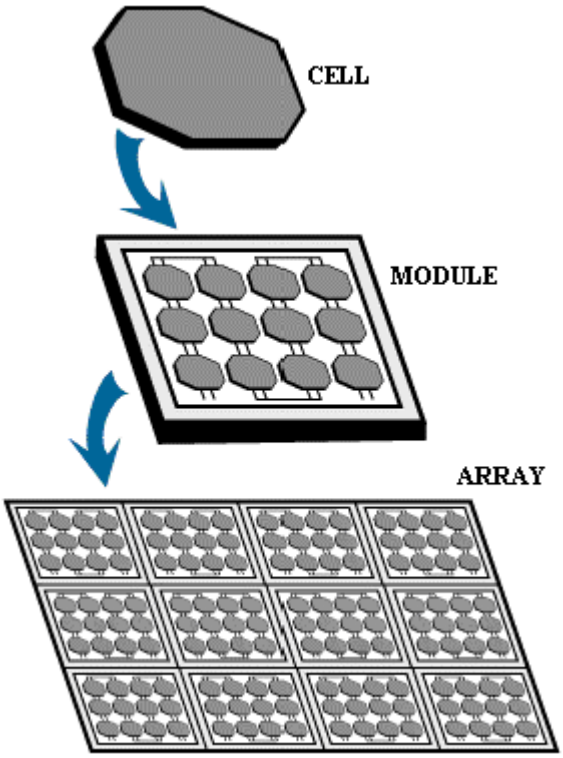

Figure 3: Solar Cell, Module, and Array Diagram [4]

Solar Cell Resistance Limitations

Solar cells have internal resistances that limit the maximum power that can be achieved. These are the bulk series resistance r_{series} of the semiconductor, and is the shunt resistance r_{shunt} arising from edge or surface leakage. To get the maximum power, r_{series} should be minimal and r_{shunt} should be very large (Figure 4).

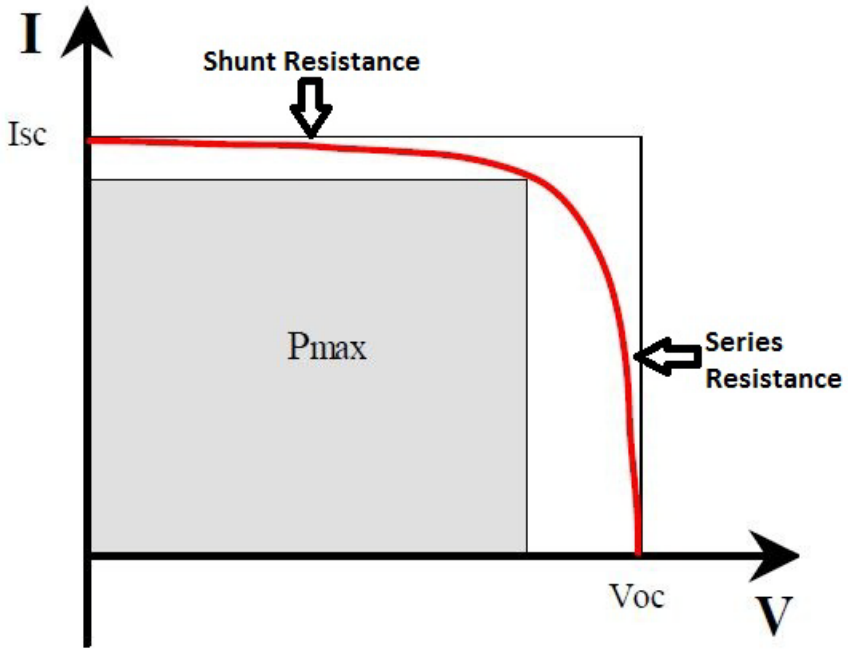

Figure 4: Current-Voltage Curve of a Solar Cell [5]

Since series resistance is the most common limitation of the cells, it is important to determine its value. The requirement on the series resistance is commonly approximated by the formula: [5]

$$r_{series} < \frac{0.8}{X}\Omega$$

for 1 cm^2 area cells, where X is the solar concentration. Under normal operating conditions, anywhere in the range of 10-20% of the maximum power available is lost due

to series resistance. [5] Additionally, the series resistance has a dependence on the cell current, causing r_{series} to have deviation between inactive and operating conditions. There are several methods that are used to determine the series resistance and in general, they are neither simple to implement nor interpret.

The second type of limiting resistance is shunt resistance. This happens when shunts are present throughout the material, consequently reducing the load current. [5] The physical value of this resistance can be determined by curve-fitting approaches. On most semiconductors, this is found from the slope of the reverse-biased current-voltage characteristic before breakdown. However, for solar cells, large reverse currents are often present well before the breakdown voltage simply because the cells are not designed to be operated under such reverse conditions. [5] This makes it almost impossible to obtain reasonable values for the shunt resistance; therefore alternate methods of curve extrapolation must be used. A common approximation is to determine the resistance under low light intensities where the series resistance is negligible compared to the shunt resistance ($r_{series} << r_{shunt}$). In this case, the shunt resistance is approximated by the formula:

$$r_{shunt} \approx \frac{V}{I}$$

at low currents. [5]

Schottky Barriers

The metal-semiconductor contact is one of the oldest semiconductor devices, having been studied or in use since the 1870s. [6] However, the physics of operation of the device was not fully understood until the 1930s when Schottky (along with Spenke and others) developed the first acceptable theory. [6] In his honor, these devices are frequently referred to as Schottky barrier devices.

A metal-semiconductor contact can display two distinct types of behavior: ohmic or Schottky barrier. Ohmic contacts have linear current-voltage (I-V) characteristics (ideally vertical lines corresponding to zero resistance) whereas Schottky barrier devices serve as rectifiers due to their highly nonlinear I-V (ideally zero resistance in the conducting direction and infinite resistance in the other). The work function of the two materials is the determining factor as to which of these characteristic behaviors the device will display. If the work function of the metal is less than that of the n-type semiconductor, $\Phi_M < \Phi_S$ an ohmic contact is made. If the opposite is true and $\Phi_M > \Phi_S$, a Schottky barrier is formed and the barrier height after contact for the given model (assuming intimate contact and no interfacial layer) is given by the formula:

$$\Phi_B = \Phi_M - \chi$$

Where χ refers to the electron affinity of the semiconductor and is defined as the potential difference between the vacuum level and the bottom of the conduction band. [6] A key concept to note is that the barrier height is independent of the doping concentration of the semiconductor and instead only depends on the physical parameters of the semiconductor and metal. [6] Diagrams of the work function definitions are shown in Figure 5:

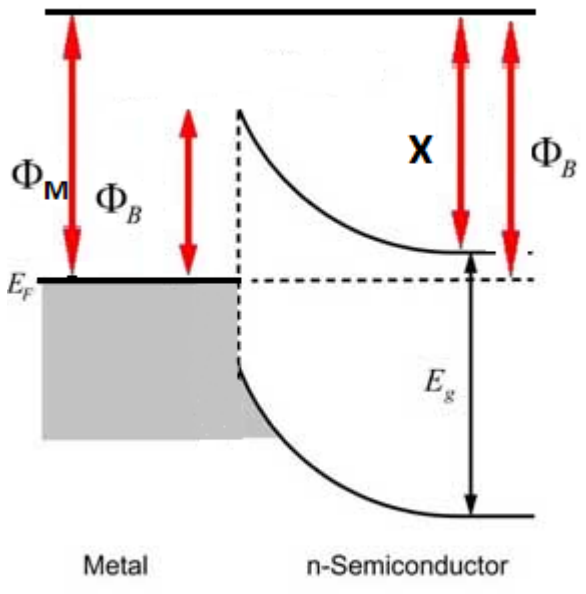

Figure 5: Definitions and Parameters of a Metal and n-type Semiconductor Junction [6]

To form a Schottky barrier on a p-type semiconductor, the exact opposite conditions must occur to that of the n-type. This device creates the barrier for the holes, therefore the work function of the metal must be less than that of the semiconductor: $\Phi_M < \Phi_S$. A diagram of the Schottky barrier is shown in Figure 6. If the work function of the metal is larger than that of the semiconductor; the device will behave with ohmic I-V behavior.

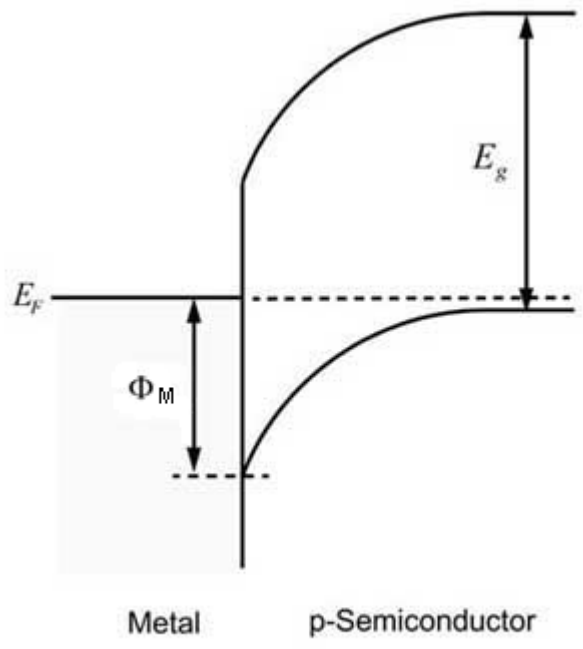

Figure 6: Schottky Barrier Height for a Metal and p-type Semiconductor Junction [6]

Returning to metal-semiconductor with n-type material, the important difference to note is that for ohmic devices, electrons traveling from the semiconductor to the metal have no potential barrier to overcome. Hence they have linear current-voltage dependence. Conversely, for the Schottky contact, there is a barrier height. Electrons in the conduction band of the semiconductor must gain additional potential in order to move from the semiconductor to the metal. This is brought about by applying to the n-type semiconductor a negative voltage which lowers the energy barrier for electrons and causes their emission into the metal, with a positive voltage, the barrier increases further and only a small leakage current flows. [6] This asymmetry in I-V characteristics is what makes the Schottky contract rectifying.

Barrier Height Measurements

There are a few different methods to measure the barrier height of a Schottky diode. The most common method used is to measure it from the current-voltage characteristics. According to the thermionic emission model that is applicable to most Schottky barriers on commonly used semiconductors, the current density J is given by

$$J = J_0(\exp(\frac{qV}{nkT}) - 1)$$

where J_0 is the reverse saturation current density given by

$$J_0 = A^{**}T^2 \exp(\frac{-q\Phi_B}{kT})$$

Φ_B refers to the Schottky barrier height. n is the so-called ideality factor, slightly greater than unity, that arises from a number of factors including image force and interfacial layer. [7] Additionally, the term A^{**} refers to the Richardson constant and is a property of the semiconductor. If A^{**} is known, the value of J_0 immediately gives the effective barrier height. J_0 is found by extrapolating a logarithmic plot of the log of the current versus voltage. [6] The location where the linear portion intersects the y-axis is the J_0 term and subsequently the barrier height can be easily determined. However, if A^{**} is not known, the current-voltage characteristics must be plotted over a range of temperatures. From here, $\log\left(\frac{J_0}{T^2}\right)$ is plotted against inverse temperature to yield a straight line, with a y-intercept equal to $\ln(A^{**}) + \frac{q\Phi_B}{k}$. This method is used to give the barrier height at absolute zero. [7]

A second way to determine the barrier height is from the photoelectric methods. If radiation with quantum energy which is greater than the barrier height is come into contact with the metal, electrons are excited from the Fermi level of the metal will have sufficient energy to cross into the semiconductor. [7] Consequently, a photocurrent will register in the external circuit. The barrier height corresponds to the photon energy at the threshold for this current flow.

The third method to be discussed to measure the Schottky barrier height is through the capacitance measurements. Provided that the diode is nearly ideal and the semiconductor has uniform donor concentrations, the differential capacitance under reverse bias V_r is given for non-degenerate semiconductors by:

$$C = S(\frac{qN_d\varepsilon_s}{2})^{1/2}(\Phi_B - \xi + V_r - \frac{kT}{q})$$

Here, S is the area of contact, q is the charge, N_d the dopant concentration, ε_s the permittivity of semiconductor, and ξ is the energy difference between the conduction band and the Fermi level. [7]

If Φ_B is independent of V_r, then a plot of C^{-1} against V_r should yield a straight line with the intercept on the horizontal axis equal to $-(\Phi_B - \xi + V_r - \frac{kT}{q})$. The barrier height is then extracted using the equation

$$\Phi_B = V_1 + \xi + \frac{kT}{q})$$

Where V_1 is the horizontal intercept. [7]

Background of Laser Science

The word “laser” is actually an acronym which stands for “Light Amplification by Stimulated Emission of Radiation”. [8] Lasers have found applications in a variety of modern industries including electronics, science, medicine, and engineering. What makes a laser unique is its ability to concentrate light at very high intensities in a single direction. This laser source emits highly coherent electromagnetic radiation in beams of extremely low divergence. [8]

A laser makes use of processes that increase and amplify previously generated light signals. This amplification is brought forth through stimulated emission and optical feedback. [8] Thus, a laser must consist of a gain or amplifying medium and a set of mirrors which are designed to feed the light back into the amplifier for continued growth of the beam. [8] This medium may be in the form of a solid, liquid, gas, or plasma. The mirrors are located in the resonator cavity and one of the mirrors must be a partially transparent output coupler which allows for controlled emission of light from the cavity. [8] Additionally, a laser must contain a pumping device which is typically either a flash lamp or another laser. [9]

The first step towards laser emission occurs when the gain medium absorbs energy from the pumping device, which in turn pushes electrons into excited quantum states. [9] From there, light is emitted through either spontaneous or stimulated emission. There are two requirements for continued laser emission: Population inversion and light amplification. [8] Population inversion implies that the number of electrons in the excited state is larger than that of the lower energy state. Light amplification implies that the

quantity of stimulated emission due to light passing through the gain medium is greater than the quantity that is simultaneously being absorbed by the said medium. [8]

In addition to being quite powerful, the laser device has a wide range of properties that enable applications as diverse as optical communications, surgery, printing and material processing. The wavelengths of lasers have been known to range from the far infrared part of the electromagnetic spectrum (1000μm) to the soft x-ray region (3nm). [8] Laser power extends over an enormous range - from 10^{-9} to 10^{20} W - and may have pulse energies as high as 10^{4} Joules with pulse durations as short as 5*f*s. [8] Lasers generally have a narrower frequency distribution, or much higher intensity, or a much greater degree of collimation, or much shorter pulse duration than that available from more common types of light sources.

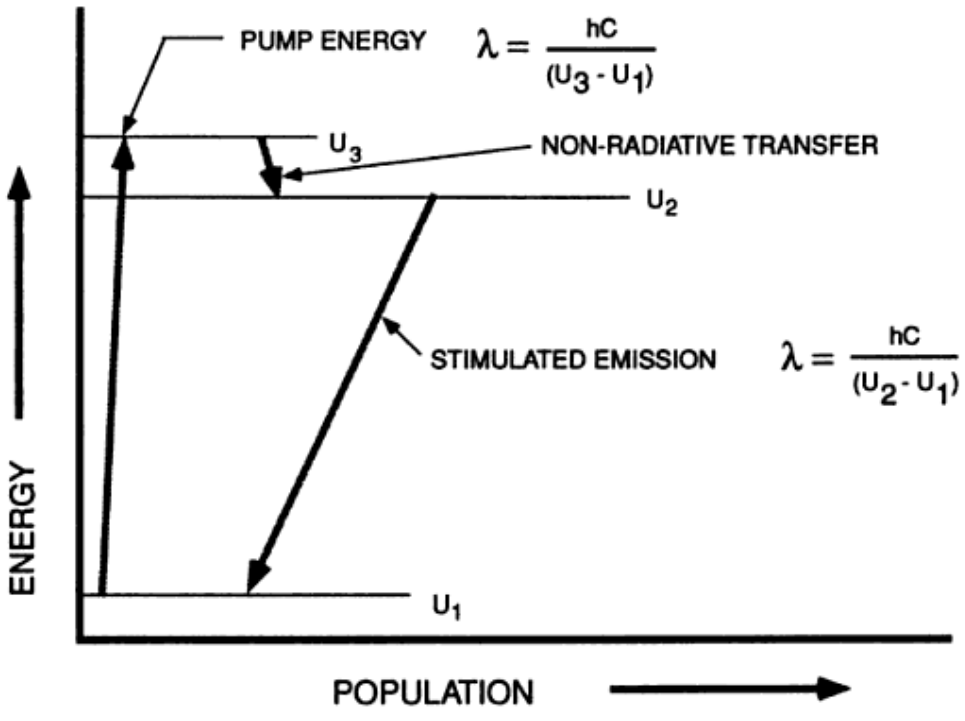

Figure 7: Transition in a Three-Level Laser [8]

Nd: YAG Laser

The Neodymium-doped yttrium aluminum garnet laser is a member of the solid-state laser group. Solid state lasers have a crystalline solid medium with ions doped inside it to provide the necessary energy state conversions. [8] Neodymium, a rare earth metallic element, is a popular dopant for these solid state lasers. This is due to the fact that Nd incorporates a four-level energy system and consequently has lower pumping threshold. Additionally, population inversion is able to be maintained because the upper laser level lifetime is relatively long, approximately 230μs. [8] The emission gain linewidths is 0.45nm. Neodymium has multiple energy bands located within the solid at levels within the range of 1.56 electron-volts (eV) and 2.32 eV. Photon emission occurs when an electron drops from the upper level of 1.38 eV to the lower level of 0.22 eV which corresponds to a wavelength of 1064 nm. [8]

The physical makeup of the laser is designed around a neodymium doped yttrium aluminum garnet rod which is surrounded by either a pump lamp filled with noble gases such as xenon or krypton, or a diode laser, which improves efficiency and optical performance. [8] During use, thermalization of excited carriers heats the YAG rod and consequently, it is necessary to cool the rod by flowing water. This thermalization occurs when the rod is in a metastable state where energy loss through non-radiative transitions cannot occur. [8] Spontaneous radiative emission is also highly unlikely within this metastable state. Because of this, the Nd atoms are able to remain in this state for long periods, further helping maintain population inversion. More efficient pumping is achieved when the rod is not overheated. If the rod overheats, it produces a large thermal

gradient between the inner core and the outside. This gradient alters the refractive index of the material which in turn lowers the optical performance stability and ultimately creates a divergent output. [8] To counteract this, pumping with diode lasers is common practice because it slightly alleviates the problem by reducing the amount of heat the rod must dissipate.

In addition to the natural frequency Nd: YAG laser, there are also commercially available frequency-doubled, frequency-tripled, and frequency-quadrupled versions which correspond to wavelengths of 532 nm, 355 nm, and 263 nm. This manipulation in frequency is done through a process of nonlinear frequency conversion. For example, frequency tripling is usually a cascaded process achieved by first frequency doubling the input beam and then performing sum frequency generation until the desired frequency is achieved. [8] These frequency manipulated lasers are typically housed in a 0.5 m long rectangular structure with a separate rack-mounted power supply.

Nd:YAG lasers can operate in both pulsed and continuous wave emissions. The pulse shapes and duration can be controlled through manipulation of the input power; however, the pulse rates are typically below 200 Hz. [8] Pulsing can be preformed with Q-switching, a technique which requires either a mechanical or an electro-optical device to either permit or prevent optical oscillation. A simple example of such a switch is an internal shutter. When the shutter is closed, there is a continuous pumping of atoms into the metastable upper laser state. Upon opening of the shutter, an extremely high energy and short pulse drains the upper state. [8] The resulting pulse is of extremely high power and because of this; this technique is often used when material ablation is required.

As far as applications are concerned, Neodymium lasers are most versatile. In industry, they are commonly used in production lines for precision welding, drilling, contour cutting, and laser marking. Their appeal arises from the precision with which the energy can be focused into a very small spot. There are also medical applications in which a Nd:YAG is applicable for such as membrane cutting and cauterizing gastrointestinal bleeding. The frequency-doubled version of the laser is very attractive as a pump source for a tunable or mode-locked titanium sapphire laser. [8]

Laser Processing in Photovoltaics

Because of the unique characteristics of a laser beam, research has been focused to utilizing lasers processing to improve the fabrication efficiency of solar cells. Laser processing techniques are able to improve the phonon emission process. Additionally, there are noncontact process advantages from lasers along with precision advantages from the extremely focused beam with high power density. Laser cutting, scribing, drilling, doping, and alloying are some of the ways which the characteristics of a laser beam are used within the photovoltaic field.

Laser Cutting

Lasers are often used to cut deep grooves into materials whereby mechanical pressure is then applied and cleaving consequently occurs. [10] In photovoltaics, this cutting process is generally used to remove the edge regions and creating a higher quality cell. Problems may arise if the depth of the laser is cut too deep. Shunts, or unwanted short circuits between the diffused emitters, may occur. [10] This in itself greatly lowers cell efficiency. An easy method in preventing this is to process the material on the non-emitter diffused side.

Laser cutting is preformed by overlapping high energy laser pulses, forming a continuous groove. [10] The groove size is primarily controlled by the power of the incident power; the higher the power, the wider the groove. The most common laser cutting manufacturing process utilizes a gas-assisted laser. Here, the laser is used to melt away the material and a pressurized assist gas is used to force the molten material away from the process leaving behind the empty groove. [9]

Laser Scribing

Scribing is another laser-based operation in microelectronics as well as photovoltaics and is a process where the laser is able to scribe grooves into the material's surface by drawing the beam across it. These scribers are typically used to create contact grooves and in contrast to the cutting process, they typically penetrate the wafer only in tens to hundreds of microns range. [10] The process leaves ablated material both on the surface and within the groove itself. To remove these residual deposits, anisotropic alkaline etches are used.

Laser Drilling

Lasers may also be used to drill deep holes into materials by firing high-irradiance pulses. These holes may be either cylindrical or conical in shape; however solar cells generally perform better with conically shaped holes because there is a reduced potential for shading and there is improved plating. [10]

Laser drilling is best demonstrated through the emitter-wrap-through solar cell structure. Here, laser drilled holes are used to electrically connect the front surface emitter to the back surface. The advantage of this is that the front side emitter improves the internal collection efficiency whereby the front side grid reduces any losses due to resistance. The downside of this approach is that the screen-printed lines decrease absorption of the impinging light, and have poor aspect ratios, conductivities, and contact resistances. [11] It is estimated that losses due to grid obscuration, grid resistance, and poor emitter characteristics reduce the commercial cell performance by nearly 30% to that produced at laboratory scale.

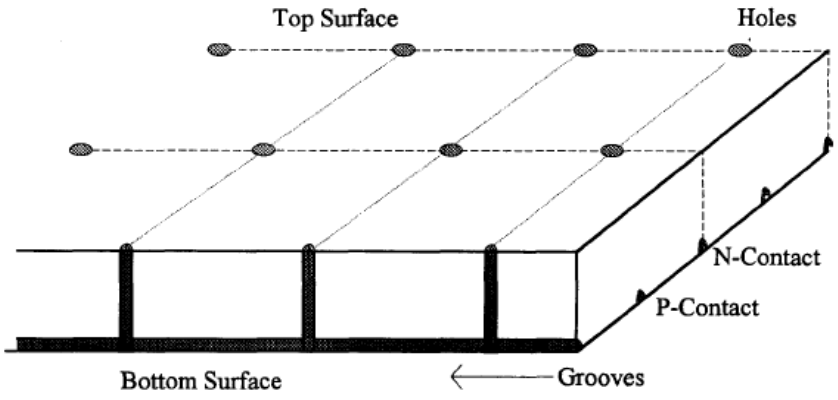

Figure 8: Diagram of Emitter Wrap Through Solar Cell [11]

The emitter wrap through solar cell is based on the buried contact cell process which has been shown to be potentially cost-competitive with conventional screen printed cells and has achieved energy conversion efficiencies between 18 – 21%. [11] There are two approaches for placing both contacts on the back of a solar cell. The first is by allowing photocarrier collection junctions and grids for both polarities to be located on the back surface. These photo-generated carriers are forced to diffuse to the back surface for collection into the back junction cells. [11] Clearly materials with a longer diffusion length are preferred over those with a short length. The second approach involves drilling "vias" through the substrate which allows the current collection grid on the back to contact the collection junction on the front. These vias are heavily phosphorous diffused and metalized which consequently reduce contact resistance and contact recombination. [11]

Laser Doping

The ability of the laser to focus high intensities at localized areas without causing the entire cell to be heated has applications within the doping field. Laser doping is able to incorporate dopants into semiconductors such as silicon while maintaining overall low temperature which results in less wafer warping and shortened carrier lifetimes. [12] The fabrication process of a doped wafer is preformed through laser technology by the use of low energy pulses. This prevents any material vaporization during processing. Unfortunately, the overall doping process is complex and the electrical performance is generally low. This is due to several factors including a lack of heavy diffusions, poor surface transmission, lack of effective anti-reflective coatings, and high recombination rates from laser processing. [10]

Laser doping has been able to successfully create selective emitters where there are specific heavily doped contact regions. [13] Experiments have yielded promising results with high shunt resistance and fill factors.

Laser Alloying

Alloying refers to the process where two or more metals are mixed together at the atomic level, creating a unique compound composed of various percentages of different metals. Diffusion of elements into other materials is a method of formation of such alloys and one way this is preformed is through laser processing. The traditional diffusion process involves annealing steps at well over 1000C in most cases. These high temperatures can create substantial electrical and structural damage to the wafers which correspond in decreased efficiency at the production level. [14] However, through laser firing, this alloying process is able to be extremely localized. The result is that laser can create highly precise alloys with unconventional shapes.

In particular, laser fired contacts within solar cell design are of particular interest in the alloying field. Here, the laser creates an alloy array of an aluminum-silicon alloy of which contains contact points on the rear surface of the wafer which result in local back surface fields that avert photocarrier recombination. [14] The point contacts and metal-semiconductor interface are typically sites of high recombination velocities and the back surface field acts to repel minority carriers from the area, which ultimately results in improved electrical performance of the cell.

Physical Phenomena Governing Barrier Height Alterations and Laser Processing

In past studies, laser processing has been found to alter the fundamental electrical characteristics of semiconductors. This is not a shocking result considering all the energy of a laser pulse focused on an extremely small area. Since laser processing is being explored seriously for solar cell manufacturing, it is necessary to assess laser damage effects on solar cell performance.

Surface Damage of Laser Pulse

As previously mentioned, lasers concentrate high amounts of photon energy onto an extremely precise location. Even when pulsed at lower energy levels, physical surface damage occurs at the surface. However, when dealing solar cells and semiconductors, precision is essential. The lattice structure of the wafers is specially constructed to have minimal defects and impurities within it.

To create semiconductor grade silicon, the oxide source material must first be reduced. This is a three step chemical process which starts out by producing metallurgical grade silicon by heading silica with carbon. [15] The reaction proceeds as follows:

$$C\,(s) + SiO2\,(s) \rightarrow Si\,(l) + SiO\,(g) + CO\,(g)$$

The next step involves purifying the metallurgical grade silicon through another reaction; however, in this case, a silicon-bearing gas known as trichlorosilane is formed. [15]

$$Si\,(s) + 3HCl\,(g) \rightarrow SiHCl_3\,(g) + H_2\,(g)$$

The final step in purification of the silicon involves allowing the trichlorosilane to react with hydrogen. This produces pure semiconductor grade silicon which is then used to make the semiconductor crystal. [15]

$$2SiHCl_3\,(g) + 2H_2\,(g) \rightarrow 2Si\,(s) + 6HCl\,(g)$$

After silicon has become pure, the physical growth takes place. The silicon is melted down and allowed to re-crystallize on a single seed crystal at a slow rate to allow for minimal lattice defects. [15]

With such care going into the growth of the semiconductors, physical laser damage on the surface can cause major problems. When a laser pulse comes into contact with a metal, the energy is translated into heat. This heat causes extreme high temperatures for small fractions of a second. Figure 9 shows an example of the temperature distribution gradient resulting from a laser pulse processing.

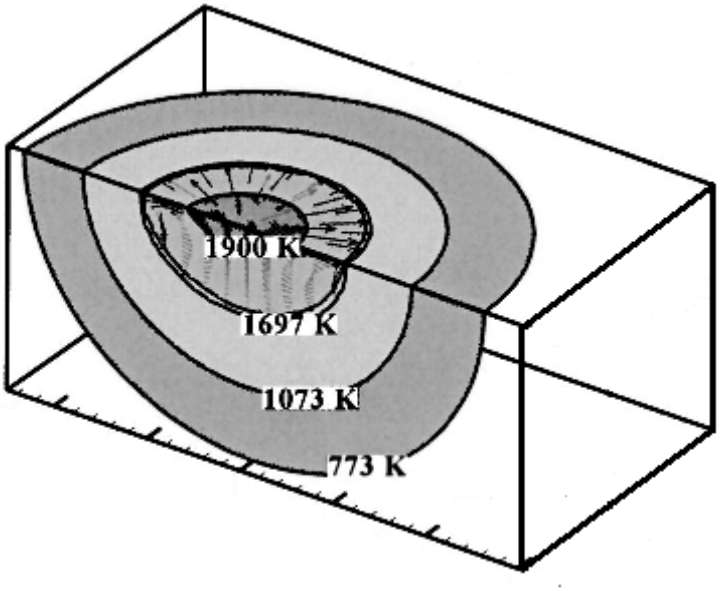

Figure 9: Example of a Temperature Gradient Resulting from Laser Processing [16]

With these high temperatures, some of the metal is sublimed from the crystalline solid phase into an evaporating vapor. Even more so, a layer of the solid is melted and moved into the liquid phase creating plasma. Once the laser has passed, the liquid is able to re-crystallize onto the semiconductor. Unfortunately, this re-crystallization is not

nearly as exact and precise as the original growth process which ultimately causes both physical and electrical damage to the semiconductor. [8]

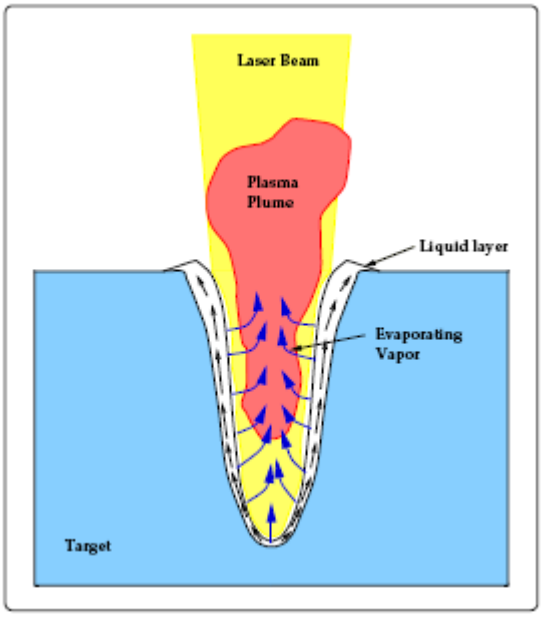

Figure 10: Schematic of a General Laser-Material Interaction [17]

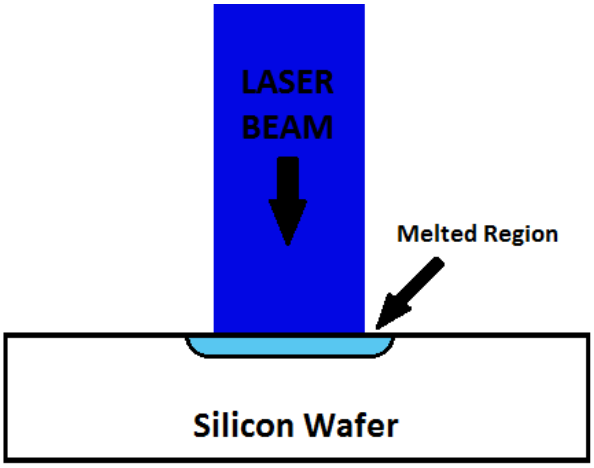

Figure 11: Schematic of Laser Beam Damage of Surface Melted Region

Electrical Damage of Laser on Schottky Barrier Height on GaAs

The electrical damage caused by laser processing on GaAs has been previously studied. A pulsed XeCl excimer laser was used to melt both n and p type GaAs samples. By melting GaAs with the pulsed laser, defects were introduced into a shallow layer near the surface. [18] The charges trapped in the surface defect layer effectively cause a Fermi level shift that dramatically changes the electrical properties of the metal-silicon device. For the Schottky barrier height measurements, the height increased 0.38eV for p-type and decreased by 0.30eV for the n-type GaAs. [18] To explain these shifts in barrier height, a bulk Fermi level stabilization model was used. Additionally, it was noted that once electrical damage had occurred, the shift was instantaneous but did not continue to grow with increased power. [18] Because silicon is also a similar semiconductor material, it is forecast that it too will display similar shirts in the Schottky barrier height measurements.

Electrical Damage of Ion Bombardment on Schottky Barrier Height

In previous studies, it has also been determined that ion-bombardment has a similar effects on Schottky barrier height as laser irradiation. Low-energy ion bombardment is inherent to numerous processes used in the semiconductor industry. Examples are plasma and reactive ion etching that offer a precise dry etching process as against conventional wet chemical etching. [19] The major advantage of dry etching procedures is etch anisotropy which yields a high-resolution pattern delineation. [19]

Conversely, there are also several consequences of low-energy ion bombardment on the Si surface. These may include: physical sputtering, surface amorphization, subsurface damage, ion entrapment, impurity incorporation, and chemical modification on the surface layer. [19] The most effective way to analyze the damages caused to the surface is by analyzing the Schottky barrier height modification. The Schottky barrier serves as an excellent diagnostic tool to evaluate the surface modification of the silicon wafer. [19]

Ion beam etching uses an inert gas which is fired at the surface of the material at low energies. The goal is to disrupt the naturally occurring oxide layer and leave a clean exposed wafer area behind. The process offers little selectivity when coming into contact with the surface as the ion beam has limited precision. The result is that the ion beam causes damage to the surface of the freshly cleaned wafer after the protective oxide layer is removed; thus lattice damage occurs. [19]

In a previous study, to quantitatively measure the surface damage, gold Schottky contacts were added to both the n and p type ion etched Si wafers. The results are shown below in Figure 12:

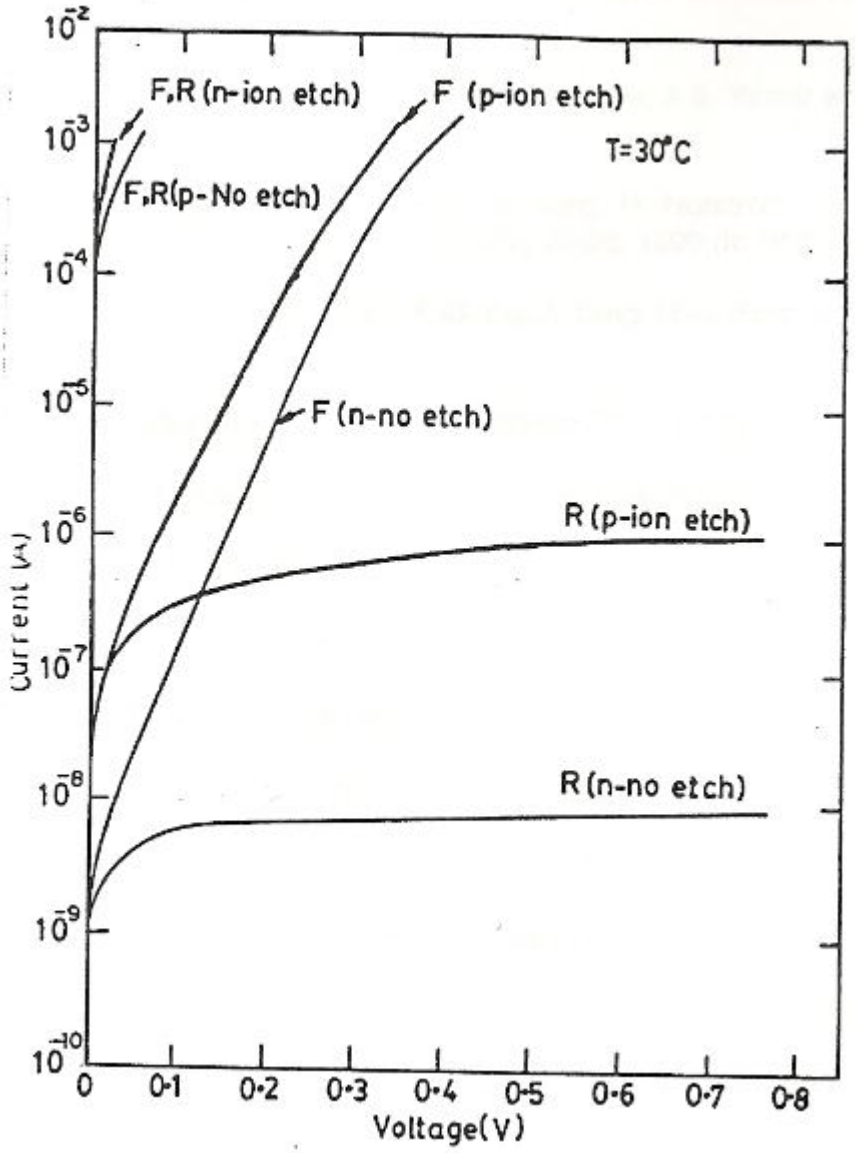

Figure 12: Forward (F) and Reverse (R) Log(I) - V Plots of Au/n-Si and Au/p-Si Diodes with and without 2keV Ar Ion Beam Etching [19]

As expected, the control devices showed that the n-type wafer displayed rectifying behavior whereas the p-type wafer was more ohmic. However, the ion-etched samples displayed the complete opposite characteristics. Now, the n-type wafer was ohmic while the p-type wafer became rectifying. [19] Qualitatively speaking, this meant

that the barrier height was reduced for the n-type and the barrier height was increased for the p-type.

Examining these results from the n-type wafer, the ohmic behavior modification is not altogether surprising. It indicates there is an increased leakage after ion damage showing that there is a relationship between sputter deposition damage and ion etch damage. [19] It was found that the root cause of the barrier modification was due to lattice damage close to the surface. The lattice damage resulted in a positive charge arising from the generation of donor-like defect states near the surface. [19] Similar Schottky barrier formation studies with in-situ ion etching have also confirmed this creation of donor levels due by ion damage. [19]

CHAPTER 3

EXPERIMENTAL PROCEDURE

Design of Experiment

The experiments performed for this thesis utilized both n-type and p-type silicon test wafers. The wafers were 150 mm in diameter and between 650 and 700 μm in thickness. Both wafers had a crystal orientation of <1 0 0>. The n-type wafer was doped with Phosphorous and has resistivity in the range 2 - 7 Ω-cm. Similarly the p-type wafer had resistivity in the 1 - 10 Ω-cm range and was doped with Boron. The corresponding doping levels for these samples were approximately 3×10^{15} cm^{-3} for n-type and 8×10^{14} cm^{-3} for the p-type. [6] Because many variables were to be tested, the large wafers were broken into smaller, 1 cm x 1 cm chips using the laser cutting technique preformed by the AVIA Nd-YAG Laser: triple frequency with wavelength of 355nm. After the samples were cut, laser scribing – preformed by the same laser – was used to properly label each sample. Figure 13 shows the cutting and labeling scheme used for the wafers.

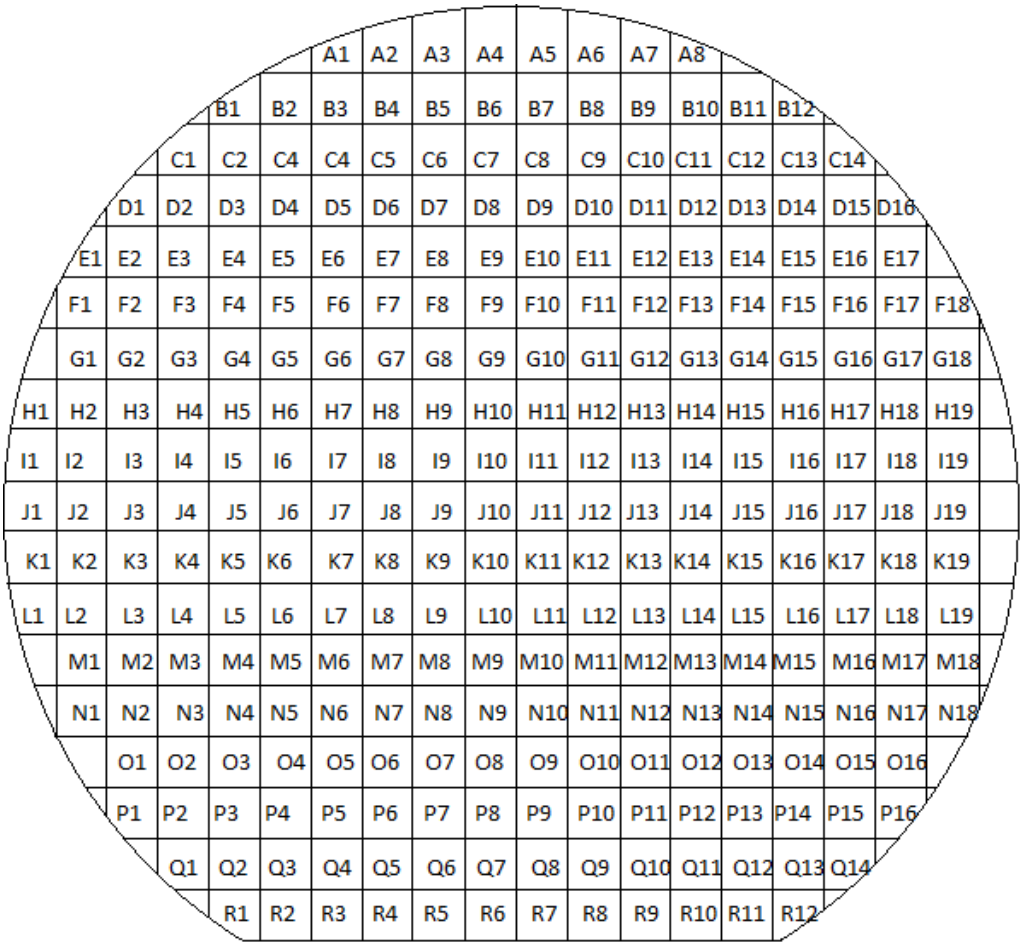

Figure 13: Silicon Wafer Sample Schematic

Each individual wafer was then subjected to laser irradiation. The frequency, and subsequently power and energy levels, for the laser pulse output were varied on the individual cells. Again, the AVIA Nd-YAG laser was chosen for the design. A 3 x 3 mm^2 area was subjected to the laser beam with the goal of obtaining uniform coverage across the exposed area. A diagram of the individual cell is shown in Figure 14.

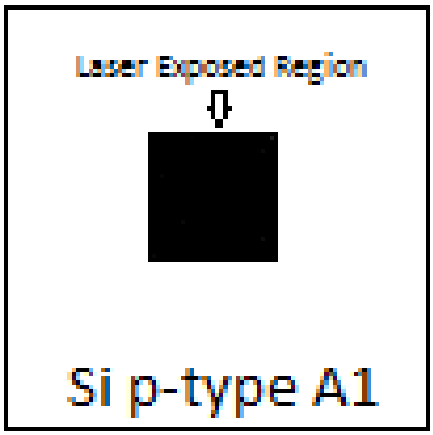

Figure 14: Individual Sample Schematic for Laser Irradiation

To achieve this, the sample was irradiated with a series of pulses while the laser beam was moving at a constant velocity across the cell. The chosen pattern in which the laser moved is shown in Figure 15.

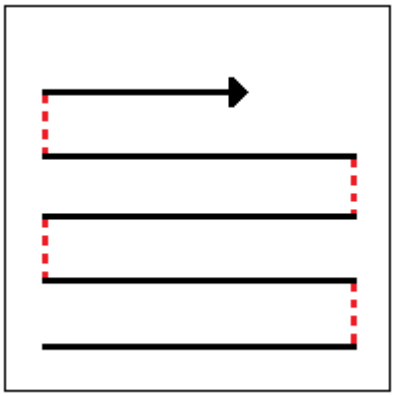

Figure 15: Laser Output Pulse Pattern Design

The samples had slight overlap in pulses due to the geometry of the circular pulse trying to cover a square area. These overlaps were minimized and routinely monitored and corrected to ensure that one area did not obtain more exposure than another. Figures 16 and 17 show a sample after laser irradiation at different magnifications.

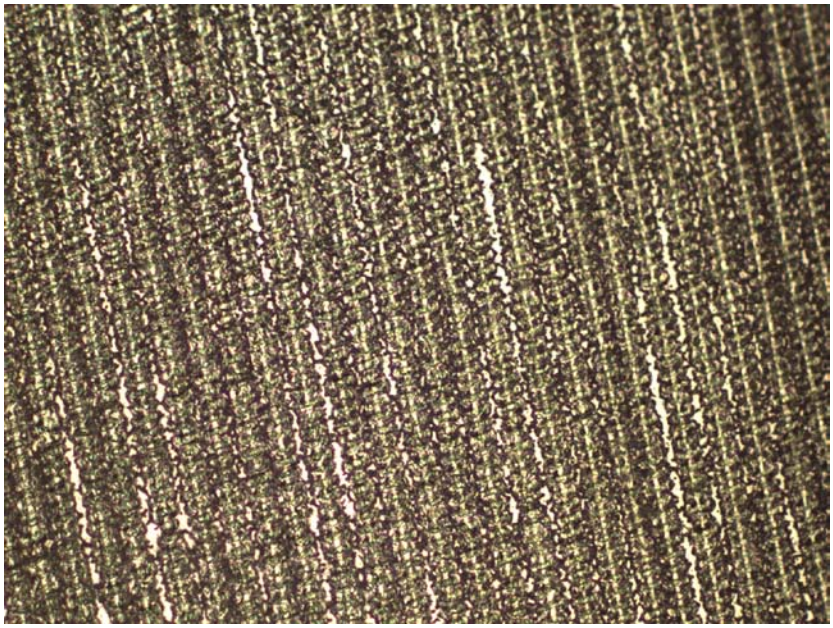

Figure 16: Laser-exposed Region of Sample under Magnification

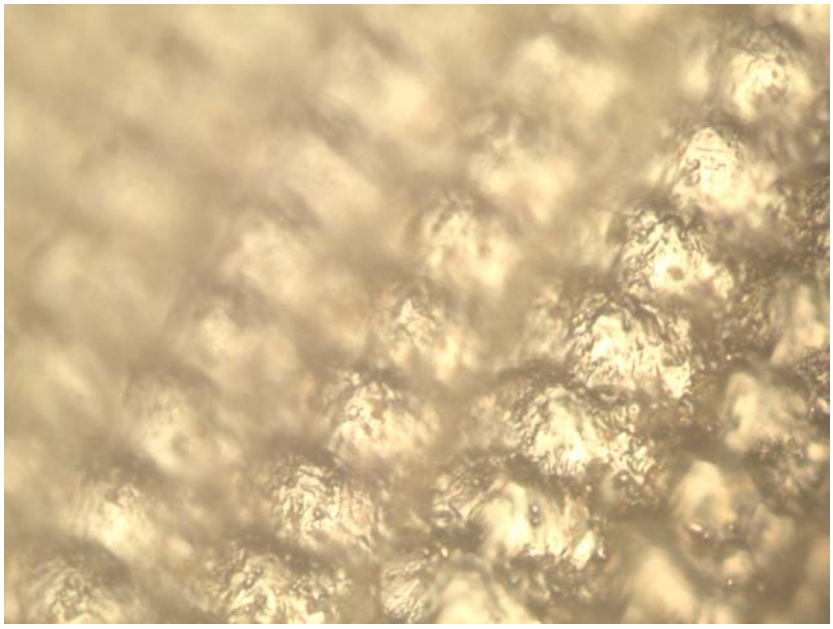

Figure 17: Individual Pulse Pattern of Laser Exposed Region under Magnification

In addition, another pulse pattern was chosen for several of the samples. Instead of covering the area with the pattern shown in Figure 18 and providing an overlap in laser

exposure, a series of individual pulses were chosen that left distinct circular marks. The schematic is shown in Figure 18. Although there was still slight overlap in this laser pulse schematic, it was minimal.

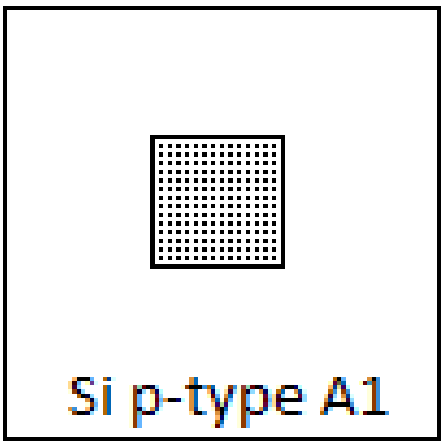

Figure 18: Secondary Individual Sample Schematic for Laser Irradiation

As previously stated, the variable being tested was the power level of the laser beam striking the silicon wafer. To experimentally test this, the frequencies values of the laser were varied in 5kHz intervals ranging from 30kHz to 90kHz. The AVIA Nd-YAG laser is able to produce 30ns pulses at frequencies of up to 100kHz. The power vs. frequency is described by the blue curve in Figure 19. The maximum average power obtained from the Nd-YAG laser is approximately 3.75W. Additionally, output energy is displayed on the figure by the red curve. Table 3-1 shows the pulse power at each of the frequencies tested.

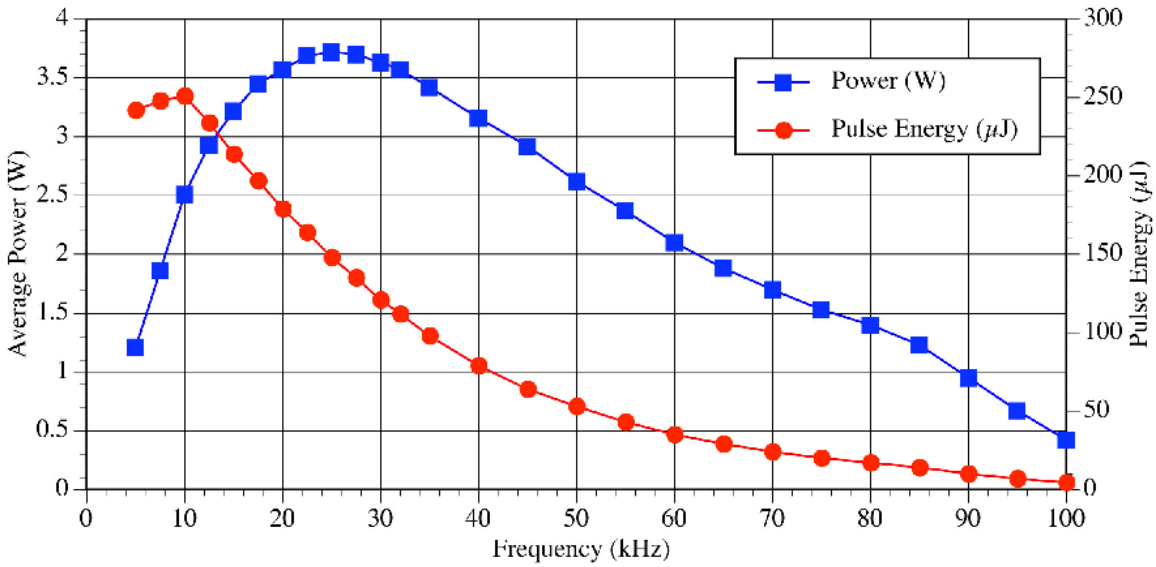

Figure 19: Power/energy Curve as a Function of Frequency for AVIA Laser

Frequency (kHz)	Power (W)
30	3.73
35	3.45
40	3.14
45	2.85
50	2.54
55	2.26
60	2.02
65	1.79
70	1.59
75	1.414
80	1.26
85	1.12
90	0.99

Table 3-1: Laser Pulse Power Delivered at Tested Frequencies

Schottky Barrier Formation

The next step in the experimental process entailed examining the electrical damage the laser creates in the surface region. To do this, multiple Schottky barriers were formed on the wafers. The Schottky barrier offers a very sensitive measurement technique because of the exponential dependence of current on the surface barrier height, which is affected by surface damage. In preparation of the Schottky barrier, the samples underwent a de-greasing procedure. The purpose of the degreasing phase was to remove any unwanted residual material from the surface of the wafer. Such residue layers arise from contact with the ambient air and so the degreasing procedure was preformed immediately before the Schottky metal was deposited, so as to minimize subsequent exposure of the sample to air.

To degrease, the individual samples were first immersed in acetone and placed in an ultrasonic de-ionized water bath for five minutes. This was then followed sequentially by a 5-min immersion in isopropanol and by a 5-min rinse in de-ionized water. The de-ionized water used had a purity level specified by a resistance of 18.3 MΩ.

After the samples were degreased, the thin native SiO_2 layer that forms under exposure to ambient air was removed from the wafers through an etching process. During this process, the samples were submerged in a buffered-oxide etch bath of hydrofluoric acid for 2 min. and immediately followed by another de-ionized water bath. Now, timing became crucial; as the samples could not be exposed to air for an extended period of time, lest another oxide layer should form on the samples.

The front Schottky contact was deposited on the samples first. The samples were fastened under a shadow mask with circular areas of 0.185 mm^2 and then placed in a

vacuum chamber pumped down to below 10^{-7} Torr. The samples were exposed to ambient air for less than 15 cumulative minutes before being placed in the vacuum to minimize any SiO_2 formation.

At this stage, sputter deposition on the samples took place to create the Schottky barriers. To sputter, plasma was formed within the metal awaiting deposition. Then, the plasma was subjected to a 5 Torr beam of argon gas which in turn created metallic vapor particles that were deposited onto the samples. The sputtering took place at a low pressure of argon to help reduce creating any additional surface damage. For the p-type samples, a 100nm thick layer of aluminum was sputtered onto the material while the n-type samples had a 100nm thick layer of gold deposited onto the wafer.

To create the required ohmic back contact, the samples were removed from the vacuum and shadow mask and subjected to another degreasing stage. This time, the samples were again submerged in 5-min dips of acetone, followed by isoproponal, followed by de-ionized water. The only difference from earlier procedure was the absence of ultrasonic bath to avoid displacing any of the newly deposited metal contacts. Again, the same buffered-oxide etching procedure was used on the samples to remove the newly formed oxide layer and the samples were placed into the vacuum with the back sides exposed with less than 15 minutes of total exposure time to ambient air.

Within the vacuum, the ohmic contacts were created by again depositing a 100nm thick layer of metal. This time, the p-type was deposited with Au while the n-type had Al. This time, there was no shadow mask so the entire back of the samples was covered by the deposited metal. A schematic of the wafers after metal deposition are shown in Figures 20 and 21.

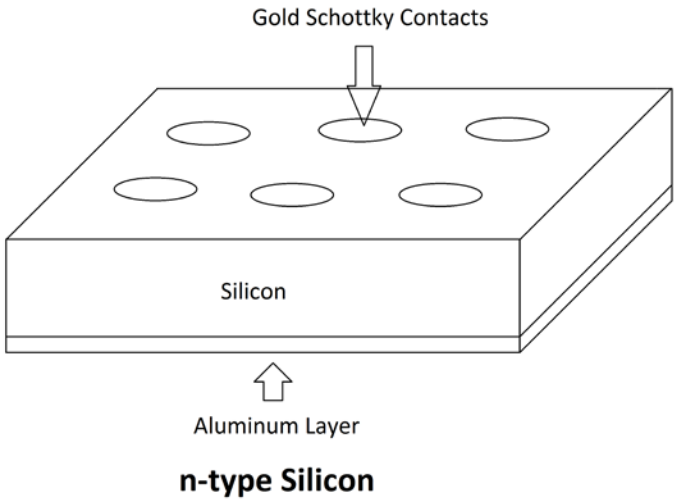

Figure 20: Schottky Contact Diagram for n-type Silicon Wafer

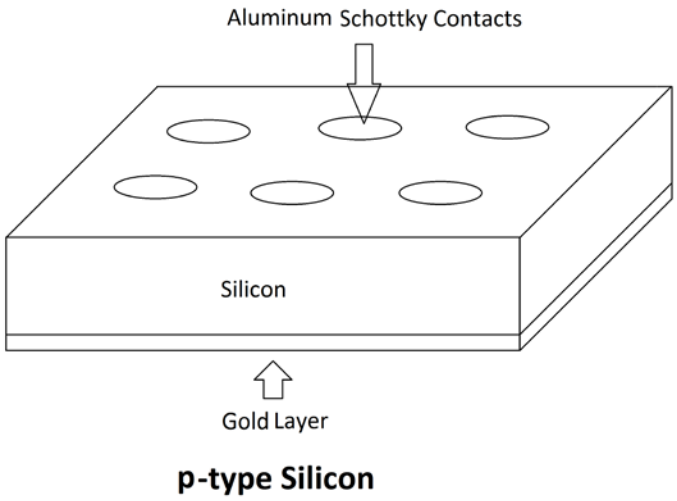

Figure 21: Schottky Contact Diagram for p-type Silicon Wafer

Each sample had approximately 12 Schottky contacts formed on the laser irradiated section and approximately 50 control barriers formed on the unexposed section. Six samples of the laser portion and four control samples were chosen for examining the Schottky barrier height modifications. Each diode had a diameter of 185μm which corresponded to an area of $2.69*10^{-8}\,m^2$. The following figures are images of the Schottky diodes created on the samples. As a reference to magnification, the diameter of each diode is taken to be 185μm.

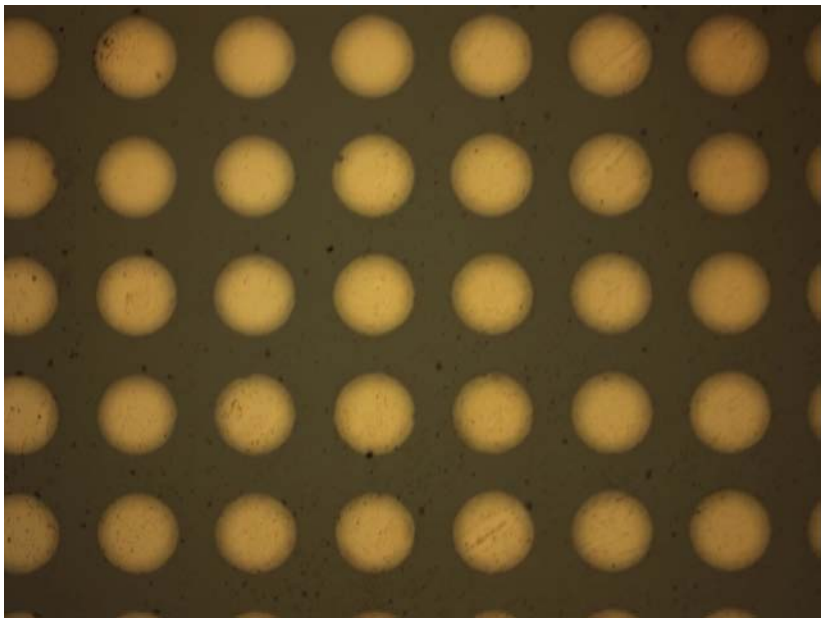

Figure 22: Aluminum Schottky Diodes on p-type Samples under Magnification

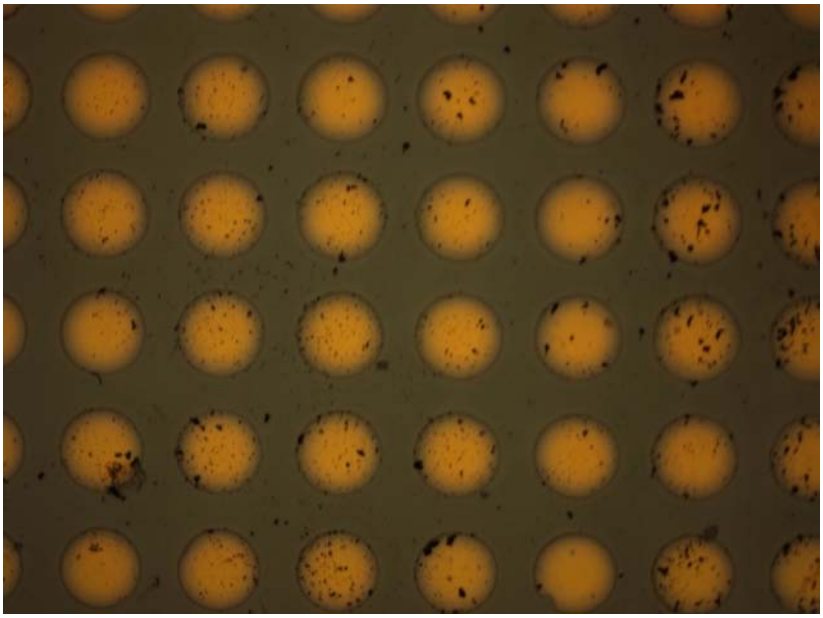

Figure 23: Gold Schottky Diodes on n-type Samples under Magnification

Schottky Barrier Measurements

Now that the barriers were created, the physical measurements were taken to interpret the electrical damage. The samples had their current-voltage characteristics measured, since as noted earlier, the Schottky diode current is very sensitive to surface damage-induced small changes in barrier height. The voltage was allowed to vary from -1 to 1V in increments of 1 mV. The data was then plotted on a *log* current vs. voltage scale to be analyzed.

Each Schottky I-V curve displayed some form of rectifying behavior. To analyze the individual barrier heights, the linear portion of the curve was isolated from the entire data set. Data points from the linear section were chosen so that there was at least a decade worth of linear points. A line was then fit to the data points so that R^2 was always greater than 0.99. From this line, the slope and the y-intercept were extrapolated from the line and these values were then used to calculate the ideality factor and the Schottky barrier height. The y-intersect was saturation current. To calculate the J_0 term in the barrier height equation, the saturation current was divided by the individual diode area.

To determine the actual barrier height, the following equation was used:

$$\Phi_B = -\frac{k_B T}{q} Ln\left(\frac{J_0}{A^{**}T^2}\right)$$

Where A^{**} is the effective Richardson constant and was taken to be $252\frac{A}{cm^2K^2}$ for n-type and $79.2\frac{A}{cm^2K^2}$ for the p-type Si at a temperature of 300K. [6] The following tables show the control diode Schottky barrier height results for both n-type and p-type wafers:

Sample	Laser Pulse Frequency (kHz)	Control Schottky Barrier Height (eV)	Barrier Height Standard Deviation (eV)	Ideality Factor
A3	90	0.72	0.025	1.26
A4	85	0.74	0.022	1.19
A5	80	0.73	0.011	1.20
A6	75	0.73	-----	1.22
A7	70	0.71	-----	1.33
A8	65	0.75	0.008	1.20
B1	60	0.75	0.015	1.18
B4	55	0.71	0.006	1.20
B6	50	0.76	0.013	1.13
B7	45	0.74	0.010	1.19
B8	40	0.71	0.010	1.33
B9	35	0.74	0.005	1.16
B10	30	0.72	0.013	1.23
Average Control Variable		0.73	0.017	

Table 3-2: Schottky Barrier Heights for Control n-Type Silicon Samples

Sample	Laser Pulse Frequency (kHz)	Control Schottky Barrier Height (eV)	Barrier Height Standard Deviation (eV)	Ideality Factor
A3	90	0.44	0.005	3.54
A4	85	0.43	0.002	4.27
A5	80	0.44	0.004	3.94
A6	75	0.42	0.003	4.85
A7	70	0.41	0.001	5.63
A8	65	0.41	0.005	5.25
B1	60	0.41	0.005	5.39
B5	50	0.43	0.002	4.20
B6	45	0.41	0.002	5.14
B7	40	0.42	0.003	4.68
B8	35	0.42	0.002	4.93
B9	30	0.42	0.005	4.60
Average Control Variable		0.42	0.012	

Table 3-3: Schottky Barrier Heights for Control p-Type Silicon Samples

The barrier heights, ideality factors, and standard deviations were also calculated for the laser pulsed area of the sample and their results are summarized in the following tables:

Sample	Laser Pulse Frequency (kHz)	Schottky Barrier Height (eV)	Barrier Height Standard Deviation (eV)	Ideality Factor
A3	90	0.50	0.013	3.20
A4	85	0.52	0.002	2.91
A5	80	0.53	0.003	2.96
A6	75	0.54	0.011	2.82
A7	70	0.54	0.013	2.90
A8	65	0.55	0.007	3.02
B1	60	0.57	0.009	2.42
B4	55	0.53	0.007	2.34
B6	50	0.59	0.016	2.41
B7	45	0.56	0.015	2.44
B8	40	0.54	0.008	2.77
B9	35	0.55	0.011	2.56
B10	30	0.55	0.012	2.70
Average Control Variable		0.55	0.022	

Table 3-4: Schottky Barrier Heights for Laser Processed n-Type Silicon Samples

Sample	Laser Pulse Frequency (kHz)	Schottky Barrier Height (eV)	Barrier Height Standard Deviation (eV)	Ideality Factor
A3	90	0.51	0.005	2.00
A4	85	0.48	0.003	2.47
A5	80	0.52	0.006	2.52
A6	75	0.52	0.009	2.60
A7	70	0.52	0.007	2.72
A8	65	0.50	0.004	3.07
B1	60	0.52	0.003	3.02
B5	50	0.52	0.007	2.99
B6	45	0.50	0.003	4.24
B7	40	0.48	0.007	5.25
B8	35	0.47	0.005	5.70
B9	30	0.50	0.005	4.39
Average Control Variable		0.50	0.016	

Table 3-5: Schottky Barrier Heights for Laser Processed p-Type Silicon Samples

As previously mentioned, these barrier heights were extrapolated from the I-V curves of the samples. These graphs are shown below. The median I-V curve for each laser processed sample is plotted so that the general trend can be observed as a function of the power level of each laser pulse.

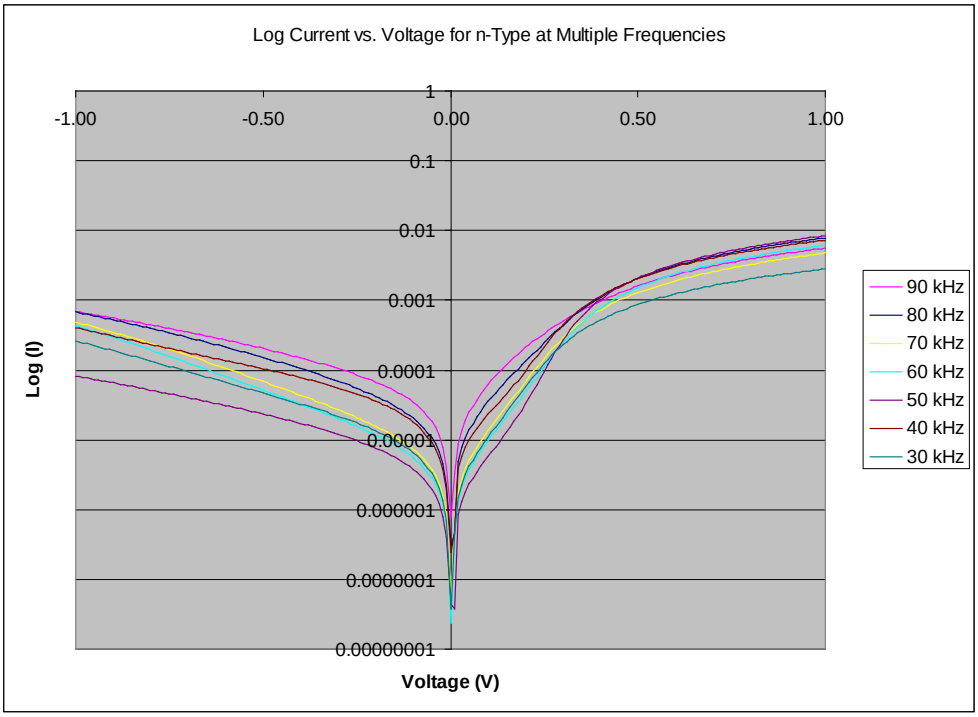

Figure 24: Log Current vs. Voltage for n-type Samples at Multiple Frequencies

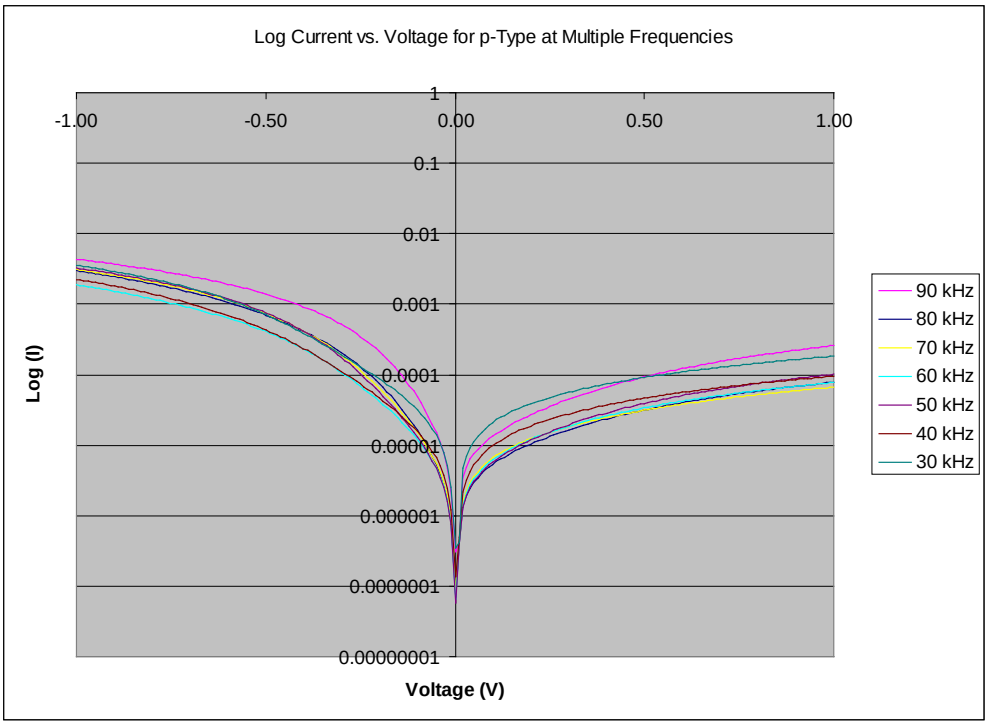

Figure 25: Log Current vs. Voltage for p-type Samples at Multiple Frequencies

In general, it was noted that the higher the frequency level, the higher the I-V curve. However, once a certain frequency level was reached, there was no further change in the I-V characteristics. This was the case for both n-type and p-type wafers. For the n-type wafers, this frequency was greater than 80kHz whereas it had to be larger than 90kHz for the p-type wafers.

The general behavior of the graphs with increasing frequency levels were also compared to that of the control diodes.

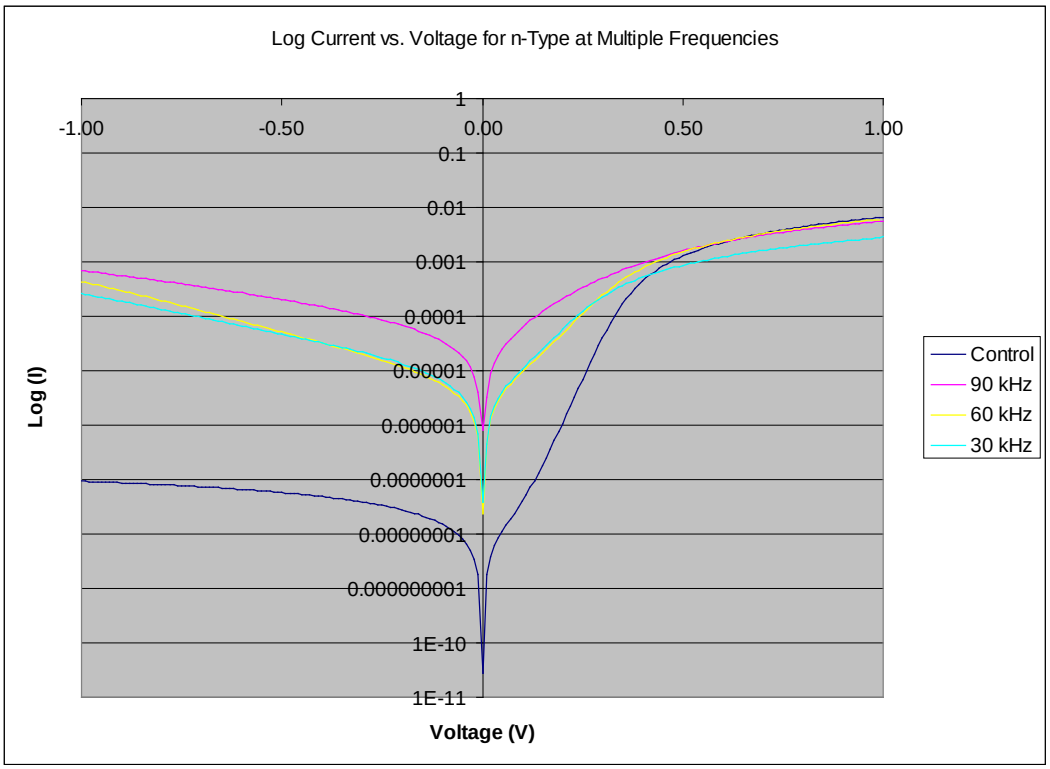

Figure 26: Log Current vs. Voltage for n-type Samples at Selected Frequencies

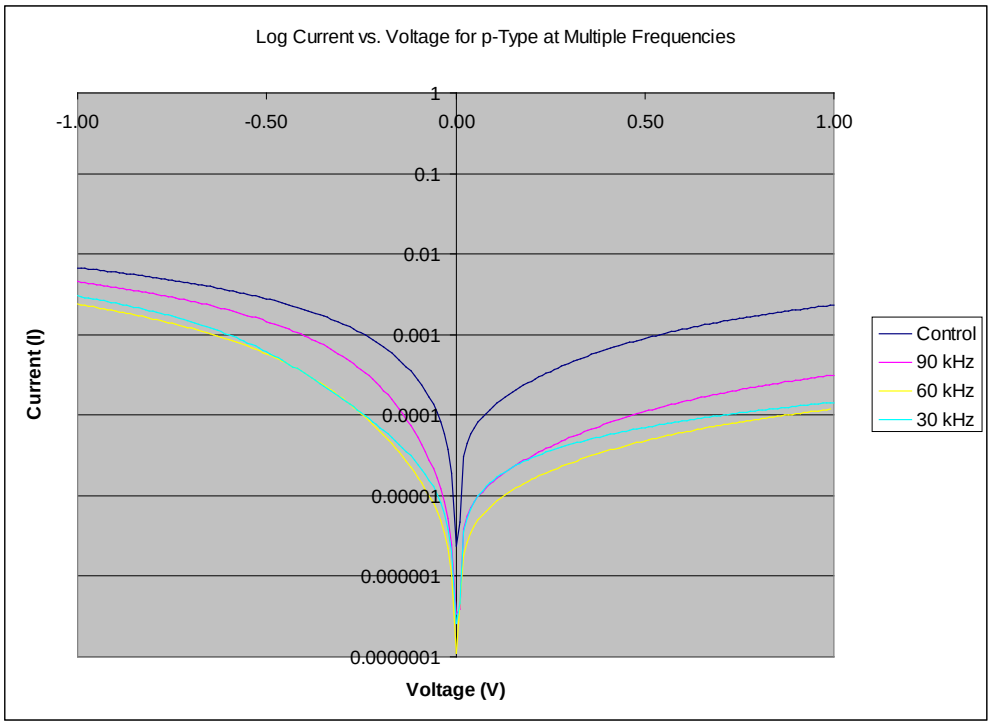

Figure 27: Log Current vs. Voltage for p-type Samples at Selected Frequencies

CHAPTER 4

RESULTS AND DISCUSSION

The goal of this thesis is to investigate the electrical damage that occurs at the surface of Silicon wafer after being processed by a laser; the results may be of significance in solar cells fabricated by lasers for junction formation and contacts.. The investigation was designed to be more qualitative rather than quantitative and the general trends of Schottky barrier height and current-voltage characteristics were studied.

It was found that using any level of laser power caused significant damage to the surface electrical properties. Even at the lowest level of power, the barrier height changed from 0.73eV to 0.50eV for the n-type material and from 0.44eV to 0.51eV for the p-type material. It is believed that this is due to extreme lattice damage caused at the surface. As the laser pulsed the wafer, it heated up the surface to high enough temperatures that a shallow melt pool was formed. When this melt re-crystallized, the lattice structure was no longer as uniform and defects were created throughout the surface.

It was found that as the laser pulse power level increased, so did the electrical damage until a certain damage point was reached. At this point, despite the increase in power level, the electrical characteristics remained the same. What was interesting to note is that this certain damage point really only applied to the shape of the current-voltage graph characteristics; the Schottky barrier height itself did not change much. For the n-type material, at power levels greater than 1.75W, the I-V curves began to look identical and for the p-type material, only a power level of 1.5W was necessary.

With regard to the Schottky barrier height, as the laser pulse power increased, there was an initial dramatic change to the barrier height; however, once initial damage occurred, increasing the power level caused no further changes in the barrier height. On average, the barrier height for the control samples for the n-type material was 0.73 ± 0.017eV. After any processing had occurred, the barrier height for the n-Si was then changed to 0.55 ± 0.022eV. This meant that the barrier was decreased by approximately 0.18 ± 0.022eV. The overall result in this decrease in barrier height was that the samples were much more "Ohmic" than they originally were. It is believed that the major reason for this occurrence is due to a dramatic increase in leakage current after the damage took place.

Examining the p-type material, the exact opposite change was observed in the Schottky barrier height. Instead of the device becoming more ohmic, it actually became more rectifying. Originally, the control samples exhibited a barrier height of 0.42 ± 0.012eV. However, after laser damage occurred, the barrier height changed to 0.50 ± 0.016eV. This meant that overall, the barrier height was increased by approximately 0.08 ± 0.016eV for the hole carriers. A possible explanation for the increase is due to a resulting positive charge from the generation of donor-like defect states due to lattice damage on the surface.

Another hypothesis for the shift in Fermi level pinning may be due to the laser potentially forming a compensation layer near the surface as what occurred in past studies involving GaAs wafers being pulsed by an XeCl excitimer laser. In order for this hypothesis to be tested, deep level transient spectroscopy measurements must be taken on the samples.

It should also be pointed out that alloying may have taken place as the power levels were increased, which would have a dramatic impact on the Schottky barrier height. As alloying occurs, the dopant atoms which are substitutionally placed within the original lattice are able to move to other sites where they have energetically deeper levels in the bandgap, disrupting the desired electrical properties. This occurs because the laser transfers power in the form of heat and the diffusion characteristics are proportional to the temperature of the sample; at higher temperatures, more alloying takes place.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

In conclusion, it was found that laser processing had a dramatic change in the surface electrical properties of doped Silicon. After having uniform laser coverage over a section of a wafer, Schottky barriers of gold and aluminum were created on n-type Si and p-type Si respectively. The parameter being investigated was laser pulse power, so subsequently the frequency of the pulse was varied between samples. The current-voltage characteristics were monitored and it was found that laser bombardment produced surface damage, resulting in Schottky barrier height decrease for n-type samples by 0.18 ± 0.022eV and increase for p-type by 0.08 ± 0.016eV. This meant that the n-type materials became more ohmic, whereas the p-type became more rectifying. At the outset, this increase in ohmic behavior for n-type can be explained away as due to increased leakage current from lattice damage. However, the increase in rectifying behavior in the p-type material involves much more complicated lattice damage defects which may include a positive surface charge due to donor-like defects or potentially a compensation layer being formed. Alloying of the doped atoms may have also had an impact on the electrical properties of the material after processing.

Future work is quite substantial and will revolve around finding better processing methods of creating photovoltaic solar cells using Silicon. Lasers hold enormous potential in this field and there are many benefits from using the high intensities and non-contact characteristics lasers have to offer. Unfortunately, the negative sides of laser processing must also be investigated and analyzed before enough is known about the

subject, which is why it is important to study the electrical surface damage.

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