THE PENNSYLVANIA STATE UNIVERSITY
SCHREYER HONORS COLLEGE

DEPARTMENT OF ENGINEERING

EFFICIENCY OF GALLIUM NITRIDE SEMICONDUCTOR SWITCHING COMPONENTS

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ABSTRACT

The primary purpose of this work is to analyze the operation and efficiency of the Gallium Nitride switching devices in the three-level switched capacitor topology. Switching devices are small components, called transistors, that are great at switching voltage or current at high frequencies. Transistors make it possible to create circuits such as a power converter that takes a DC voltage and converts it to an AC voltage.

Transistors are utilized in a prodigious amount of applications that are used on a daily basis such as in cellphones and electric motor controls. The wide use of the switching devices is a big reason why it is important to study the efficiency of the switching devices. By knowing how efficient the Gallium Nitride switching devices are in certain circuit topologies, designers would then be able to create even more efficient devices for consumer and industrial applications.

Another reason why it is important to improve the efficiency of the switching devices is because nearly half of the power generated in power plants goes into factories to power electric motors. Therefore, since the switching devices are part of the control circuitry for these motors, the more efficient the control circuitry the less power losses that occur, hence cost and energy is saved.

This research project is rather broad in scope so it was conducted over two semesters. The first semester was focused more of the design and simulation of the circuitry while the second semester was the actual construction and implementation of the circuit. In the first semester, the design of a power electronics building block (PEBB) started using Multisim 14.0, which is a circuit simulation software. The circuit created was half of a three-level switched capacitor circuit and so two boards were cascaded together to form the total three

level switched capacitor circuit. Efficiency of the circuit topology will then be analyzed and compared to that of other types of transistors such as the Silicon transistor.

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Chapter 1

Introduction

In today's society where there is a dire need to help fight the energy crisis, newer and more energy efficient products are always being sought. These products are not only sought after by consumers, but also by industrial companies who often benefit financially by continuously upgrading to more efficient machinery and control systems. A key role in developing more efficient products is delving into the power electronics within a specific product. In the research field of power electronics, there are a plethora of areas to consider. However, the main focus of the following work will be on a specific electrical component within power electronics known as a transistor.

The following study specifically focuses on how much more efficient Gallium Nitride (GaN) transistors make circuit topologies, as compared to circuit topologies that use other types of transistors such as Silicon Carbide. GaN transistors were chosen as the research component because GaN transistors became readily available to the public about a year ago and are deemed to be more efficient than older types of transistors such as the Silicon transistor. Since the GaN transistor has not had much time out in the public domain, there has not been a lot of research into how much more efficient the Gallium Nitride transistor makes certain circuit topologies. The lack of research in the field of GaN transistors is why it is exciting to see how much more efficient the new transistors make certain topologies. This research can not only lead to more efficient factories that use power electronics such as power plants, but also more efficient consumer products such as cell phones.

In order to conduct the above research, the work will take place in two parts. The first part of the research will focus on the design of the testing module, while the second part will focus on implementing and testing the module. The first phase of the research will last through the Spring 2017 semester and the second phase will proceed through the Fall 2017 semester.

Chapter 2

Background Information

Before proceeding into the main portion of this work it will be necessary to provide some background information on some of the topics that will be central to the following text. The first topic is transistors.

Transistors are electrical components that act as switches that can toggle very quickly. These components are used instead of mere mechanical switches because they can switch on and off very rapidly without wearing out and they can switch with minimal power loss. Mechanical switches cannot be operated at such high switching frequencies, and therefore are not used in power electronics as a switching device. In addition to the transistor's fast switching capability, it is also capable of controlling high current and voltage with a very small control voltage. This kind of capability is necessary because many methods of controlling circuits utilize devices that can only output a small voltage such as 3.3 volts or five volts which would be an insufficient signal to control other types of switches that can handle large voltages such as a relay. In addition, there are many different kinds of transistors. A common transistor type is the Bipolar Junction Transistor (BJT) and there are several types such as positive negative positive (pnp) transistors and negative positive negative (npn). Another type of transistor is a MOSFET transistor. MOSFETs can be constructed using standard Silicon (Si), or more recently using Gallium Nitride (GaN). The GaN MOSFET transistor is the kind of transistor being studied in this work. The MOSFET transistor (Si or GaN) has several parts to it known as the gate, drain,

and source. The gate is the part of the transistor that receives the signal to turn on and off. The drain is the part where the power comes into the transistor and the source is where the power comes out of the transistor.

Another key topic is frequency. Frequency is a term that identifies with how quickly a signal goes through one full cycle. An example of this can be seen below in figure 1. Frequency has the unit of one over seconds also known as Hertz (Hz).

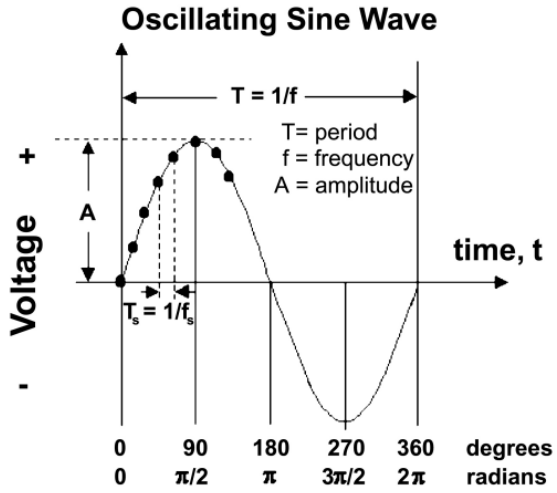

Figure 1: Frequency is the reciprocal of the time period T of the waveform. [2]

Alongside the idea of frequency, another large topic during this research project is pulse width modulation (PWM). PWM is a square wave that can be set to run at practically any frequency. PWM is even able to be programmed to change how often the signal comes on and off known as duty cycle.

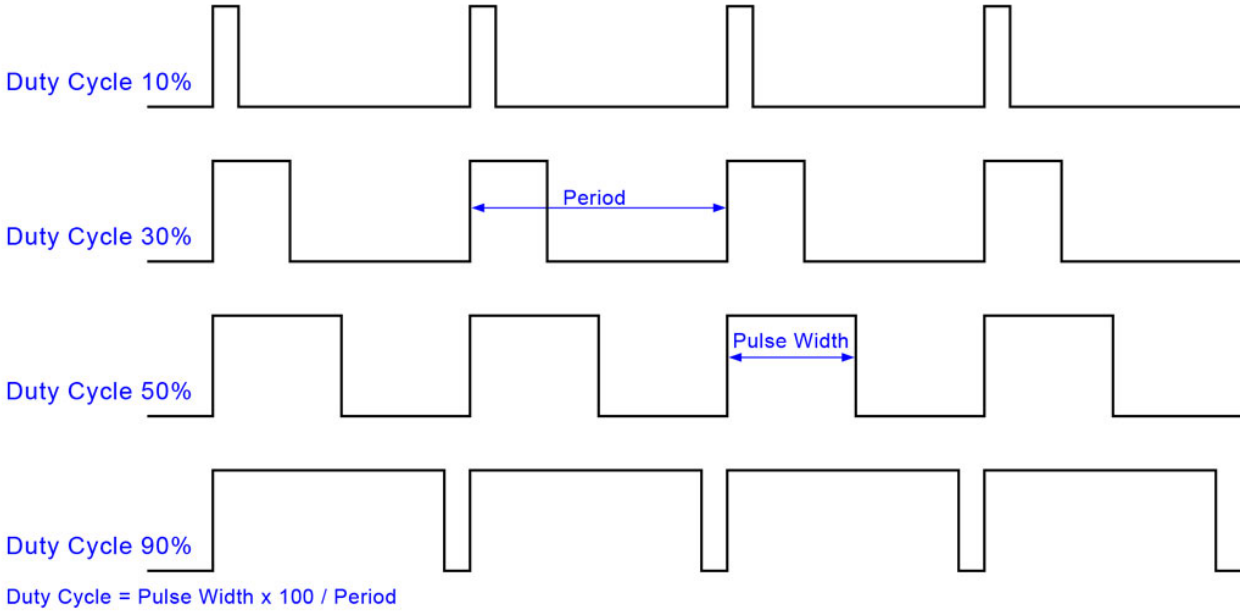

Figure 2:Representation ofPWM duty cycle and pulse width [1]

Chapter 3

Research Criteria

In order to begin the research project, it was necessary to develop a list of criteria necessary to complete the research effectively. The first piece of criteria was to develop a testing board. This board had to be designed in such a way that it has the flexibility to be transformed into a number of circuit topologies so that it can be used in future research projects. In addition, the circuit board will utilize a switched capacitor topology to both exploit the fast switching capability of the GaN and to eliminate the need for bulky inductors. When designing the circuit board, the components must be placed close together in order to minimize parasitic inductance and capacitance in the traces on the board that can degrade high-speed switching performance. The previous requirement is a key component to reduce switching losses, since a main focus of the research is to look at how efficient the GaN transistors can make circuit topologies. If the design circuitry is introducing unnecessary losses into the circuit, then the research will be inaccurate. In addition, having the components closer together allows one to have a higher power density which is desirable. A high-power density is desirable because it shows that there is not wasted space on the board and one is able to place more power in a smaller area.

Another key requirement for the board that will reduce energy losses is to place the GaN devices and the Gate Drivers close to each other. This requirement is necessary and even more important than having the other components close together because the gate drivers control when the GaN devices switch. If the gate drivers are further away from the GaN devices then this introduces power losses, as well as introduces lag into the system. Lag within the system is

undesirable because the transistors are switched on and off at a high frequency. With lag, the operating frequency decreases slightly and causes unnecessary power losses into the system. In addition, if lag is introduced there is a possibility that the signals for each GaN device could cause the GaNs to turn on at the same time causing a short circuit.

Additional requirements were that the board needed to be restricted to being a two-layered board. A two-layered board allows one to place traces and components on the top and bottom of the board. A higher layered board could not be used because with more layers added, the more expensive it is to produce the board. This more expensive option was not feasible because the budget for the entire research project was $600. The board also could not be a one-sided board because it would cause the board to be quite large and it would not allow the components to be close together reducing the power density. Having a two-sided board also allows for a higher power density than if you had a one-sided board.

A final requirement was that the components needed to be surface mount (SMT) instead of through-hole (THT). Surface mount components are more desirable than through hole components in this application because their packaging density inherently reduces the parasitic inductance and capacitance, and allows one to place the components closer together than through hole components. Some components may only come in through hole, but if there is a surface mount option for a component it would be ideal to use the surface mount component.

Chapter 4

Design of the Test Set-Up Using Multisim 14.0

To begin the design process to meet the design criteria listed in the previous chapter, the initial step was to decide on what kind of circuit would be used. In order to choose a circuit, the primary focus was finding a topology that could easily be transformed into a number of different circuits. Another significant factor in choosing the circuit topology was making sure that the topology was something one would see in industry, primarily in the field of voltage transformation. In addition, the circuit is to have a high-power density, which led to the selection of a capacitive switching circuit that does not rely on bulky inductors. Switched capacitor topology is particularly attractive at the high switching frequencies that the GaN MOSFET is capable of operating at. When considering all of the above criteria, the circuit that fit the criteria was a three-level switched capacitor circuit. The switched capacitor circuit can be seen below in figure 3.

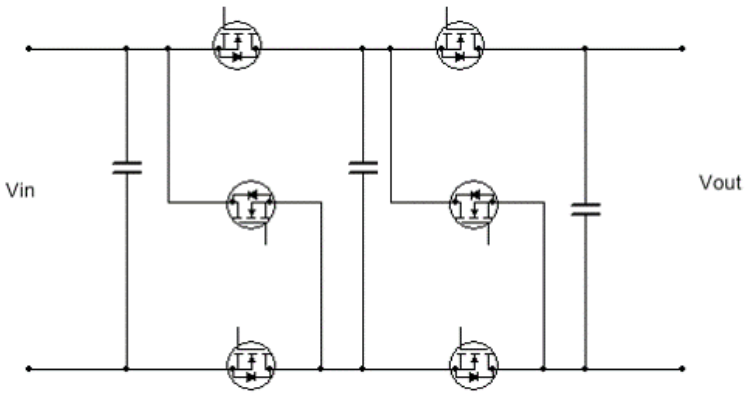

Figure 3:Switched capacitor circuit utilized in board design [3]

The switched capacitor circuit is capable of transforming into a number of different circuit topologies such as a Marx inverter, a three level Marx inverter, and an isolation cell among others. In choosing the switched capacitor circuit, a more power dense solution as compared to an inductive topology can be achieved.

The energy stored in a capacitor is given by

$$E_c = \frac{1}{2} C V^2 ,$$

where *C* is the capacitance, and V is the voltage across the terminals of the capacitor. In a switched capacitor topology, the power delivered by the capacitor to a load per switching cycle is described by

$$\Delta P_c = \Delta E_c f_s = \frac{1}{2} C \Delta V f_s$$

where f_s is the switching frequency. Since the physical size of a capacitor is directly related to its capacitance (*C*) at any given voltage rating, it can be seen from the equation above that it is most effective to increase the switching frequency to obtain increased power density (that is, increase ΔPc without increasing size). Since the GaN is capable of very high switching frequency, the switched capacitor topology is very well suited to the use of GaN switching devices.

Once the main circuit topology was known, the circuit began to be designed. In order to design the circuitry, Multisim 14.0 was utilized. Multisim 14.0 was used due to the availability on campus, as well as its ability to allow users to easily design circuits and simulate them. The other option for a simulation software was LTspice. LTspice is similar to Multisim in that it simulates the circuitry, but LTspice is far harder to simulate the circuitry due to its ability to

make the simulation highly customizable. Multisim lets the program software run the simulation according to its code allowing for less customization, but it is far easier to operate.

When designing the board, the circuits were partitioned into sections according to their functionality. The first part designed was the control circuitry and then the switching circuitry was created. The control circuitry was designed first because this circuitry is what primes the PWM signal to go into the switching circuitry to control the GaN devices. The control circuitry takes a PWM signal and breaks the input signal into three separate signals and introduces approximately 6 microseconds of dead time into the signals. Dead time is when two or more signals are low before one of the signals goes high. Dead time is needed in this type of circuitry because with the GaN devices switching so rapidly, there is a possibility that the control signals for the GaN devices could all be high at once which would cause a short circuit. When a short circuit occurs, current runs infinitely high and this would ultimately destroy the circuitry. Hence, the dead time circuitry is used to keep the short circuit from happening and to ensure that the control signals are on at different times. One signal is inverted so that the signals are opposite of each other. This is needed because with the three-level switched capacitor circuit, the top two switching devices are controlled by the same signal while the GaN device on the parallel branch is controlled by the other signal.

In order to choose the correct component values in the dead time circuitry, as seen in figure 4, that consists of a resistor, diode, and capacitor. Given a dead time needed of 6 microseconds the resistor and capacitor values are given by:

$$\tau = RC$$

Where τ is the time constant and R and C are the resistor and capacitor values respectively. The dead time needed is four time constants so the desired time constant is

$1.5x10^{-6}$. Choosing a small capacitance of 0.01 microfarads one can see that one would need a resistance value of at least 15 ohms. In order to allow for some adjustment of the dead-time, a 100 ohm potentiometer was used to increase and decrease the resistance as needed.

After the control signals have been manipulated, the signals are fed through an optocoupler to the high voltage side of the board. The test board was designed so that there would be isolation between the low voltage control signals and the high voltage switching capacitor circuit. In order to provide the isolation necessary, an optocoupler is used which physically isolates a smaller control signal from the higher voltage circuitry on the other side of the optocoupler.

After the isolation was brought into the circuitry, the switched capacitor circuit began to be designed. When the board was designed, half of the circuit in figure 2 was placed on a board so that the complete circuit shown could be made with two boards. This decision was made in the design process to allow for an easier time to change the circuit topology into different configurations. The first piece of circuitry coming off of the isolation was a gate driver. This gate driver takes the control signal and boosts the amount of current and voltage in this signal. The GaN devices require a voltage of 5 to 6 volts in order to switch the transistor on and the high frequency application requires there to be higher current than what the optocoupler can provide in order to quickly charge the capacitive gat input of the GaN device. The gate driver essentially acts as a buffer in order to prime the signal for use by the GaN devices. Once the signal comes out of the gate driver, it comes into some gate drive circuitry that limits the gate driver inrush current, while not making the gate drive susceptible to stray coupling that becomes so important at high switching frequency. Following the inrush protection circuitry is the actual GaN devices. The control signal is placed onto the gate of the GaN device. This part of the circuitry was

designed as per the topology of the three-level switched capacitor circuitry. It was chosen to design the circuitry to be run at 50 volts and then have the capability to double up to 100 volts. To allow the circuitry to double to 100 volts, the capacitors that are used in this circuitry were chosen to be two 3300 microfarad capacitors in parallel to make a 6600 microfarad capacitance. This capacitance was chosen as per the following equation:

$$\frac{\Delta V}{t} = \frac{I}{C}$$

where I is the max current load of 20A and the ΔV is change in voltage and t is time. Change in voltage over time needed to be approximately 3 volts per millisecond in order to supply enough energy to the circuit and to be able to charge quickly enough when the capacitor is not switched on. As one can see, the capacitance is 6600 microfarads in order to meet the above criteria for current and change in voltage over time.

This high capacitance was needed so that enough energy could be stored within the capacitor to allow a large enough current to flow off of the discharge of the capacitor so that it could match the output current of the circuitry when the capacitor is charging and the output is from the power source. In addition, the circuitry was designed so that it could handle a maximum of 20 Amperes of current. The final circuit design is shown below in figure 4.

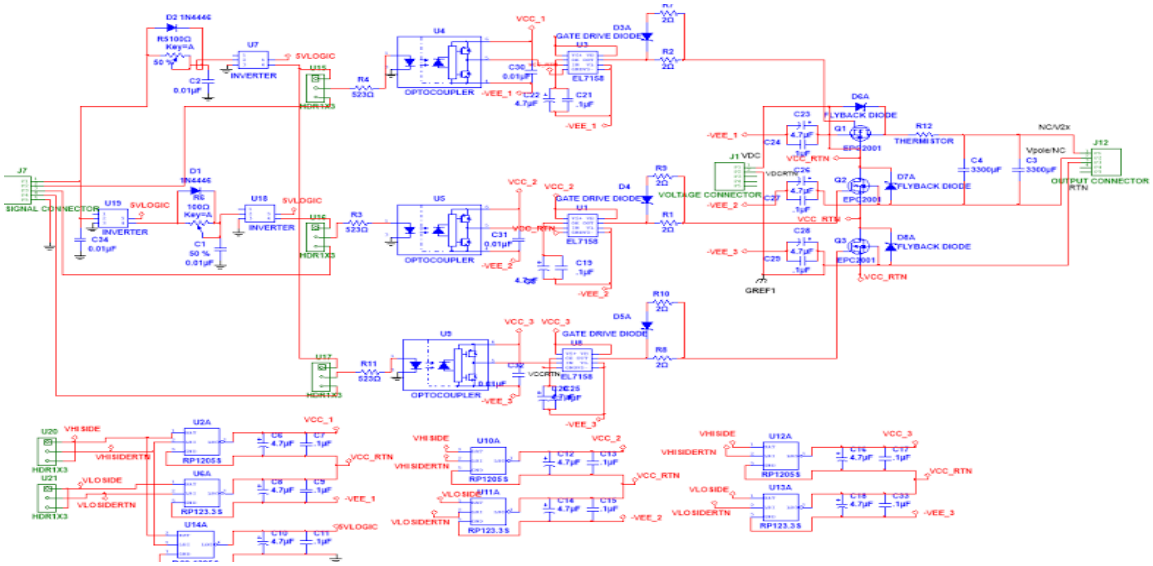

Figure 4:Multism Circuit for three-level switched capacitor circuit

Chapter 5

Design of the Test Set-Up Using Ultiboard 14.0

After completing the design of the test board using Multisim 14.0, the layout had to be converted over to Ultiboard 14.0 in order to produce the board layout file. When using Multisim, the electrical connections were established and the components were chosen, but the layout of all of the components on the board and how the electrical connections would be laid out were not specified. In order to specify the unspecified mechanical and electrical characteristics, Ultiboard allows the designer to choose the size of the board, the placement for each component, and the layout of all of the traces.

When designing this particular board, each of the above pieces of the design were considered carefully. In regards to the size of the board, due to budget restrictions the board had to be kept within a 6”x 6” space. Oftentimes, board manufacturing companies charge a higher price for printing a larger board and with the limited budget of $600, it was key to reduce costs where possible.

In order to properly design the layout of the board, it was imperative that the correct footprint for each component was put onto the board. The footprint is what the electrical component is soldered to in order to make the electrical connections. If the wrong footprint is used, then the component will not fit and the circuit will not function properly. After making sure that the board was designed properly from a footprint perspective, the board was then laid out in Ultiboard.

Just like the board was designed left to right in Multisim, the components were laid out in the same manner in Ultiboard. On the left side of the board was the control circuitry followed by the electrical isolation and then the actual switching circuitry. In addition, when the board was laid out the components were placed as close together as possible in order to reduce the size of the board and to obtain the most efficiency of the GaN devices. However, when placing the footprints on the board there had to be a ten mil space between any of the footprints and anything else that was on the board. The ten mil space is called a keep out area and it is used to keep connections that are close to each other from connecting. In order to keep the board size to a minimum, some of the components were placed on the underside of the board. The components that were placed on the underside of the board were mainly the bypass capacitors. The bypass capacitors are not part of the main circuitry, but rather they help to reduce noise that is produced by the quick switching of the components.

Once the components were laid out, the traces, also known as electrical connections, were designed. Once again when laying out the traces, there had to be at least a ten mil space between any of the traces and the footprints. Another design consideration when laying out the traces was the traces' thickness. The factor that decided how thick the traces were was how much current would be going through the trace. For example, the control circuitry had very low current going through it so those traces were only 10 mils thick. However, on the switching side of the board there were places where there could be up to 20 amps of current flowing through the circuit and so those traces had to be 958 mils. A key feature in designing the traces was having them be able to run from one side of the board to the other. Traces are unable to run on top of each other or run into each other so in order to run all of the traces on one board it had to be designed so that some of the traces were on the top side of the board and some were on the bottom side. A

picture of the board layout can be seen in the figure below. Also, the traces were laid out so that they were as short as possible to reduce power losses and parasitic effects.

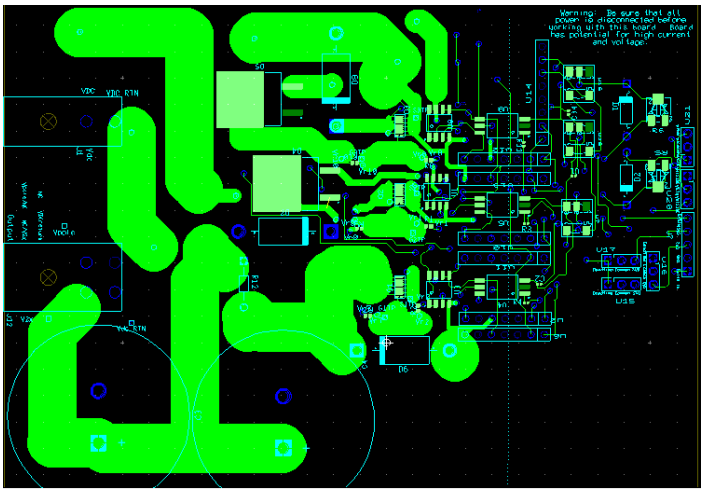

Figure 5: Layout of the top of the circuit board

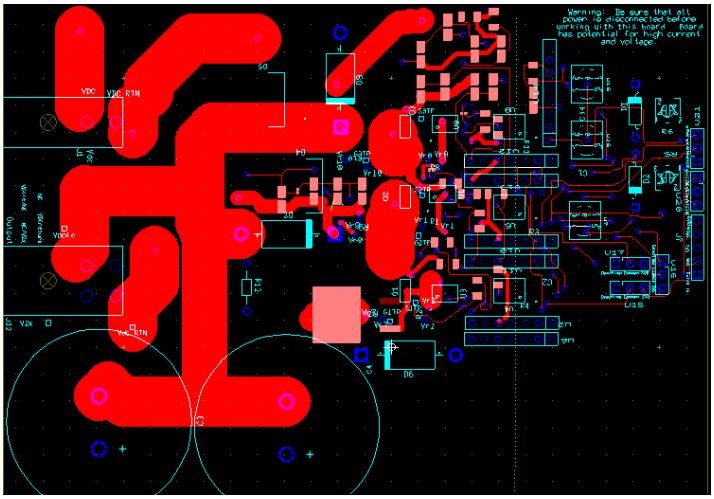

Figure 6: Layout of the bottom of the circuit board

Chapter 6

Manufacturing of the Design

After all of the board files were checked for accuracy, the board files were sent to a circuit board manufacturer. The board manufacturer simply made the circuit board and I was challenged with placing all of the components on the circuit board. In order to make troubleshooting easier, I chose to manufacture the two circuit boards in three separate phases. Both circuit boards will be the same so they will both be manufactured in three separate phases.

The first phase was to manufacture everything up to and not including the optocoupler. This phase includes all of the components needed for the deadtime implementation circuitry. Once the first phase was completely manufactured, I tested each component to make sure that it was properly connected and had the correct value associated with the component. I checked for a proper connection by utilizing a multimeter and checking the resistance of each resistor, the capacitance of each capacitor, and the continuity of connections for other components such as the Direct Current to Direct Current (DC/DC) converters.

Once the components were connected properly, I made sure to test the circuitry using a square wave as well as a 12-volt power supply. I applied the 12 volts to the high side voltage pins in order to supply power to the five-volt logic power supply which gives power to the inverters needed for the dead-time circuitry. The square wave signal I applied to the deadtime pins and the waveform pulsed from two and a half volts to 7.5 volts and the frequency did not matter. Once the voltage was applied and the signal was applied, I placed an oscilloscope at the three pin signal connectors used to supply the input signal to the optocouplers to be sure that the

circuitry was working properly. The first phase worked properly when two of the output signals were inverted and one was not inverted. Another point of functionality to check was if by varying the potentiometer, the offset of the output signal varied. An example of the offset of the output signal can be seen in figure 7 and 8.

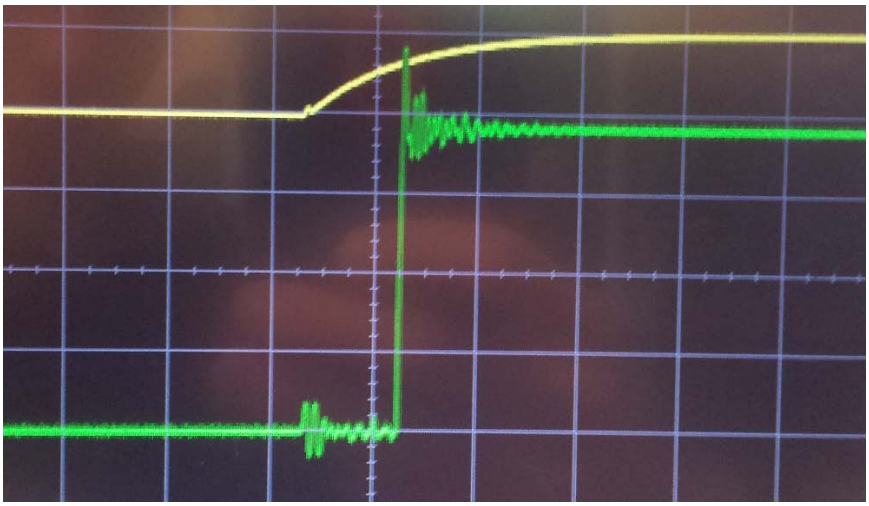

Figure 7: Waveform representing less deadtime where the yellow signal is the input signal and the green is the waveform seen by the circuit

Figure 8: Waveform representing more deadtime where the yellow waveform represents the input waveform and the green waveform represents the waveform seen by the circuit

The second phase of manufacturing was to solder all of the components from the optocoupler up to the gate drivers. This phase mainly included the circuitry that takes the signals from the deadtime implementation circuitry and applies the signal to the high voltage side of the circuit. In addition, this portion of the circuitry implemented the five-volt regular and the 3.3 volt DC power sources to operate the gate drivers. Once again, after the components were placed, I tested each component to be sure that the components made the proper connection. I used the same tests as in the first phase to make sure that all of the components were placed properly. After all of the circuitry placement was confirmed, the same signals were supplied to the circuitry as in the testing for the first phase. When the signals were applied, each DC-DC converter output the proper voltage, either 3.3 volts or five volts. However, in the implementation of this board, it was chosen not to run the 3.3 volt DC/DC converter because the GaN devices could easily be operated by just having a five volt differential between the gate and the source. The 3.3 volt DC/DC converter was placed on the board in case another kind of transistor would be placed on the board that would need more than five volts to turn on. In addition, the signals should be getting to the gate drivers. The signal output of the gate drivers were verified by oscilloscope and the output voltage of the DC-DC converters were tested by a Multimeter.

Following the verification and manufacturing of phase two, the third and final phase was manufactured. This third phase included the GaN devices as well as the output capacitors. Once again, the circuit was tested to make sure that all of the components were placed properly before applying the test signals. The test with the signals on this phase was done more carefully due to the exposure of high current and voltage. In addition to the signals supplied to the board as before, another twenty-volt variable power supply was added to the GaN devices for testing to

allow for a voltage to be put through the GaN devices. In order for this phase of the circuitry to be deemed successful, the output of the circuit needed to output double or close to double of the input voltage to the GaN devices. The finished boards can be seen below.

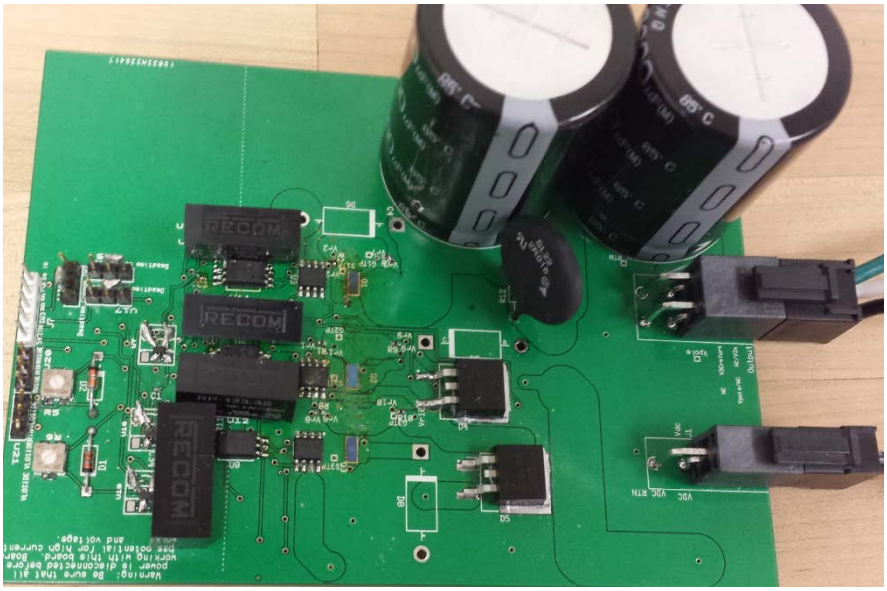

Figure 9: Completely assembled board top side

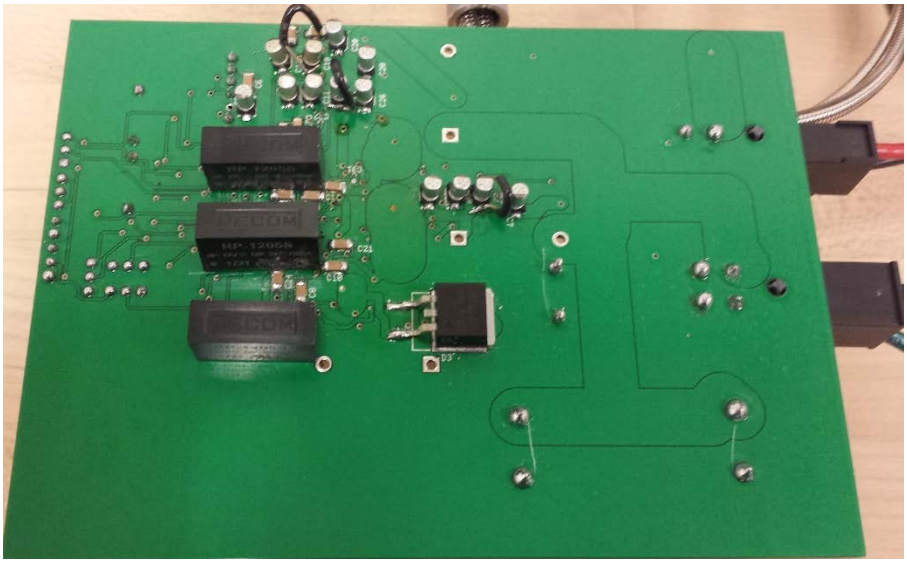

Figure 10: Completely assembled board bottom side

Chapter 7

Experimental Set-Up for Research Testing

Once the boards were tested and functional, the actual set-up of the boards for research could be completed. In the initial tests, the boards will act as a three-level inverter which will take a desired DC input, double the voltage and convert it into a sine wave that will run a motor. By placing a load at the end of the circuitry, it will be possible to obtain efficiency data due to the higher power that will flow through the circuit as opposed to without a load. In order to have the boards function in the way described above, the duty cycle of the PWM put into the board must vary like a sine wave. In order to do this, a Tiva C Series TM4C123G microcontroller was used in order to manipulate the PWM. To manipulate the PWM signal into one that represented a sine wave, a triangle wave at a frequency much higher than the frequency of a compared sine wave must be compared in order to have the PWM signal duty cycle increase and decrease as a sine wave increases and decreases with amplitude. An example of a PWM signal representing a sine wave can be seen below.

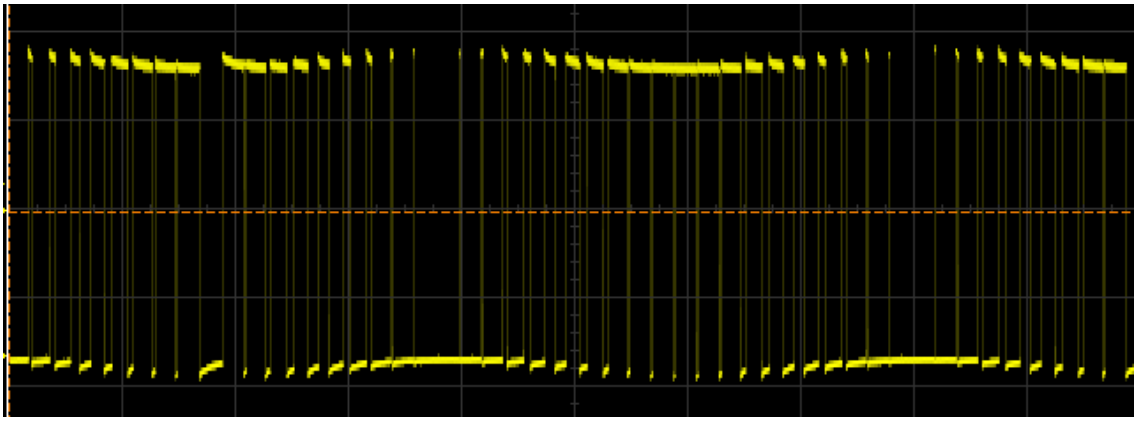

Figure 11: Sine wave represented in pwm format

In order to get the circuitry to work in the desired manner as a three-level inverter, the sine wave shown in figure 11 essentially needs to be “split in half”. The sine wave needs to be “split in half” because in order for the three-level inverter to work, one board will create part of the sine wave up until 50 volts and then the second board will create the second half of the sine wave from 50 volts to 100 volts. A three-level inverter is constructed in this manner to allow for a higher resolution sine wave. If one board was to complete the entire sine wave by itself, at the output one would see a very choppy sine wave. When one splits the sine wave up among two boards, where one does half of the sine wave and the other board does the other half one achieves a higher resolution sine wave. An example of the split sine wave signal can be viewed below.

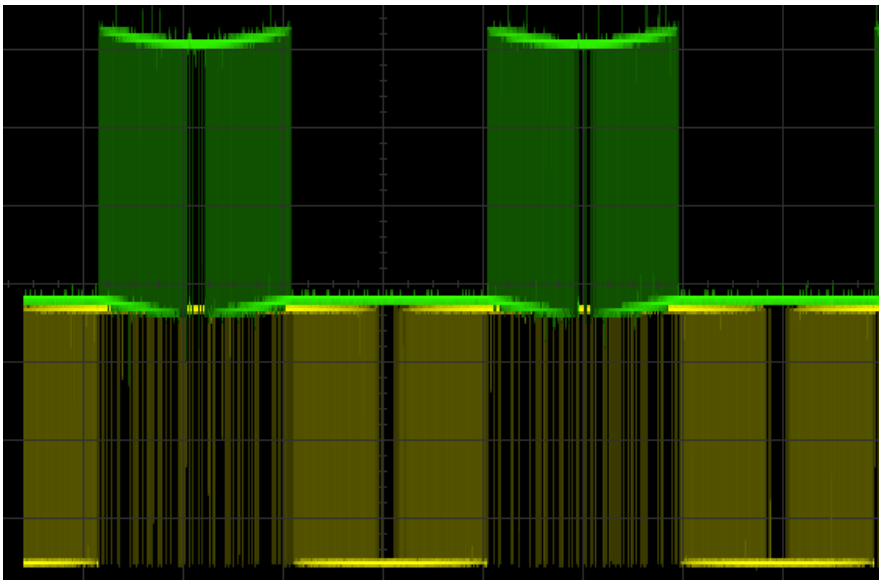

Figure 12: Sine wave split up over two signals where the yellow signal is the bottom portion of the wave while the green is the top portion of the wave

As one can see the bottom sine wave slowly increases in pulse width while the top portion is low. Once the top portion engages, the bottom PWM signal is constantly on until the top PWM signal reaches its peak and back down to the point where the two halves meet and then the

bottom portion decreases to being on none of the time as shown by the black break in the yellow and green signals.

After the signals were generated properly, one board would get connected to the lower half of the sine wave PWM and the other board would get connected to the upper half of the PWM. Once the boards are connected, the output of the board that is being controlled by the lower half of the sine wave will have a voltage source applied. Then the doubled voltage out of that board will be fed into the second board controlled by the upper half of the PWM. At the output of the second board, a motor or other load will be attached. Once the board and motor are working cohesively together, one will be able to calculate the input power as well as the output power. By determining the input and output power, one will be able to validate the efficiency of the Gallium Nitride switching devices.

Chapter 8

Research Results

As progress continues on this project, the circuit boards are functional, but are not ready for full testing. Up to this point, there has been simulation done on the circuitry utilizing Multisim 14.0. However, these simulations are just approximations of the actual efficiency of the Gallium Nitride transistors. In addition, these simulations were tested in which there was only a load resistance on the output of the circuit. Due to there only being a resistance on the output of the circuitry, the simulation results did not reflect how the circuitry would react to a load such as a motor that has both a resistance and an inductance. By simulating with a purely resistive load, it is impossible to accurately simulate the efficiency of the circuitry in an application where other loads other than a purely resistive load is used such as in a power plant. In addition, the simulation was done for one board and not both boards. Simulation for one board was done due to the amount of time it would take to simulate two boards. Also, the simulation was run with a regular square wave PWM signal and not a PWM signal representative of a sine wave. The simulation did not include the PWM signal that represents a sine wave because the simulation did not need to have a smooth oscillating sine wave because it was not running a motor. One is able to verify the operation of the circuit by seeing if the output switches between the input voltage and the doubled voltage. By knowing the input voltage and the doubled output voltage one is able to see how efficiently the circuit is operating.

When the circuit was actually simulated the following signal was produced.

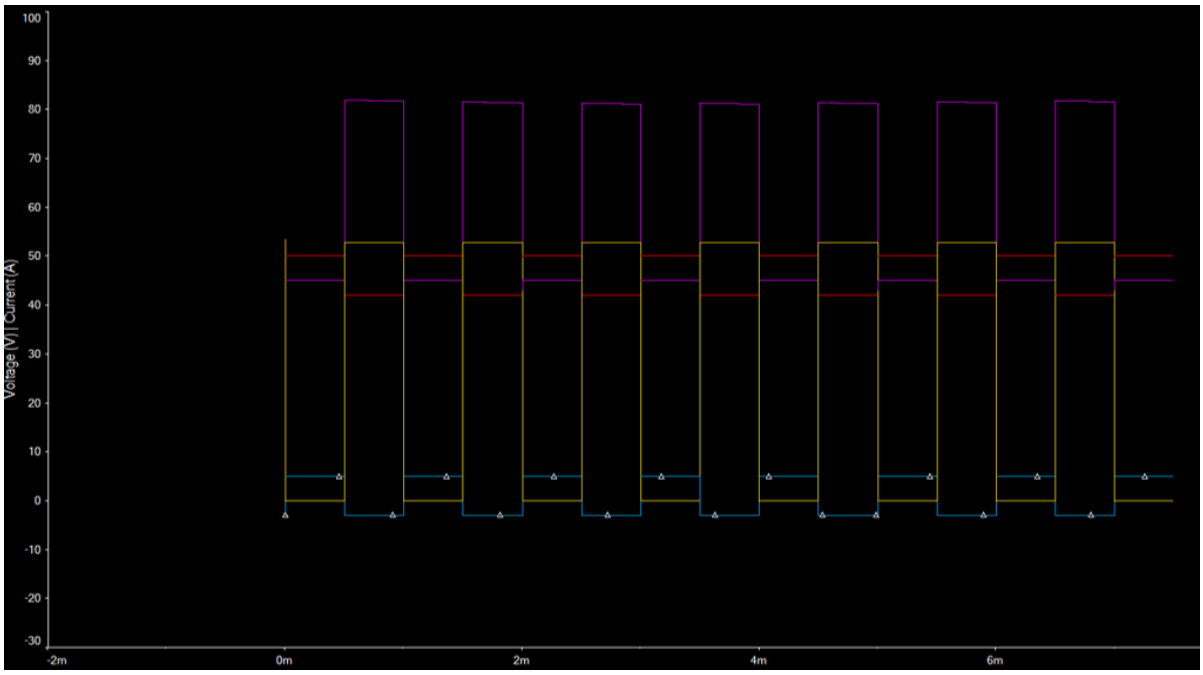

Figure 13: The purple waveform represents the switching output voltage while the other signals represent the control signals for the GaN devices

As one can see the output voltage switches between 45 volts and 80 volts. Ideally the voltage should have switched from 45 volts up to 90 volts. Since this was a simulation one should have seen a value that was very close to ideal, however this was not the case in this simulation. I believe the simulation did not give the expected values because the components within the simulation did not accurately represent the real-life component. For each component there is a mathematical model that represents the component. If the model is not correct then how the component functions within the circuit is affected. This could certainly be a possibility with the new GaN transistor models.

Due to the simulation results, this simulated circuitry shows that the circuitry operated at an efficiency of 89 percent. As mentioned above, ideally this efficiency should be much higher, but due to the possibility that the model for the GaN components could have been slightly off, the efficiency is much lower than the expected upper 90 to 100 percent efficiency.

Chapter 9

Future Work

In continuing work towards gathering efficiency data for the three-level inverter switched capacitor circuit, it is planned to obtain actual efficiency data by the end of the fall 2017 semester. This data will be used to compare the efficiency of the GaN transistors to the silicon carbide transistor. In addition, it is being planned that following the fall 2017 semester there will be continued work on this research project. The future proposed work is to delve into other circuit topologies to see how the GaN transistors affect the efficiency of the various other circuit topologies. It is with the knowledge of how the GaN transistors affect different circuit topology's efficiencies that more efficient control circuitry and consumer products such as cell phones could be designed and created.

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Hardware Engineering Intern

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- Work with full time engineers to design and develop test fixtures, products and other materials

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Project Management and Design Services Intern

- Wrote multiple informational guides to assist company employees in using Blue Beam Revu, the Physical Plant's purchasing software and the Physical Plant's method for starting drawings in AutoCAD
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