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AN OPEN-SOURCE BEACON RECEIVER FOR CUBESAT MISSIONS

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Abstract

This document presents the design of an open-source beacon receiver for *in situ* ionospheric total electron content (TEC) measurements. Its design was the result of optimizing the physical size and functionality of an existing ground-based TEC instrument that utilizes the Universal Software Radio Peripheral (USRP) and the GNU Radio software package. The specific areas of focus in this design included the field-programmable gate array (FPGA) selection process, radio-frequency (RF) front-end receive chain circuitry, and the development of a single printed circuit board (PCB) solution. This system was developed in order to provide a working proof-of-concept instrument, with the intent of integration with a CubeSat payload bus in future revisions.

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Acronyms

- ADC – Analog-to-Digital Converter
- ASPIRL – Applied Signal Processing and Instrumentation Research Laboratory
- AWG – American Wire Gauge
- BPF – Band-Pass Filter
- CDH – Command and Data Handling
- CIDR – Coherent Ionosphere Doppler Receiver
- COM – Communications
- DAC – Digital-to-Analog Converter
- DSP – Digital Signal Processing
- EMI – Electromagnetic Interference
- FPGA – Field Programmable Gate Array
- GPC – General-Purpose Computer
- GRBR – GNU Radio Beacon Receiver
- HDL – Hardware Description Language
- I/O – Input/Output
- ISR – Ideal Software Radio
- JTAG – Joint Test Action Group
- LEOS – Low Earth Orbit Satellite
- LED – Light-Emitting Diode

- LIDAR – Light Detection and Ranging
- LNA – Low-Noise Amplifier
- MMIC – Monolithic Microwave Integrated Circuit
- OSIRIS – Orbital System for Investigating the Response of the Ionosphere to Stimulation and Space Weather (CubeSat Mission)
- PCB – Printed Circuit Board
- PGRBR – Pico GNU Radio Beacon Receiver
- PLL – Phase-Locked Loop
- PVC – Polyvinyl Chloride
- QFP – Quad Flat Package
- RF – Radio-Frequency
- SCR – Software-Controlled Radio
- SDR – Software-Defined Radio
- SMA – SubMiniature Version A
- SNR – Signal-to-Noise Ratio
- SPI – Serial Peripheral Interface
- SWIG – Simplified Wrapper Interface Generator
- TDM – Time-Division Multiplexing
- TEC – Total Electron Content
- UHF – Ultra High Frequency
- USB – Universal Serial Bus
- USD – US Dollars
- USR – Ultimate Software Radio
- USRP – Universal Software Radio Peripheral, Version 1

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Chapter 1

Introduction

Today, measurements of space weather and the ionosphere are performed using one of two methods: remote sensing or *in situ* (also called direct) sensing. Remote sensing operations involve probing the medium of interest, not with a physical instrument, but with an electromagnetic or sonic wave [1]. Radar, LIDAR (Light Detection and Ranging), and Sonar systems are common examples of remote sensing systems. This type of sensing has the advantage that no sensor or instrument needs to be placed in the medium of interest. Measurements are taken without deploying (and likely expending) expensive sensors or probes. Ground-based remote sensing systems are powerful tools that can provide long-term data on large structures and events that occur in the ionosphere. Despite this advantage in the temporal domain, remote sensing systems are inherently limited in reconciling fine-grain spatial details. Probing with higher frequency electromagnetic waves provides better spatial resolution, but the waves are also more easily impeded in their forward and return paths. This is the fundamental challenge with remote sensing.

In situ measurements refer to those made directly within the medium of interest [1]. In the ionosphere, this type of measurement provides high spatial resolution, albeit for short intervals of time. Temperature and pressure are common properties that are measured *in*

situ. Highly accurate measurements can be made without signal path effects (present in remote sensing systems) distorting the results. In the case of atmospheric measurements, a vessel is needed to both house the instrument and relay its data. Spacecraft, such as satellites, sounding rockets, and long-duration balloons, make a convenient mechanism for this purpose. Unlike remote sensing, *in situ* sensing provides higher spatial resolution on small scale features, and provides access to certain processes in space physics that cannot be observed by ground-based systems [2]. However, its measurement scope is limited in time, as the support vehicle travels through the medium. Moreover, the presence of the probe or sensor can disturb or contaminate the medium of interest, providing readings influenced by the measurement itself.

This design presented in this work aims to provide an instrument capable of making *in situ* measurements of the total electron content (TEC) of the ionosphere in order to complement the results obtained previously by ground-based systems. The data with high spatial resolution obtained from the *in situ* measurements, along with the data with high temporal resolution obtained from the ground-based measurements, will help to provide better insight into the ionosphere and space weather. This insight will allow better understanding of the effects of space weather on communication and information systems. It will also enable more effective and robust communication technology to be developed.

1.1 Project Scope and Requirements

The GNU Radio Beacon Receiver (GRBR) is an open-source beacon receiver for measuring TEC, on which the design of this project, the Pico GNU Radio Beacon Receiver (PGRBR), was based. Nearly all of the elements of the GRBR could be optimized for the size and power constraints dictated by the the CubeSat form factor specifications. The scope of this revision of the PGRBR is limited to physical size optimization of all radio frequency (RF)

and digital hardware between the antennas and the general-purpose computer (GPC) in the receive chain. This includes the RF front-end (amplifiers and filters), the signal digitizers, and the data processing and transfer devices. The rationale for excluding the antennas from this design effort is that their design and construction for the CubeSat form factor is an extensive project in itself, with physical and electrical interface requirements that would vary widely across missions. Because estimation of the TEC requires high processing power for the intense calculations, it is unlikely that this step would be preformed on-board a satellite. Rather, the raw data would be transmitted to the ground via the satellite's Command and Data Handling (CDH) and Communications (COM) subsystems.

As a part of the design development of the PGRBR, a set of engineering requirements were established in order to drive the design decisions. These requirements are listed in Table 1.1, along with the rationale behind each. The PC/104 form factor described in Requirement 1 is illustrated in Figure 1.1.

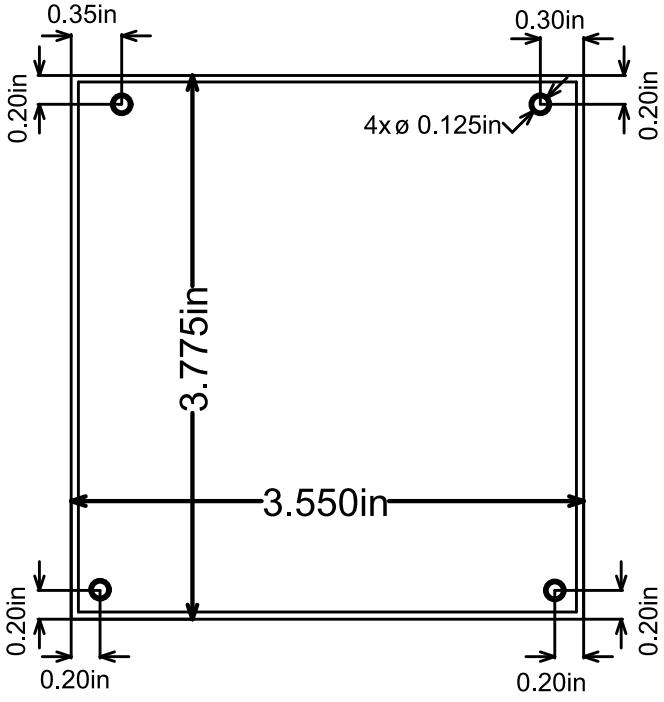


Figure 1.1: PC/104 Form Factor.

Table 1.1: PGRBR Design Requirements.

ID	*Name*	*Requirement*	*Rationale*
1	Form Factor	The PGRBR PCB shall follow the PC/104 form factor (illustrated in Figure 1.1).	CubeSat Kit is a popular commercial support bus system for CubeSats that utilizes the PC/104 standard [3]. This size PCB is optimal for the CubeSat form factor.
2	Power Supply	The PGRBR PCB shall be supplied by a single 5-V power bus.	The input power supply range for the USRP is 5–6V. 5-V is a common bus voltage for space electronics.
3	Functionality	All unnecessary hardware and logic functionality shall be removed from the GRBR design.	The USRP contains transmission functionality (hardware and logic) that is not needed for the GRBR. By removing this functionality, a more optimized system will be designed.
4	Compatibility	This revision of the PGRBR PCB shall be interchangeable with the GRBR receive chain.	Interchangeability will allow verification the PGRBR's performance against the GRBR.
5	Assembly and Verification	The components shall be selected such that they can be soldered by hand and verified visually.	The PGRBR will be assembled by hand and soldered by hand. All solder joints (except ground pads) need to be visually inspected for electrical and physical ruggedness.

1.2 Thesis Overview

This document provides a comprehensive discourse of the first revision of the PGRBR system. Chapter 2 develops the necessary background information for context and the understanding of the project. Chapter 3 details the selection process for the field-programmable gate array (FPGA) as a part of the digital hardware design. Chapter 4 presents the process used in selecting and designing the anti-aliasing filters and amplifiers. Chapter 5 explains the process and design strategies used in developing the PGRBR Printed Circuit Board (PCB). Chapter 6 summarizes the design process and results and provides direction for future efforts on the

project. Appendix A contains S-parameter plots for the RF hardware discussed in Chapter 4. Appendices B and C contain the schematic diagrams and PCB layout designs, respectively, for the PGRBR PCB. Appendix D outlines the basic operational procedures developed in preliminary testing.

The PGRBR system is currently still under development. This document represents the state of the project at the time of writing. All project design files and updates are freely available (i.e., open-source) for further study and development, and are located on the web server for the Applied Signal Processing and Instrumentation Research Laboratory (ASPIRL) in the Electrical Engineering department at the Pennsylvania State University.

Chapter 2

Background

The GRBR and PGRBR are multi-disciplinary projects, spanning the areas of remote sensing, communications, and signal processing. Before detailing the design of the PGRBR, several concepts will be discussed in this chapter to develop the necessary background for understanding and further developing the system.

2.1 Software-Defined Radio

Although the fundamental theories behind radio communications have remained relatively constant for the past half a century, physical implementations of these systems have changed significantly over the years [4]. Once based entirely in hardware, radio systems with software elements are becoming increasingly popular. Advances in the digital signal processing (DSP) capabilities of microprocessors and other specialized processing units have allowed the development of these "software-defined radio" (SDR) systems to grow at an accelerating rate. The use of DSP in SDR systems allows conventional hardware elements, such as filters, mixers, signal generators, demodulators, etc., to be implemented in software, with performance levels that rival or exceed those of hardware radio systems. These systems are flexible in the sense that the functionality of an SDR can be completely changed simply by

changing the software [5]. In hardware radio systems, operational flexibility comes with a steep price attached, and its flexibility may be limited to support for different modulation schemes. SDR systems, however, can be completely redefined by a change in software, with the only cost being the development costs of the new software functionality.

Radio systems can be classified in a set of five tiers of increasing in software control and capabilities [6]. Tier 0 is defined by conventional hardware radio systems. These systems may offer minimal flexibility, and none via software control. Tier 1 is characterized by software-controlled radio (SCR) systems, which are radio systems that use software for control functionality, but have hardware-defined RF characteristics, such as frequency and modulation scheme. Many modern cellular phones utilize SCR. The next level, Tier 2, is characterized by software-defined radio systems. SDR provides additional flexibility and improvements to SCR, including software controlled RF waveforms, wide- and narrow-band operation, simultaneous multi-functional operation, and modifiable functionality. While they are powerful platforms, SDR systems still require RF front-end hardware (amplifiers, filters, etc.) and an analog-to-digital converter (ADC) or digital-to-analog converter (DAC) to transfer between the digital and analog (i.e., real-world) domains. Tier 3 is known as the ideal software radio (ISR), and it features all the functionality of SDR, in addition to high-speed and extremely sensitive ADCs and powerful DACs to eliminate the need for an RF front-end. Finally, the top tier, Tier 4, is called the ultimate software radio (USR). This system is an all-encompassing software radio chip that can operate on all frequencies, with all types of modulation schemes, without the need for an external antenna. The feasibility of the implementation of a USR system is still very low. For this reason, its purposes are to provide a benchmark for other systems to compare against and to drive the software radio technology further up the tiers. At this point, even the best software radios available are Tier 2 software-defined systems.

One important application of SDR is interoperable communication systems [7]. During

disaster events, such as the terrorist attacks on 11 Sept. 2001 or Hurricane *Katrina* in 2005, a lack of interoperable communication systems between firefighters, police forces, and other emergency responders only added complications and reduced the effectiveness of their rescue efforts. With the development of smart radio systems that can "bridge" the communication networks together, future rescue efforts will be more timely and effective, with the potential to save more lives of those in danger.

2.1.1 Universal Software Radio Peripheral

A variety of SDR hardware platforms exist today, including a popular open-source platform called the Universal Software Radio Peripheral (USRP) developed by Ettus Research (now a subsidiary of National Instruments) [8]. The USRP is a modular hardware platform designed specifically to meet the reconfigurability needs of SDR systems. It consists of a motherboard that includes functionality to handle signal processing and interfacing to a general-purpose computer (GPC), and a number of pluggable daughterboards that provide various transmit and receive capabilities. Because of its affordability and flexibility via various daughterboards, the USRP is the SDR platform of choice for a wide variety of different projects, including space research; terrestrial, underwater, and underground communication; signal processing education; and amateur stations [8]. There are several different generations of the USRP currently available, including the USRP1, USRP2, USRP E100, and USRP N200 series products. For this application, the USRP1 was used and herein will be referred to as the USRP. Figure 2.1 shows the USRP with the two daughterboards used in the GRBR, the BasicRX and the RFX-400.

Figure 2.1: The USRP1 with BasicRX (top left) and RFX-400 (right) Daughterboards.

2.1.2 GNU Radio

The USRP is a hardware platform that enables SDR, but it still needs software to operate it. The GNU Radio software package is a powerful open-source toolkit for developing software radio systems that has undergone extensive development using the USRP [9]. This software features both a signal processing run-time and an extensive library of software processing "blocks," allowing both real-time and offline operational modes. Each signal processing block has a specific functionality, such as a filter, demodulator, or signal source. Software radio designs are constructed in the form of signal flowgraphs, made up of two or more functional blocks. Every design needs at least one signal "source" and one signal "sink," each of which could be the USRP, data files, or other devices. Figure 2.2 illustrates a typical flowgraph that might be used for simultaneously listening to and recording a received radio signal. In this figure, the USRP is configured as a receiver and it "sources" the received signal to GNU Radio over the Universal Serial Bus (USB) connection. After it is digitally processed by the filters and demodulator, the output file and sound card "sink" the signal. In this fashion, complex digital transceiver systems are built by simply connecting software signal blocks.

Each block is written as a standalone object in C++. Although the blocks can be instantiated and connected in a C++ environment, the preferred (and more documented)

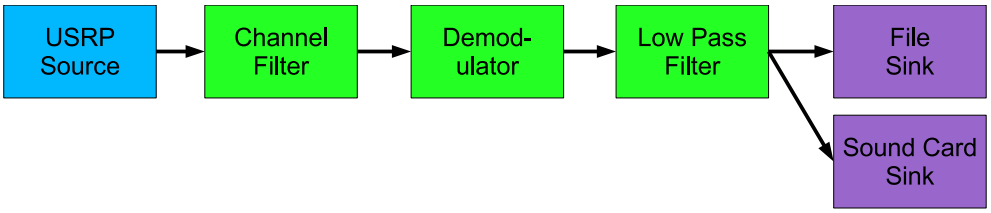


Figure 2.2: A Typical GNU Radio Flowgraph.

method of generating flowgraphs is using a Python interface. A C++ interface wrapper, called the Simplified Wrapper Interface Generator (SWIG), is used to tie the C++ blocks directly into the Python scripts. This allows the user to rapidly develop and test complex software radios, without the dealing with the technical intricacies of C++.

2.2 GNU Radio Beacon Receiver

The GNU Radio Beacon Receiver (GRBR) is an open-source beacon receiver system developed by Dr. Mamoru Yamamoto at Kyoto University, Japan [10]. Utilizing both the USRP and GNU Radio, low Earth orbit satellite (LEOS) beacon signals are received and digitized in order to calculate the total electron content (TEC) of the ionosphere. Excellent correlation has been shown between the GRBR and an analog Coherent Ionosphere Doppler Receiver (CIDR). Additionally, the GRBR can be constructed for about one-tenth the cost of the CIDR.

2.2.1 Total Electron Content

Ionospheric total electron content (TEC), or "total number of electrons present along a path between two points" [11], is an important atmospheric parameter for calculating and understanding scintillation and group delay of radio waves through the atmosphere. By measuring the carrier phase shift of a radio signal traveling through the atmosphere, the

ionospheric TEC can be calculated by

$$\Psi = \frac{2\pi f}{c} L - \frac{\pi A}{cf} \int N dx + \eta, \tag{2.1}$$

where Ψ is the total measured carrier phase, f is the carrier frequency, c = 3×10^8 m/s is the speed of light, L is the propagation path length, $\int N dx$ is the TEC, and η is an unknown phase bias constant [10]. Many factors contribute to the TEC, including geographic position, time of day, Earth's current position with respect to the Sun, and the current phase of the solar cycle [11]. One method of resolving the inherent path length ambiguity of Equation 2.1 is to make simultaneous phase measurements at two or more frequencies. The GRBR uses LEOS beacon signals at 150 MHz and 400 MHz, which are both integer multiples of a common frequency, f_r = 50 MHz. The phase difference between the two received signals Ψ is

$$\Phi = \frac{\Psi_{150}}{p} - \frac{\Psi_{400}}{q} = \frac{\pi A}{f_r c}(q^{-2} - p^{-2}) \int N dx + \eta', \tag{2.2}$$

where Ψ_{150} and Ψ_{400} are the total phase measurements made at 150 and 400 MHz, respectively, and p and q are the integer ratios between the measurement frequencies and f_r, 3 and 8, respectively [10]. Although a phase bias, η', remains, calibration procedures can be used to find this constant. In the case of the GRBR, post-processing in a Python script is used to calculate the TEC from the measured phase data.

2.2.2 System Overview

Illustrated in Figure 2.3 is the system diagram for the GRBR [10] [12]. Signals received by the 150- and 400-MHz antennas are conditioned through the use of analog amplifiers and filters, before being passed to the USRP daughterboards. Using digital down-conversion techniques (discussed in Section 4.2), the 150-MHz signal can be applied directly to the ADC on the USRP. The same technique cannot be performed on the 400-MHz signal, so

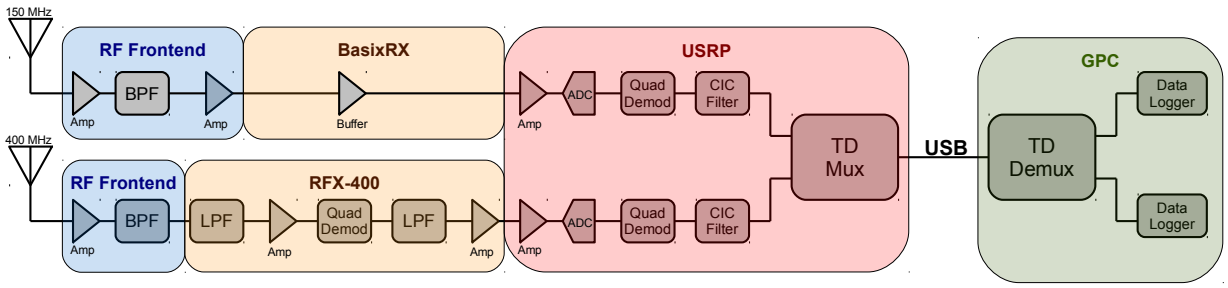


Figure 2.3: System Diagram for the GNU Radio Beacon Receiver.

additional circuitry on the RFX-400 daughterboard demodulates and down-converts it before applying it to the ADC. Once the signals are digitized, the FPGA on the USRP performs additional digital processing (simultaneously on both channels), before the data is transferred using time-division multiplexing (TDM) over a USB connection to the host GPC. The GNU Radio software interfaces with the USRP, demultiplexing the data and storing each channel as a complex data log.

The antennas used to capture the satellite beacon signals are of the Quadrafiliar Helix (QFH) design. This type of antenna has a quasi-omnidirectional beam pattern [10], which is perfect for tracking satellites as they pass overhead because no tracking system is necessary to adjust the antenna position. In order to avoid phase variation between the two beacon signals, the 400-MHz antenna was nested directly inside the 150-MHz antenna, shown in Figure 2.4. Both antennas were constructed with 12 American Wire Gauge (AWG) copper wire and polyvinyl chloride (PVC) pipe.

2.3 CubeSat

Often, *in situ* sensing experiments consist of a sensor array that helps to provide a greater understanding of the measurements made, as well as increase the system's tolerance to failures. For ionospheric and space weather applications, an array of artificial satellites

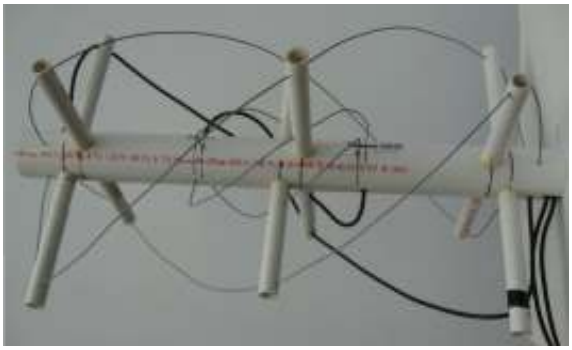


Figure 2.4: The QFH Antennas for the GRBR (rotated for formatting).

makes an excellent measurement platform. CubeSats are small (10 cm on a side and less than 1.33 kg in mass), relatively inexpensive cube-shaped pico-satellites that make prime candidates for such applications [13]. All CubeSats follow a standard specification developed by the California Polytechnic State University, allowing them to piggy-back on almost any spaceflight operation, with minimum integration efforts needed.

The CubeSat is a popular platform for developing low-risk satellites for instrumentation and communication systems. Due to their form factor and inexpensive nature, the development timeline for a fully-functional CubeSat could be less than a year. There are over 60 universities and high schools participating in the CubeSat Program, and that number is growing [13]. Many companies are producing commercial off-the-shelf (COTS) components and payload buses for quick and easy integration into a CubeSat mission, such as the Pumpkin CubeSat Kit [3]. The development of this project will provide CubeSat design teams with a low-cost science instrument requiring minimal system integration efforts.

2.4 Summary

In this chapter, several important concepts and background were discussed to familiarize the reader with the technologies used in the design of the PGRBR. The next three chapters will detail the design utilizing the concepts and technologies previously described.

Chapter 3

Field-Programmable Gate Array

A number of aspects of the GRBR system were considered for minimization in order to fit the requirements listed in Table 1.1. The first area considered was the central processing unit of the USRP system: the field-programmable gate array (FPGA). Because the USRP is capable of simultaneously transmitting and receiving signals on two channels each (four channels total), there is considerable unnecessary functionality enabled by the FPGA on the USRP for the application of the proposed PGRBR system. This chapter will present brief background information about FPGAs, provide a summary of the characteristics of this type of device used on the USRP, and detail the selection criteria used in choosing a new FPGA for the PGRBR system.

3.1 Background

Field-programmable gate arrays (FPGAs) are multi-purpose logic devices that have become popular in recent years for their flexibility, relatively low power, and high parallel processing capabilities. FPGAs have found their way into many different fields, including communication systems, signal processing, medical applications, and aerospace systems, among others. For instance, software-defined radio systems have benefitted greatly by the flexibility and

speed FPGAs offer. The USRP, an FPGA-based system, is an exceptionally powerful open-source platform for communications and signal processing, with the advantage that it can be produced and sold at a fraction of the cost of conventional radio systems.

One method of designing the internal logic of an FPGA is through the use of a hardware description language (HDL), such as Verilog or VHDL. Unlike traditional programming languages, the execution of HDL code is parallel, not sequential. FPGAs' extreme processing capabilities are fostered by this parallelized architecture. Rather than a single instruction, the entire logic design is operated on one clock cycle. Modularized units can be constructed and linked together to form large, complex systems on a single chip. Before implementing a design on an FPGA, the code is synthesized into a bitstream, which in turn is used to configure the FPGA over a hardware interface, such as Joint Test Action Group (JTAG) or Serial Peripheral Interface (SPI).

Currently, general-purpose and specialized FPGA devices are produced by four major FPGA manufacturers (Xilinx, Altera, Actel, and Lattice). The device costs range from several dollars a chip for hobbyist and small designs to well over $15,000 a chip for systems that require extremely high-end performance and reliability. It is expected that, as technology progresses, FPGAs will continue to find more areas of application in which parallel computing is advantageous.

3.2 Altera Cyclone Family

Although many devices from the various FPGA manufacturers could handle the USRP logic design, a device from the Altera Cyclone family was chosen to support the USRP. This family of FPGAs includes low-cost, low-power devices that are suitable for small-to-medium design projects that do not require many advanced features or high computational power. Several basic FPGA features (by today's standards) are included on these devices, such as internal

memory blocks, internal clock and timing circuits, support for various signal interfaces, and support for soft microprocessors. Altera has continued to develop and optimize these devices in the newer Cyclone II, III, and IV families. The Altera Cyclone family of devices is roughly comparable to the Xilinx Spartan family of FPGAs in terms of performance, features, and cost.

The Cyclone EP1C12Q240 is used on the USRP. Specifically, this FPGA has about 12,000 internal logic elements, about 530 kilobits of internal memory (including RAM blocks), up to 173 general-purpose I/O connections, and 2 internal phase-locked loops (PLLs). The standard FPGA image (used on the USRP) build results provided in Table 3.1 indicate that the USRP makes nearly full use of the resources provided by this Cyclone device.

Although HDL designs are nearly completely portable between different vendor's design tools and devices, the associated project files, configurations, and constraints files are not cross-compatible. For this application, there were no FPGA features needed that the Altera Cyclone family could not fulfill. Therefore, it was decided that in order to minimize changes from the USRP system, other than to strip unnecessary functionality, the Altera Cyclone family would be maintained in the PGRBR system. An effective selection process, with minimum feature trade-offs was enabled by the relatively large selection of Cyclone family devices available. The Cyclone I, II, and III classes of devices are the focus of this trade study.

3.3 Selection Criteria

There were several factors involved in determining which FPGA was most suitable for this design, including package style, I/O pins, and internal logic and memory characteristics. These factors considered both the physical and electrical aspects of FPGA system design and are discussed in the following sections.

3.3.1 Package Style

Current FPGA technology is generally sold in two different package styles: quad flat package (QFP) and ball grid array (BGA). The former style features pin connections along the four edges of a square package. This allows the package to be soldered to the PCB by hand or using a solder-reflow oven. Because all the pins are located along the edge, every contact between the device and the PCB can be visually inspected and verified.

On a BGA-style package the pin connections are located in a grid array across the bottom of the chip. Each pin has a small ball of solder that contacts the corresponding grid of pads on the PCB. In order to populate a BGA package device, a solder-reflow oven must be used. Because many pins are not located around the outer edge of the chip, their connection to the PCB cannot be visually verified. A typical verification method for BGA technology is the use of X-ray imaging devices.

The FPGA on the USRP (Altera Cyclone EP1C12Q240) uses a QFP-style package. In order to meet Requirement 5 in Table 1.1, the QFP-style package must also be used on the PGRBR, as visual verification of pin connections is inhibited by the BGA-style package, whereas visual verification is possible with the QFP-style. BGA-packaged devices typically have higher pin densities than QFP/QFN packages and consequently higher-end and newer FPGAs (with more I/O pins) typically use the BGA package style. In the USRP application, a lower-end FPGA is sufficient and thus devices that meet the internal logic requirements are available in QFP-style packages.

3.3.2 I/O Pins

There were two factors related to I/O pins that needed to be addressed when selecting a new FPGA: number of available I/O pins and the logic-level compatibility. Because the transmission feature was removed from the USRP in minimizing the system, the number

of necessary I/O pins on the FPGA was significantly reduced. Consequently, physically smaller devices were considered. The modified FPGA bitstream contains connections to the additional I/O pins for debugging purposes, so the modified design by itself requires only 81 I/O pins, as shown in Table 3.2.

As semiconductor devices continue to shrink and consume less power, the logic-level voltages are also being reduced. The Altera Cyclone device on the USRP uses a 3.3-V CMOS logic interface on its I/O banks, and is also compatible with 2.5-V, 1.8-V, and 1.5-V logic-levels, depending on configuration. The digital circuitry on the USRP uses 3.3-V logic. In order to retain compatibility with these devices, 3.3-V logic-level capability was a necessary design criterion. All of the Altera devices beyond the Cyclone III family are either incompatible or only partially compatible with 3.3-V logic-level interfaces, so only the older model devices were considered.

3.3.3 Internal Logic and Memory

Another important consideration in FPGA selection was the number of internal logic elements and memory available in each device. Because the HDL logic design for the PGRBR was reduced from the standard USRP bitstream, fewer logic elements were required to fit the design. As listed in the build results provided in Tables 3.1 and 3.2, there was approximately a 20% reduction in the total number of logic elements between the standard and modified USRP bitstreams. An additional logic element reduction is shown by the results of the Cyclone III device, due in part to the additional functionality on their logic blocks compared to the Cyclone device. Another explanation for the notable decrease in total logic elements used is more direct signal routing between logic elements, thus requiring fewer elements to be dedicated for signal routing.

Each family of Cyclone devices contains several different models with varying numbers of total logic elements and memory. Because the HDL logic design is unlikely to change

in future revisions of the PGRBR, extra logic elements and memory for contingency are not necessary. Therefore, the smallest devices (in terms of number of logic elements and memory) that fit the modified USRP bitstream were evaluated as potential candidates for the PGRBR.

3.3.4 Other Considerations

Two other characteristics examined in selecting an FPGA for the PGRBR were power consumption and clock rate. Although they were not driving criteria for the decision, their consideration will be important in future revisions of the PGRBR.

Power consumption of FPGAs is difficult to accurately quantify because it is highly dependent on the nature of the logic design. In general, however, a smaller device (in terms of internal logic elements) will consume less power than a larger one. This is mainly due to leakage currents and switching losses present in all the logic elements [14].

The FPGA and mixed-signal front-end devices on the USRP are clocked at 64 MHz. In order to retain compatibility with the other devices on the USRP, it was necessary for the the maximum clock rate of the new FPGA to be greater than 64 MHz. All of the devices in the Cyclone families met this requirement, so consideration beyond this clock rate was not necessary. Future revisions may deviate from the 64 MHz clock rate and, therefore, this criterion may need to be considered more carefully.

3.4 Build Statistics

Another method of gauging different FPGA devices against each other for a particular design is to compile the design for each device and compare results. The ability to customize and generate bitstreams for specific devices is featured in the Altera Quartus II design software. Because the HDL logic design is abstracted from the low-level hardware details specific to

Table 3.1: Summary Altera Quartus II Build Results for the Original USRP Bitstream.

	EP1C12Q240
Total Logic Elements	11,071 / 12,060 (92%)
Total I/O Pins	173 / 173 (100%)
Total Memory Bits	150,528 / 239,616 (63%)

each device, porting the design from one FPGA to another can be as simple as regenerating the bitstream (depending on the available internal logic, I/O pins, etc. of the target device). In this way, the modified USRP HDL logic design was generated for several different devices, with a summary of relevant results from the builds provided in Table 3.2. A build of the modified bitstream on both the Cyclone device used on the USRP and the Cyclone III device selected for use in the PGRBR shows that significantly fewer I/O pins were left unused on the latter, signifying it is more optimal for this design.

3.5 Conclusion

After a list of available FPGAs was narrowed down, the Cyclone I/II/III family devices that met the selection criteria were tabulated in Table 3.3. Of the listed devices, the two with the smallest package footprint were the EP2C8T144 and the EP3C10E144 devices. These devices were smaller than the others listed, mainly due to their lower pin count. A physical size comparison of the EP1C12Q240 (on the USRP) and the EP3C10T144 devices is shown in Figure 3.1. The EP3C10E144 had several more I/O pins and and more internal logic elements (which are both useful for debugging) available than the EP2C8T144 device. The

Table 3.2: Summary Altera Quartus II Build Results for the Modified USRP Bitstream on Several Cyclone FPGAs.

	EP1C12Q240	*EP3C10E144*
Total Logic Elements	8,684 / 12,060 (72%)	7,607 / 10,320 (74%)
Total I/O Pins	81 / 173 (47%)	81 / 95 (85%)
Total Memory Bits	76,800 / 239,616 (32%)	76,800 / 423,936 (18%)

Figure 3.1: Size Comparison Between the EP1C12Q240 and EP3C10T144 Devices.

other devices listed all had either significantly more I/O pins and/or internal logic elements than minimum necessary for the modified FPGA bitstream. All of the devices in Table 3.3 are compatible with 3.3-V logic-level interfaces, which is important in interfacing with the other devices on the USRP. The only caveat with interfacing is that it is required by the Cyclone III devices that series termination resistances be applied in order to limit the input current to the FPGA to a lower level than is tolerated by the Cyclone and Cyclone II families. Finally, the modified USRP HDL logic design was compiled in the Altera Quartus II design software for each device, and all were successful except the EP2C8T144, due to lack of logic elements for internal routing to all the I/O pins. From these considerations, the best Cyclone device for this application was the EP3C10T144 (Cyclone III) and it was consequently selected for use in the PGRBR design.

Table 3.3: Cyclone I/II/III Family Devices Considered for Use on the PGRBR.

Device	*Package*	*I/O Pins*	*I/O Logic-Level*	*Logic Elements*	*Builds in Quartus?*
EP1C12Q240	PQFP-240 (34.6 mm × 34.6 mm)	173	3.3-V, 2.5-V, 1.8-V, 1.5-V	12060	Y
EP2C20Q240	PQFP-240 (34.6 mm × 34.6 mm)	142	3.3-V, 2.5-V, 1.8-V, 1.5-V	18752	Y
EP2C8Q208	PQFP-208 (30.6 mm × 30.6 mm)	138	3.3-V, 2.5-V, 1.8-V, 1.5-V	8256	Y
EP2C8T144	TQFP-144 (22.0 mm × 22.0 mm)	85	3.3-V, 2.5-V, 1.8-V, 1.5-V	8256	N
EP3C10E144	TQFP-144 (22.0 mm × 22.0 mm)	95	3.3-V, 2.5-V, 1.8-V, 1.5-V, 1.2-V	10320	Y
EP3C16Q240	PQFP-240 (34.6 mm × 34.6 mm)	160	3.3-V, 2.5-V, 1.8-V, 1.5-V, 1.2-V	15408	Y
EP3C25Q240	PQFP-240 (34.6 mm × 34.6 mm)	148	3.3-V, 2.5-V, 1.8-V, 1.5-V, 1.2-V	24624	Y
EP3C25Q240	PQFP-240 (34.6 mm × 34.6 mm)	128	3.3-V, 2.5-V, 1.8-V, 1.5-V, 1.2-V	39600	Y

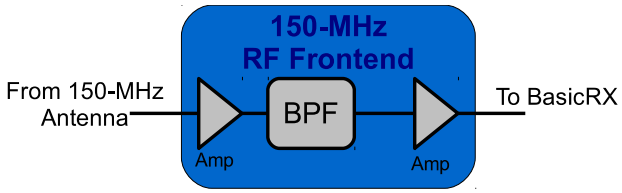
Chapter 4

RF Front-End

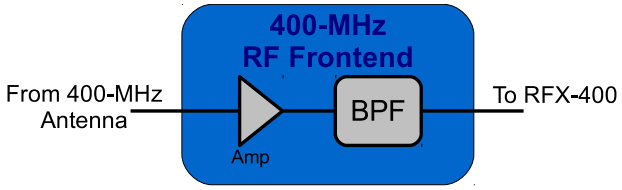
Despite the flexibility of software-defined radio systems, there are still some limitations that differentiate them from ideal software radios. As discussed in Section 2.1, SDR systems require an RF front-end for signal conditioning before being digitized (on the receiver side) or after being synthesized (on the transmitter side). Because the PGRBR uses two receive channels, two separate RF front-ends are required before signal digitization. The block diagrams of these analog conditioning paths for the 150-MHz and 400-MHz channels are illustrated in Figure 4.1. On each channel, the received signal is amplified using a tuned preamplifier. Band-pass filters further reject unwanted out-of-band spectral energy. The 150-MHz signal is then amplified with a wideband amplifier to increase its signal level into the range measurable by the ADC on the mixed-signal front-end device. The 400-MHz signal does not require additional amplification (following the band-pass filter) because the RFX-400 circuitry already contains an additional amplifier.

4.1 Preamplifiers

The RF signals received by the GRBR/PGRBR are very weak and, as discussed in Chapter 2, practical limitations of the digital hardware necessitate an RF front-end. Several stages



(a)



(b)

Figure 4.1: (a) 150-MHz and (b) 400-MHz Channel RF Front-End Block Diagrams.

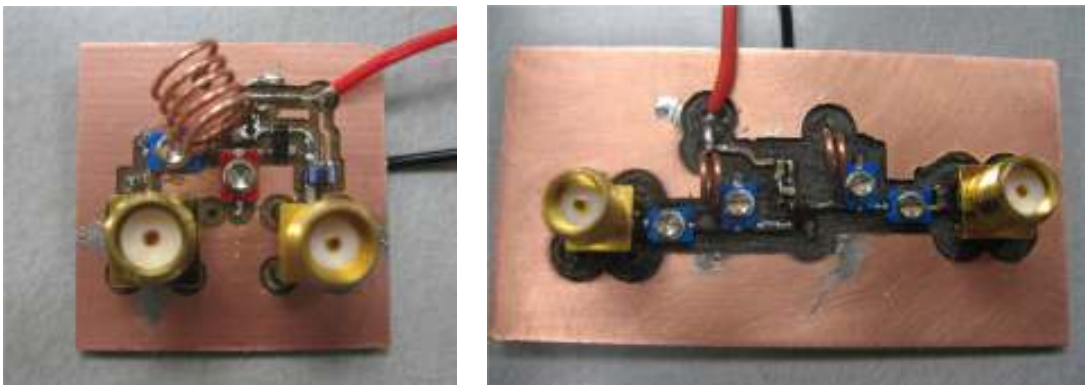
of amplification are used in the GRBR. Preamplifiers are low-noise amplifiers (LNAs) that are tuned to amplify only a specific frequency band. The purpose of the input preamplifiers is to both amplify and band-pass filter the RF energy received by the antennas. Figure 4.2 shows the Hamtronics LNK-series preamplifiers recommended for the GRBR [12].

Because these preamplifiers were designed to be powered by a 12-V power supply, direct application of their design to the PGRBR was not possible (without the use of a step-up switching voltage regulator), due to Requirement 2. However, with careful study of the preamplifier design, modification of the circuit to be powered by a 5-V power supply was

(a)

(b)

Figure 4.2: Hamtronics (a) LNK-146 and (b) LNK-450 Receiver Preamplifiers.



(a) (b)

Figure 4.3: Prototypes of (a) LNK-146 and (b) LNK-450 Preamplifiers Powered by 5 V.

possible. In the original design of each preamplifier, an 8-V linear voltage regulator was used to provide a voltage reference for biasing the transistor. By completely bypassing this regulator, the preamplifiers tolerated the 5-V power supply, even though the transistors were biased at a slightly lower bias voltage. Minimal effects on performance were observed, so prototypes of the modified preamplifier designs were constructed. Figure 4.3 shows the modified LNK-series preamplifiers. The prototypes were designed with with the goals of confirming both 5-V operation and the feasibility of size reduction.

In order to characterize the prototype preamplifiers, the *S*-parameters were measured and compared to *S*-parameters of the LNK- preamplifiers. This set of measurements was obtained with a 12-V power supply for the LNK- devices (as suggested for nominal operation) and a 5-V power supply for the prototype preamplifiers.

4.1.1 150-MHz Preamplifier

The *S*-parameter magnitude and phase responses of the LNK-146 and the 150-MHz prototype preamplifier are plotted in Appendix A. For simplicity, several metrics of comparison were used to compare the responses, and these results are summarized in Table 4.1. The S_{21} magnitude and phase responses of the original preamplifier and the prototype were overlaid

Table 4.1: 150-MHz Preamplifier Results Summary

Preamplifier	LNK-146	150-MHz Prototype
Center Frequency (MHz)	151.5	150.5
Bandwidth (MHz)	8.0	6.0
Gain (dB)[1]	20.1	20.6
Noise Floor (dB)	−40	−48
Input Reflection (dB)[1]	−7.0	−10.0
Forward Phase Shift (^{o})[1]	43.1	141
Size (mm)	114 × 38 × 29	22 × 22 × 13
Supply Current (mA)	10.58	10.00

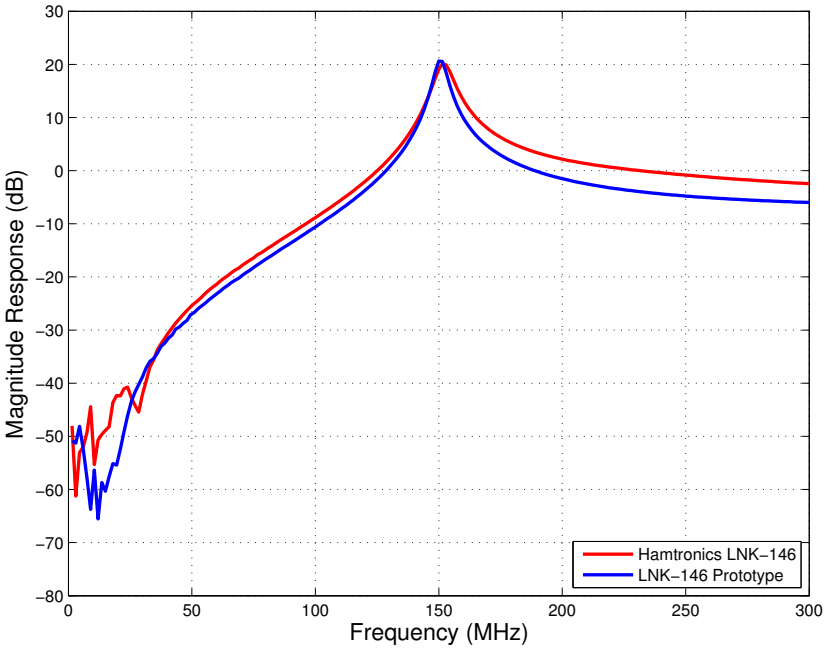
for direct comparison in Figure 4.4.

The responses of both the LNK-146 and the prototype amplifier show very similar characteristics. Both preamplifiers are centered close to the ideal center frequency (150 MHz) and have a narrow bandwidth, which helps to reject out-of-band energy. Both preamplifiers had similar forward gains and the input reflections, with the prototype preamplifier exhibiting slightly better results for both. As indicated on the S_{21} magnitude plot, the noise floor is slightly lower for the prototype, which also helps to reject unwanted RF energy. The only significant difference between the preamplifier responses was the forward phase shift at 150 MHz. While there is no specification on the absolute phase shift, it is important to keep the net phase shift between all elements of the 150-MHz and 400-MHz receive chains the same, as TEC measurements are based on the phase difference between the two channels. Tuning capacitors on both preamplifiers allow for phase response adjustments, so this is not a major concern.

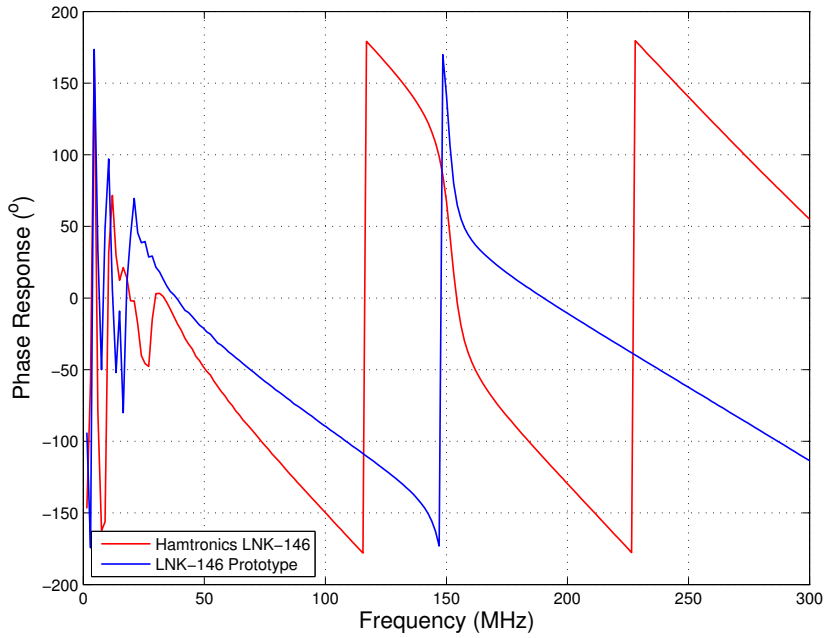
4.1.2 400-MHz Preamplifier

As with the 150-MHz channel preamplifiers, the *S*-parameter magnitude and phase responses of the LNK-450 and the 400-MHz prototype preamplifier are plotted in Appendix A. The

[1] At 150 MHz.



(a) Magnitude Responses



(b) Phase Response

Figure 4.4: S21 (a) Magnitude and (b) Phase Responses of the 150-MHz Preamplifiers.

Table 4.2: 400-MHz Preamplifier Results Summary

Preamplifier	LNK-450	400-MHz Prototype
Center Frequency (MHz)	398	401
Bandwidth (MHz)	50	34
Gain (dB)[2]	15.2	16.7
Noise Floor (dB)	−52	−48
Input Reflection (dB)[2]	−4.5	−10
Forward Phase Shift (^{o})[2]	170	−48
Size (mm)	114 × 38 × 29	41 × 13 × 13
Supply Current (mA)	10.26	8.76

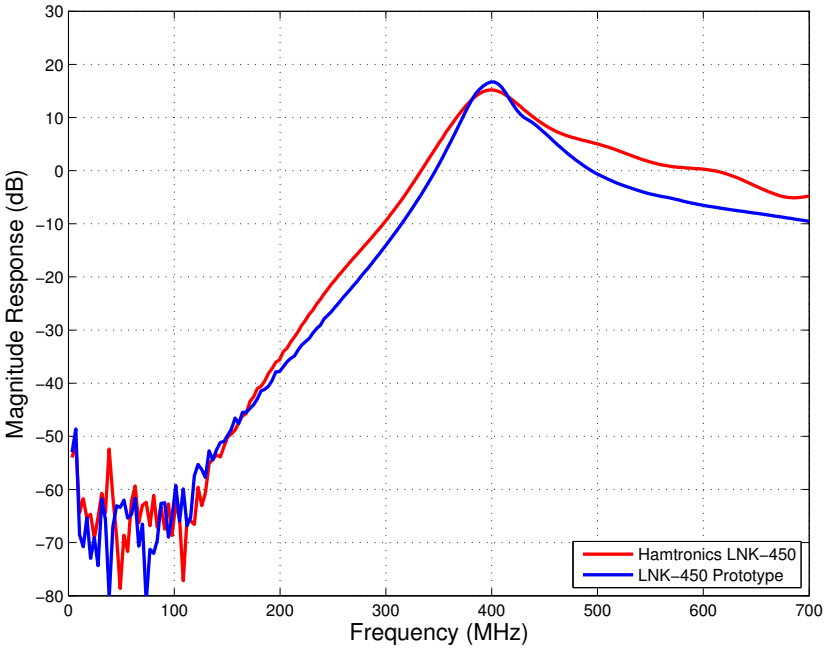
same comparison metrics as used for the 150-MHz preamplifiers were used to characterize the 400-MHz preamplifiers, as listed in Table 4.2. Figure 4.5 illustrates the S_{21} magnitude and phase plots of the LNK-450 and the prototype preamplifier overlaid.

The LNK-450 and prototype preamplifiers exhibit similar frequency response characteristics, with the prototype slightly outperforming the LNK-450. Both preamplifiers are centered close to the target frequency (400 MHz), but the prototype is slightly more narrowband than the LNK-450. This, in addition to the lower input reflection at 400 MHz, indicate slightly better out-of-band rejection. An additional 1.5 dB of gain at 400 MHz is also a favorable property of the prototype preamplifier. As previously mentioned, the phase shift discrepancy is not an issue because it is assumed that tuning of the entire receive chain will eliminate the phase shift between the 150-MHz and 400-MHz channels.

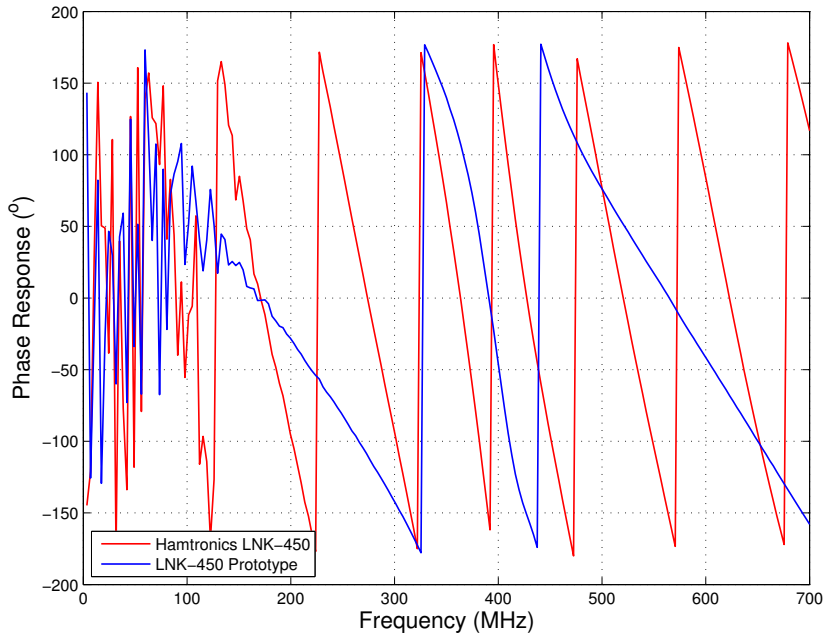
4.2 Band-Pass Filters

Like many software-defined radio systems, the GRBR makes use of a technique known as digital down-conversion, which takes advantage of an otherwise undesirable effect, aliasing, caused by the sampling of a continuous-time signal. The frequency folding that occurs at multiples of one-half the sampling frequency, due to the ambiguity imposed by the Nyquist

[2]At 400 MHz.



(a) Magnitude Responses



(b) Phase Response

Figure 4.5: S21 (a) Magnitude and (b) Phase Responses of the 400-MHz Preamplifiers.

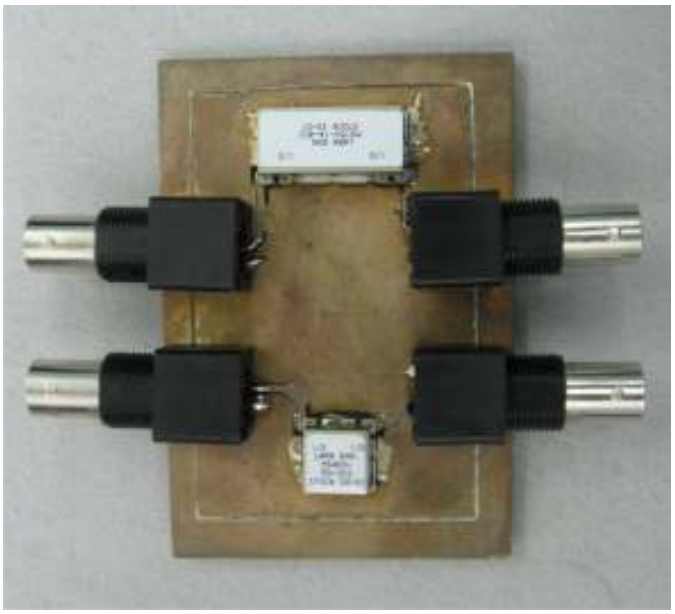
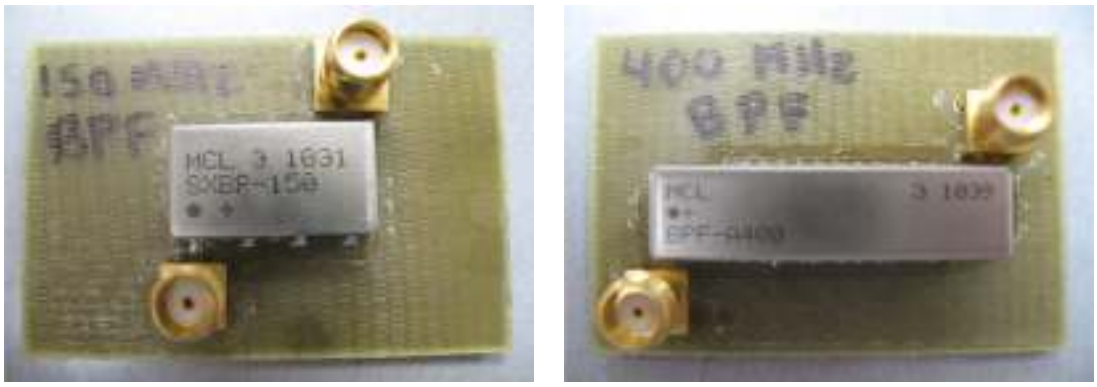


Figure 4.6: Lark Engineering MS150 (top) and MS400 (bottom) Filters.

Sampling Theorem [4], produces an infinite series of images of the baseband signal. Digitally, the sampled spectrum is limited to one-half the sampling frequency, so all spectral components of the sampled signal are aliased into this sampled spectrum. In order to avoid overlapping images from RF energy outside the frequency band of interest, the signal is band-pass filtered, such that the pass-band of the filter does not overlap any multiples of half the sampling frequency (32 MHz for this system). For this reason, these filters are also known as anti-aliasing filters.

The band-pass filters recommended for the GRBR by [12] are the Lark Engineering MS150 and MS400, which are designed to be high performance filter modules. For this reason, they were evaluated as candidates for the anti-aliasing filters used on the PGRBR. Figure 4.6 shows a prototype circuit board with both the MS150 and MS400 filters in surface-mount packages.

Mini-Circuits offers a variety of plug-and-play RF circuit modules that aim to provide good performance as well as reasonable cost. The Mini-Circuits SXBP-150+ and BPF-



(a) (b)

Figure 4.7: Prototype Boards with the Mini-Circuits (a) SXBP-150+ and (b) BPF-A400+ Band-Pass Filters.

A400+ band-pass filters were considered for use as anti-aliasing filters on the PGRBR based on their expected performance characteristics and affordability. Figure 4.7 shows initial prototype boards utilizing the Mini-Circuits SXBP-150+ and BPF-A400+ band-pass filters.

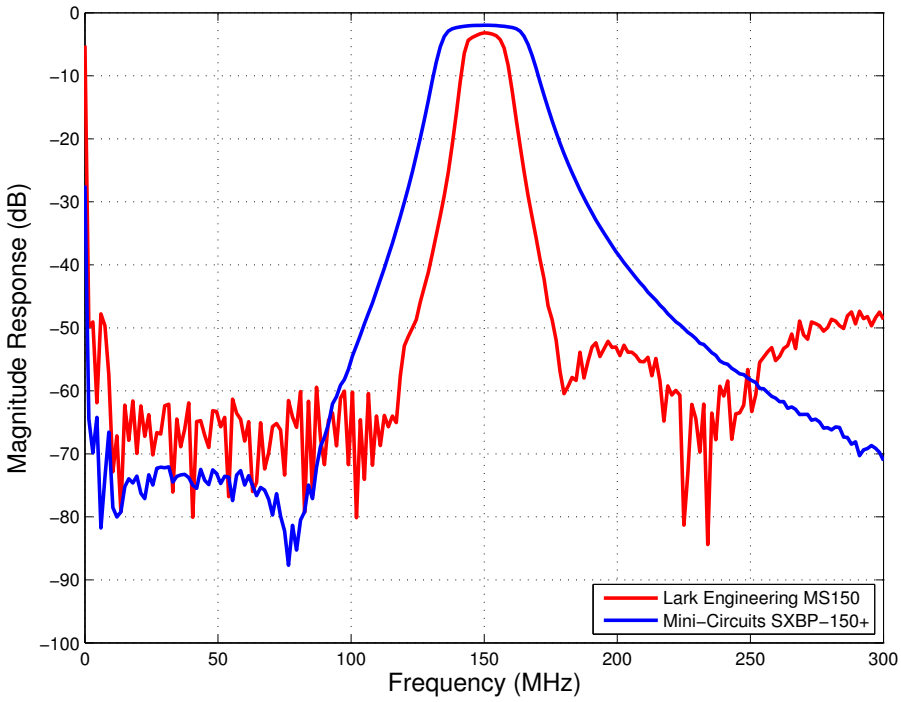
In determining the best anti-aliasing band-pass filters for the PGRBR, the Lark Engineering and Mini-Circuits filters were characterized on prototype circuit boards. The PCB footprint patterns recommended by Lark Engineering and Mini-Circuits were used in order to obtain the most accurate results of filter performance.

4.2.1 150-MHz Channel

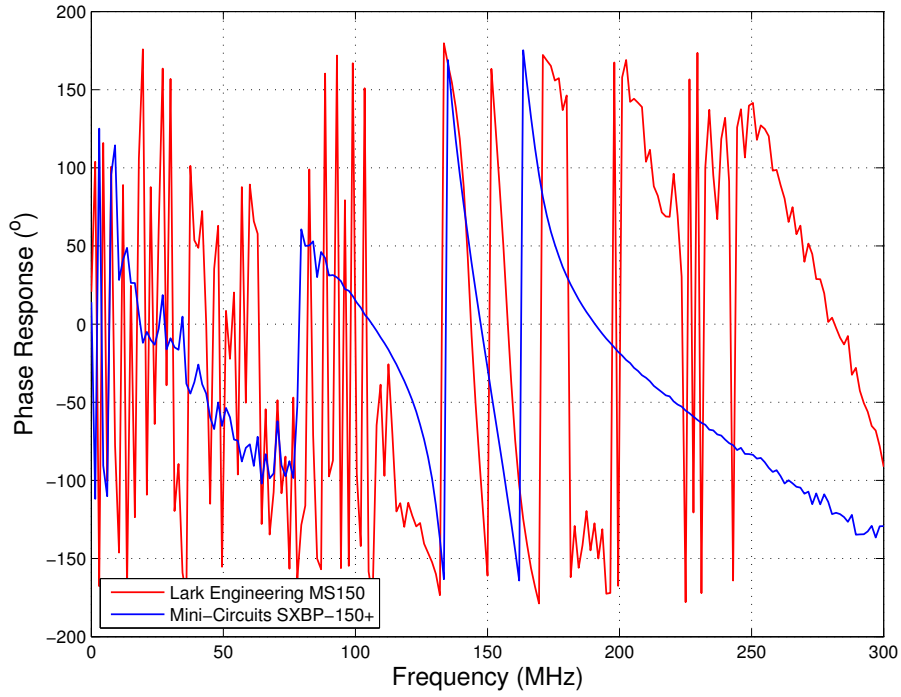
In order to characterize the responses of these filters for comparison, the S-parameters were measured. The magnitude and phase responses of the Lark Engineering MS150 and Mini-Circuits SXBP-150+ band-pass filters are plotted in Appendix A. Table 4.3 highlights the important filter characteristics that were used in the selection process. Additionally, the S_{21} magnitude and phase plots are overlaid in Figure 4.8 for direct comparison.

As the results indicate, the Lark Engineering MS150 shows a more narrowband response

[3] At 150 MHz.



(a) Magnitude Responses



(b) Phase Response

Figure 4.8: S21 (a) Magnitude and (b) Phase Responses of the 150-MHz Band-Pass Filters.

Table 4.3: 150-MHz Band-Pass Filters Results Summary

Filter	MS150	SXBP-150+
Center Frequency (MHz)	150	150
Bandwidth (MHz)	14	32
Insertion Loss (dB)[3]	3	2
Noise Floor (dB)	−48	−65
Input Reflection (dB)[3]	−21	−23
Stopband Reflection (dB)	−0.8	−0.8
Forward Phase Shift (^{o})[3]	−180	25
Cost (USD)	105.00	15.95
Package Size (mm)	26 × 13 × 8	19 × 11 × 7

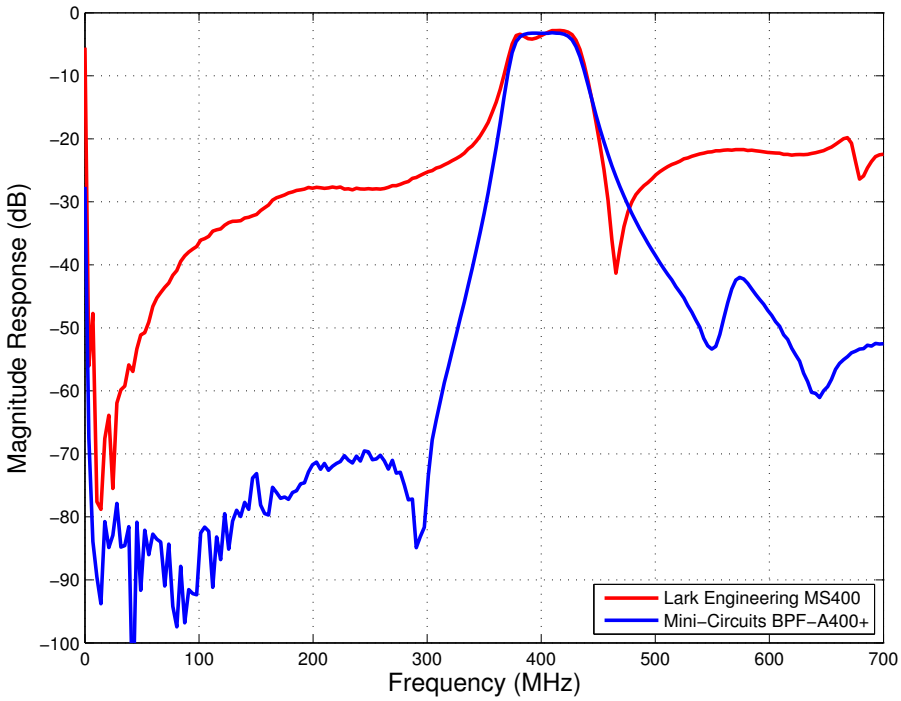
(14-MHz bandwidth) than the Mini-Circuits SXBP-150+ (32-MHz), which is advantageous for the anti-aliasing application. Both filters were centered at 150 MHz, and the MS150 showed a 1 dB greater insertion loss. Both filters showed similar input reflection responses (S_{11}), both at 150 MHz and out-of-band. A considerably lower noise floor was obtained from the SXBP-150+ filter (about 17 dB lower), indicating a better rejection of out-of-band energy. The SXBP-150+ is also slightly smaller in physical size than the MS150. The forward phase shift of each device is important, but, as previously mentioned, it is the net differential phase between the two receive paths is that is important to be minimized.

4.2.2 400-MHz Channel

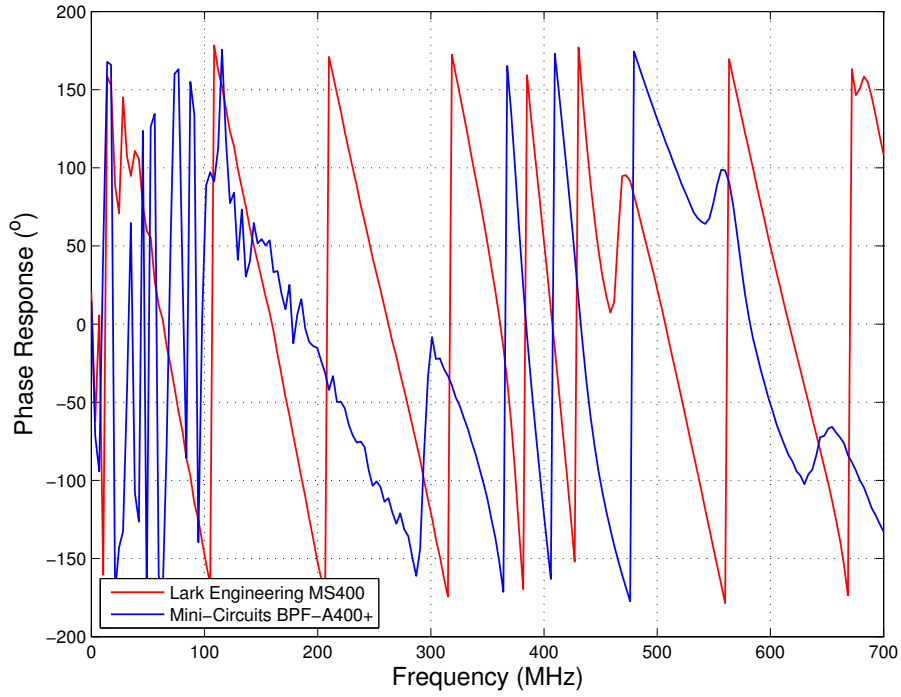
Similarly to the 150-MHz band-pass filters, the S-parameters of the MS400 and BPF-A400+ filters were measured. The magnitude and phase plots of these measurements are plotted in Appendix A. A summary of the criteria used for comparison is listed in Table 4.4. The S_{21} magnitude and phase plots of each both filters are overlaid in Figure 4.9.

The presented results suggest similar performance within the passband region for the Lark Engineering MS400 and the Mini-Circuits BPF-A400+. Both are centered close to the nominal 400 MHz, have relatively wide bandwidths (around 60 MHz), and similar insertion

[4] At 400 MHz.



(a) Magnitude Responses



(b) Phase Response

Figure 4.9: S21 (a) Magnitude and (b) Phase Responses of the 400-MHz Band-Pass Filters.

Table 4.4: 400-MHz Band-Pass Filters Results Summary

Filter	MS400	BPF-A400+
Center Frequency (MHz)	402	403
Bandwidth (MHz)	61	59
Insertion Loss (dB)[4]	3.5	3
Noise Floor (dB)	−65	−70
Input Reflection (dB)[4]	−8	−15
Stopband Reflection (dB)	−1.5	−1
Forward Phase Shift (^{o})[4]	50	−145
Cost (USD)	92.00	29.95
Package Size (mm)	13 × 13 × 8	34.5 × 9 × 8.5

losses. The BPF-A400+ has a slightly lower input reflection response at 400 MHz. The S_{21} response of the BPF-A400+, however, shows a much better rejection of out-of-band energy, as much as 40 dB. Where the BPF-A400+ continues to roll off from the passband, the MS400 shows flat stopband regions of −28 dB on the lower side of the passband and −22 dB on the upper side. Again, the forward phase shift is not critical, and the receive chain phase can be tuned via the preamplifier.

4.3 Wideband Amplifier

As briefly discussed at the beginning of this chapter, the 150-MHz RF front-end includes an additional wideband amplifier because the BasicRX daughterboard does not include an amplifier, whereas the RFX-400 daughterboard does include additional amplification. Wideband amplifiers exhibit an extremely flat forward gain response spanning a large frequency range. This allows them to be used as amplifiers for broadband RF signals or even as general-purpose amplifiers for many applications. In the GRBR, the Mini-Circuits ZFL-500LN+, pictured in Figure 4.10, is used as a general-purpose gain block for the 150-MHz RF front-end.

In order to minimize design and testing time, the design for the PGRBR's wideband

Figure 4.10: Mini-Circuits ZFL-500LN+ Wideband Amplifier.

amplifier was borrowed from the input amplifier design on the RFX-400. A prototype of this amplifier is shown in Figure 4.11. The amplifier uses a monolithic microwave integrated circuit (MMIC) that only needs an external bias resistor and input impedance matching.

In order to compare the response of the RFX-400 wideband amplifier prototype to the Mini-Circuits ZFL-500LN+, the S-parameter magnitude and phase responses were measured. The ZFL-500LN+ and RFX-400 wideband amplifier prototype responses are plotted in Appendix A. For direct comparison, the S_{21} magnitude and phase responses were plotted in Figure 4.12.

As indicated by the results, there is a distinct gain discrepancy between the two amplifiers. Over the measured bandwidth, the ZFL-500LN+ amplifier's forward gain is around 24.5 dB.

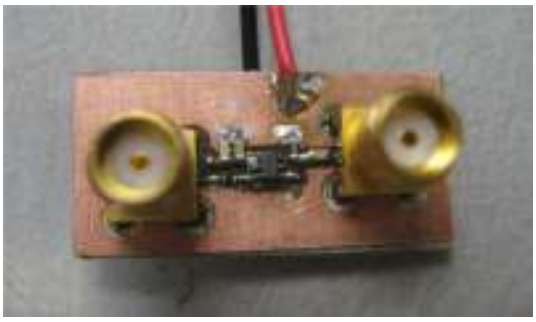
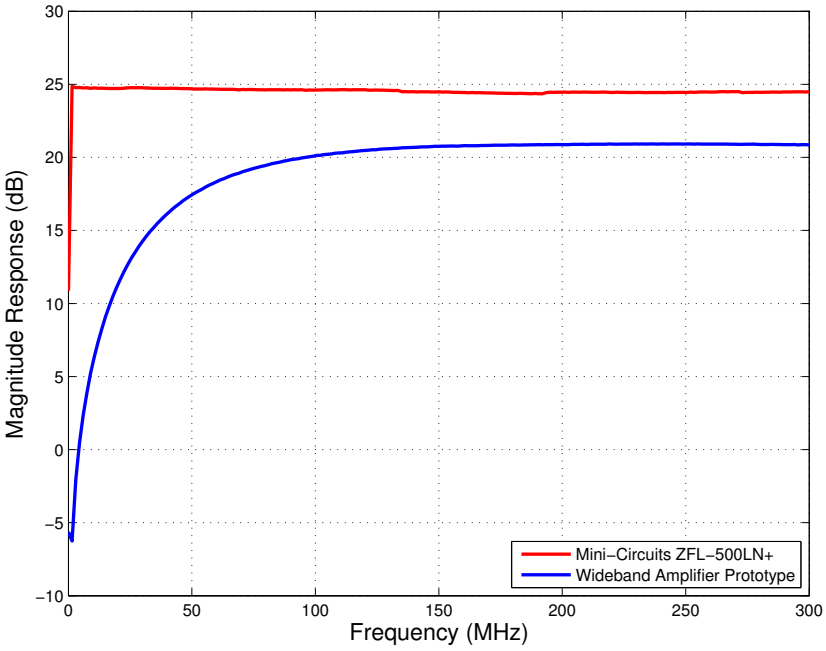
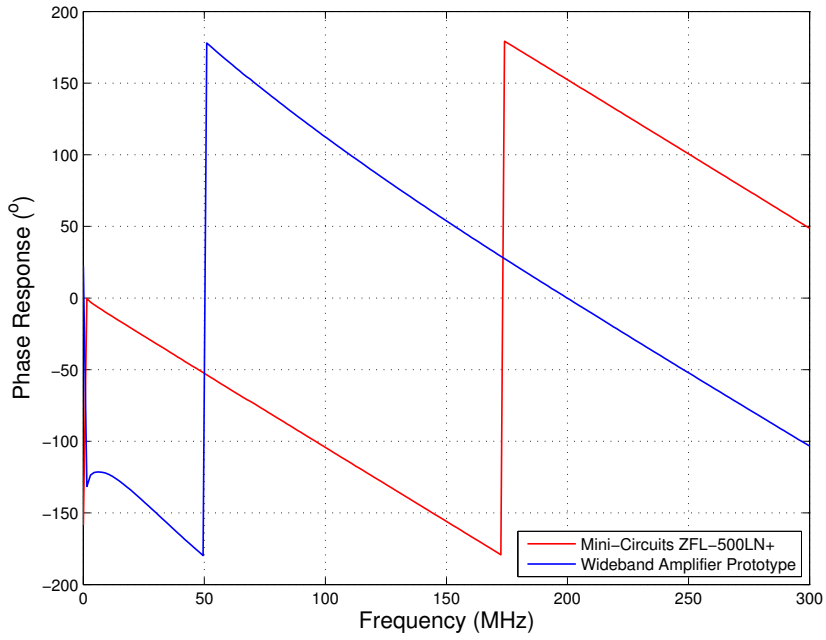


Figure 4.11: Prototype of the Wideband Amplifier Used on the RFX-400 Daughterboard.



(a) Magnitude Responses



(b) Phase Responses

Figure 4.12: S21 (a) Magnitude and (b) Phase Responses of the Wideband Amplifiers.

The prototype amplifier's forward gain increases following an exponential until about 125 MHz, at which point it flattens out at 21 dB. At the frequency of interest, 150 MHz, there is a 3.5-dB gain difference between the two amplifiers. There is also a phase difference between the two amplifiers at 150 MHz, but as discussed in Sections 4.1 and 4.2 the absolute forward phase shift is not critical.

4.4 Conclusions

In order to fit on the PGRBR PCB, reducing the size of the GRBR's RF front-end circuitry was necessary. Several amplifier and filter prototypes were developed in order to characterize the functionality of the reduced circuitry. Mixed success was obtained with the prototypes of the RF front-end.

4.4.1 Preamplifiers

Overall, both prototype preamplifiers were successful in matching the responses of the LNK-146 and LNK-450 preamplifiers. The size of the original circuitry was significantly reduced for the prototypes, and the supply voltages were reduced from 12 V to 5 V. Tuning of the preamplifiers will likely be necessary on the PGRBR to cancel out the overall phase difference between the two channels. The prototype designs were copied into the PGRBR design, with minimal layout changes as an attempt to maintain similar performance characteristics.

4.4.2 Band-Pass Filters

Although the Lark Engineering MS150 illustrated a narrower passband, the Mini-Circuits SXBP-150+ was selected for use on the PGRBR PCB for several reasons. First, its response exhibited a lower noise floor, allowing better rejection of out-of-band signals and, ultimately, more meaningful and accurate TEC estimations. The lower input reflection and insertion

loss at 150 MHz, though small, may be critical considering how weak the receive signals may be. Additionally, the filter has a smaller package size, reducing the PCB space necessary for it. Finally, the SXBP-150+ is substantially cheaper and more readily available for purchase. The passband of this filter does cross the a multiple of one-half the sampling rate (32 MHz); however, it can be argued that the selectivity of the preamplifier and of the antenna is significant and little out-of-band RF energy will be digitized.

For the 400-MHz channel, the Mini-Circuits BPF-A400+ was selected for similar reasons: lower noise floor, slightly lower insertion loss, lower cost, and more readily available. The driving factor, however, was the difference in out-of-band rejection. A 40-dB difference would make the difference between a strong signal for TEC estimation and one that is unusable because it is not discernible from the stray images aliased from the stopband. The significantly larger package size of the BPF-A400+ is still reasonable for the PC/104 form factor of the PCB. The passbands of both of these filters cross multiples of one-half the sampling frequency on both sides of the center frequency (384 MHz and 416 MHz), so it is likely that some out-of-band RF energy between 352 MHz to 384 MHz and 416 MHz to 448 MHz will be aliased into the baseband. The selectivity of both the antenna and the preamplifier will assist in reducing the magnitude of these images.

Neither of the selected band-pass filters provide effective anti-aliasing properties to the PGRBR. In future revisions, additional, more narrowband band-pass filters need to be considered, as the antenna topologies feasible for the CubeSat form factor are limited and may not provide the additional selectivity of the QFH antennas. Time constraints limited the scope of research and testing different filter topologies for this revision.

4.4.3 Wideband Amplifier

The RFX-400 wideband amplifier does not provide enough gain to meet the specifications of the recommended wideband amplifier for the GRBR. During the PCB design, however, this

issue was overlooked. This will definitely reduce the effectiveness of the TEC estimation. It is unclear how much system performance will be affected, but it still may be possible to make preliminary measurements. Future revisions will need to address this issue with a complete redesign of this broadband amplifier.

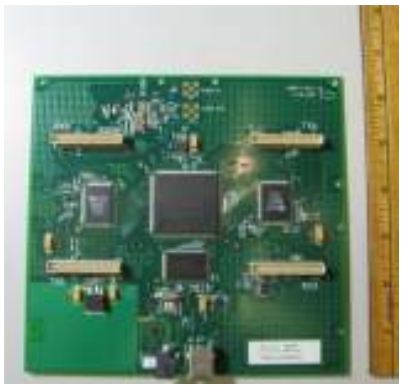
Chapter 5

Printed Circuit Board Layout

This chapter will discuss the hardware integration of the GRBR system onto the single PGRBR PCB, as well as the PCB design philosophy and choices. As discussed in Section 2.2, the GRBR was constructed from a number of discrete components that include: antennas, RF front-ends (i.e., amplifiers and filters), USRP mother- and daughterboards, and a GPC running GNU Radio. The need to compress the GRBR receive-chain onto a single PC/104 form factor PCB was dictated by Requirements 1 and 4. Removal of unnecessary circuitry (e.g., the transmission functionality of the USRP) was an implication of Requirement 3. In the process of developing the PGRBR PCB, the electrical schematic designs from the USRP and its daughterboards were combined with the filters and amplifier designs discussed in Chapter 4.

5.1 Circuitry Integration

Because the USRP is a flexible SDR hardware platform that is adaptable for many different applications, there is on-board functionality that is not necessary for the GRBR system. By removing this additional functionality, using smaller components where possible, and removing the unnecessary headers between the mother- and daughterboards, the size of the



(a) The USRP Motherboard.

(c) The GRBR RF Front-End Hardware.

(b) The USRP Daughterboards.

(d) The PGRBR PCB (unpopulated).

Figure 5.1: Size Comparison of the GRBR (a) Digital and (b)-(c) RF Hardware to (d) the PGRBR PCB .

system was significantly reduced. Figure 5.1 shows the GRBR components in (a) – (c) and the PGRBR PCB in (d) to demonstrate the physical size reduction of the GRBR by the PGRBR.

5.1.1 RF Front-Ends

Because circuit performance is affected by layout at RF, the amplifier and filter layouts used for prototyping were copied onto PGRBR PCB with minimal changes in order to obtain similar results to those obtained during prototyping. SubMiniature version A (SMA) connectors between each stage of the RF front-ends were retained in order to compare individual

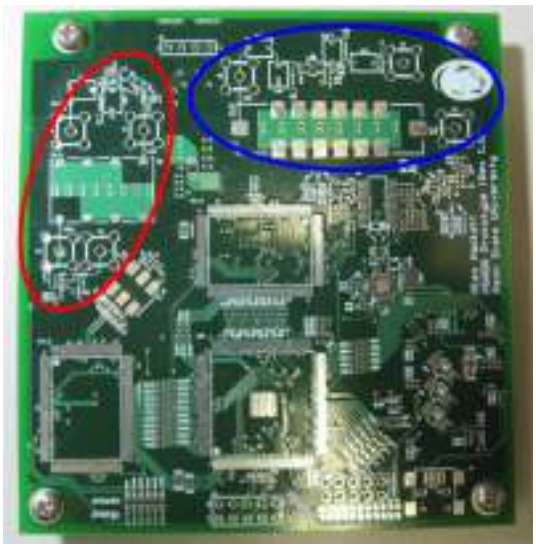


Figure 5.2: Reduction of the 150-MHz (red) and 400-MHz (blue) Channel RF Front-Ends.

stage performance to the prototypes, as well as to tune the preamplifiers. In Figure 5.2, the sections circled in red and blue are the 150-MHz and the 400-MHz channel RF front-ends, respectively.

5.1.2 BasicRX

The BasicRX daughterboard is a basic unit for the USRP with two signal inputs (in-phase and quadrature), an isolation transformer for each, biasing circuitry, a small electrically erasable programmable read-only memory (EEPROM) for identification, and breakout header pins for attaching or monitoring various signals on the USRP.

On the GRBR, only one signal input and isolation transformer/biasing circuitry are necessary to receive the 150-MHz beacon signal. The EEPROM is also necessary to notify the GPC which daughterboard is attached. The required circuitry on the BasicRX daughterboard is circled in red in Figure 5.3. From the figure, it is clear that on this daughterboard (6.99 cm $\times$ 6.35 cm), the size reduction was mostly due to removal of the breakout headers and motherboard connector. The minimized BasicRX circuitry on the PGRBR PCB is

(a) Top (b) Bottom

Figure 5.3: Necessary Circuitry on the BasicRX Daughterboard.

shown in Figure 5.4. On this PCB, a direct connection was made between the RF transformer and the USRP's mixed-signal front-end chip, eliminating the need for the 64-pin header pair on the USRP and BasicRX daughterboard.

5.1.3 RFX-400

Unlike the BasicRX daughterboard, the RFX-400 daughterboard is slightly more complicated than just an RF transformer, as it is able to both transmit and receive between 400 and

Figure 5.4: Reduction of the BasicRX Circuitry on the PGRBR PCB.

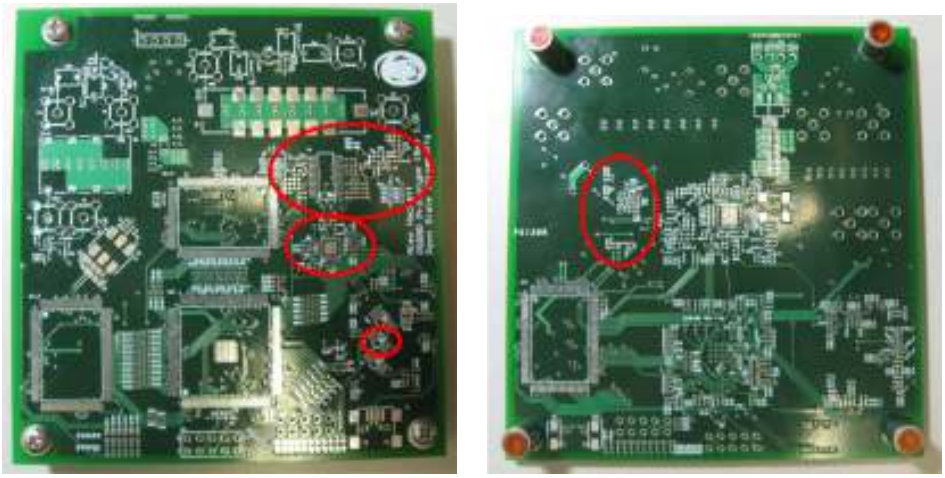
(a) Top (b) Bottom

Figure 5.5: Necessary Circuitry on the RFX-400 Daughterboard.

500 MHz, which is well beyond the capability of the mixed-signal front-end devices alone. In order to perform these operations, a variety of filters, local oscillators, a quadrature demodulator, mixers, amplifiers, and other support circuitry is needed. Only about half of the circuitry on the RFX-400 daughterboard is utilized for the GRBR, as most of the circuitry was removed. The final design for this reduced daughterboard included an input filter and amplifier, quadrature demodulator, a pair of output filters and amplifiers, an oscillator, and additional supporting circuitry (see Appendix B for the full schematic design). The circuitry circled in red in Figure 5.5 is the necessary hardware that was designed onto the PGRBR PCB. The reduction of this hardware is shown in Figure 5.6, with the circled areas highlighting the RFX-400 components. Because it includes more functionality than the BasicRX daughterboard, the RFX-400 daughterboard (14.29 cm $\times$ 6.35 cm) there were two 64-pin headers (one for receiving and one for either transmitting or receiving) that were also unnecessary for the PGRBR, as all the components were integrated onto a single PCB.

5.1.4 USRP Motherboard

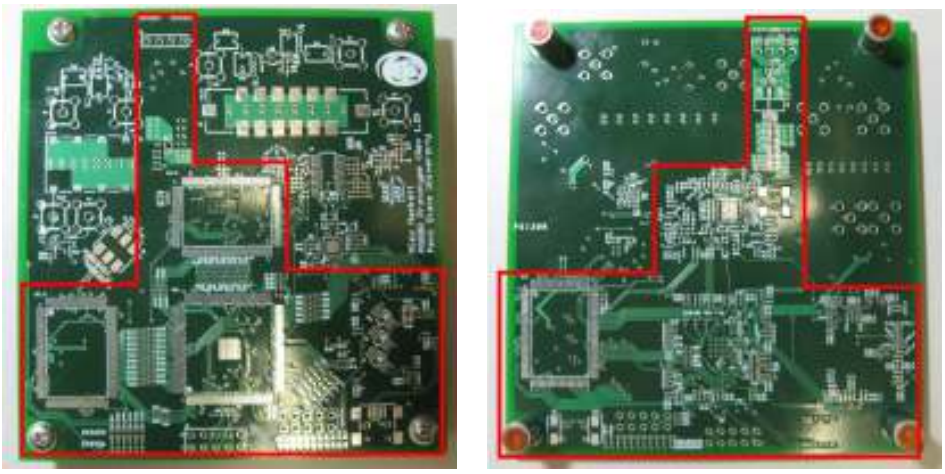
Unlike the daughterboards, minimization of the USRP motherboard was mainly limited to the removal of the daughterboard connection headers and reduction of routing to the mixed-signal front-end devices. Nearly all of the remaining circuitry was retained, including the FPGA, mixed-signal front-ends, the clock source, the USB microcontroller, the EEPROM,



(a) Top (b) Bottom

Figure 5.6: Reduction of the RFX-400 Circuitry on the PGRBR PCB.

and the other supporting circuitry. Smaller package passive components (i.e., resistors, capacitors, and inductors), devices (i.e., EEPROM and linear regulators), and external connectors (i.e., USB and power) were utilized where possible. The reduced USRP circuitry on the PGRBR PCB is outlined in red in Figure 5.7. As illustrated, the majority of the circuitry on the PGRBR PCB is dedicated to the USRP functionality.



(a) Top (b) Bottom

Figure 5.7: Reduction of the USRP Circuitry on the PGRBR PCB.

5.2 Component Placement and Routing

While there are numerous placement configurations for the PGRBR circuitry, the number of *effective* configurations is limited to only a handful. Careful component placement consideration has several benefits in terms of system operation, as well as overall professionalism.

By organizing functionally related components near each other, a modular layout is achieved. This allows shorter PCB traces to be used to interconnect the components. In low frequency designs, that is, below Ultra High Frequency (UHF), long, thin PCB traces are generally avoided, as both inductance and resistance are proportional to trace length. Unless this effect is desired for transmission lines, as is the case in many microwave RF circuits, these effects are classified as losses and are detrimental to system performance. The use of shorter and wider PCB traces alleviates these effects and allows more ideal interconnects between components and, ultimately, more ideal circuit operation.

More effective routing between functionally different circuitry is also fostered by the modular layout approach. By aligning subcircuit inputs/outputs towards their origin/destination, more direct (and consequently, more ideal) signal paths can be chosen between components. The physical board area necessary for a particular design can be significantly reduced if the interconnect routing between sub-circuits is simplified.

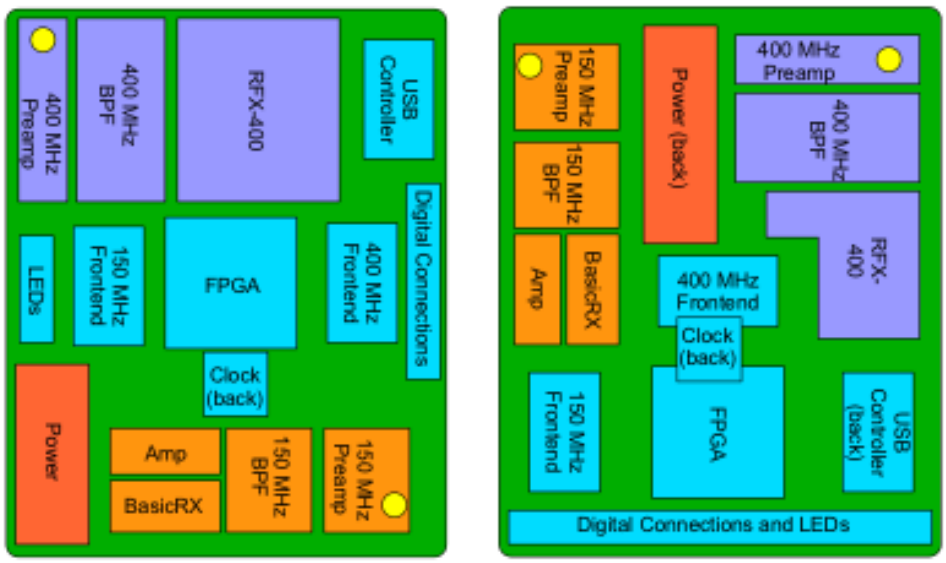
Another placement and routing advantage is added by the extreme flexibility of FPGA devices. Because the majority of pin connections on FPGAs are general-purpose I/O pins, the pin connections easily can be reorganized in the FPGA design software in order to best suit the layout needs. This technique is known as "pin swapping" and facilitates shorter and more effective PCB trace routing between the FPGA and other circuitry [15].

Digital circuitry operates by switching transistors on and off. During this switching period, short bursts of high frequency current are drawn from the power supplies and, by Kirchhoff's Voltage Law, returned on the ground path. Digital circuitry is relatively tolerant

to the slight variations in supply and ground voltages caused by these spikes. Precision operation of analog/RF circuitry, however, requires stable power supply and ground voltages. For this reason, it is common practice to isolate digital and analog/RF circuitry by their associated power and ground supplies. Because they both must ultimately be connected to the board power and ground supplies, the digital and analog/RF power and ground supplies are respectively connected through low-pass filters or ferrite beads. This filtering suppresses current spikes on the power and ground supplies from the digital circuitry so that the analog/RF circuitry can operate with minimal local interference.

All of these PCB design techniques were used in the layout of the PGRBR PCB. Modularization was implied by the organization of the schematic design, so grouping related components followed naturally. The components of each subcircuit were placed such that the shortest and most effective routing between them was possible. Each subcircuit as a whole was placed such that the shortest connections could be made with other sub-circuits, taking advantage of FPGA pin swapping (for the digital circuitry) and complying with isolation between the digital and analog/RF circuitry.

Two possible layout organizations were developed as a result of considering these design techniques. These are illustrated in Figure 5.8. As illustrated in PCB layout option A, the 400-MHz and 150-MHz RF signals are supplied in the top left and bottom right corners of the board, respectively. These signals are conditioned as they travel in a clockwise direction around the PCB, spiraling towards the FPGA at the center. Finally, the digitized signals are passed to the USB microcontroller and connector at the top right corner of the board. Power is supplied at the bottom left corner. This design uses modularization and isolation between digital and analog/RF circuitry; however, it has the disadvantage of requiring that the 400-MHz channel power and ground supplies be routed farther across the PCB than those of the 150-MHz channel. This introduces a larger path on which local and external noise could couple and disrupt the operation of the 400-MHz channel circuitry.



(a) (b)

Figure 5.8: PCB Layout Options (a) A and (b) B.

PCB layout option B alleviates this problem by co-locating the RF receive channels on the top of the PCB, split down the center by the power supply. In this configuration, the power and ground supplies to the sensitive RF circuitry are kept as short as possible to reduce noise coupling. Longer power and ground supplies are needed to reach the digital circuitry at the bottom of the PCB; however, digital circuitry is intrinsically more immune to noise[1]than the analog counterpart, making this a reasonable trade-off. Like option A, a modular layout is also utilized in option B, with the 150-MHz and 400-MHz RF signals flowing in parallel from top to bottom, converging at the FPGA (bottom center) after being digitized. Finally, the processed signal is sent to the GPC via the USB microcontroller and connector at the bottom right corner of the board.

Due to the advantages discussed above, layout option B was used to design the PGRBR PCB. Pin swapping of the FPGA I/O connections allowed shorter and more effective routing throughout the complex digital network.

[1]There are cases in which analog designs outperform digital designs in the presence of noise; however, in this context, it is a reasonable assumption to ignore these special cases.

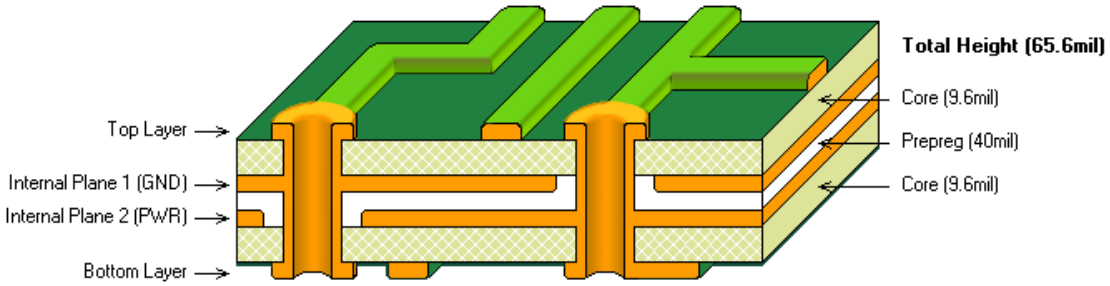


Figure 5.9: The PCB Layer Stack Used on the PGRBR PCB.

5.3 Power and Ground Planes

In the design of PCBs with more than two copper layers, some of the inner layers are often used as power and/or ground planes that span a portion or the entire PCB. This design technique is advantageous for systems like the PGRBR. Because resistance is inversely proportional to the physical dimensions of a conductor, larger PCB traces provide a lower impedance paths for forward (power) or return (ground) currents. Taken to the extreme, a trace that spans an entire PCB layer (or plane), provides the lowest impedance path possible. This aids in mitigating voltage drops across the forward or return current paths that increase proportionally with current. When used with proper power supply bypassing (i.e., medium-valued low-loss shunt capacitors that present a low impedance at medium to high frequency), power and ground planes can be very effective in providing near ideal voltage sources (constant voltage, no output resistance). Figure 5.9 shows the PCB layer stack of the PGRBR PCB[2]. Out of the four copper layers, two were dedicated to power and ground distribution.

The use of power and ground planes is useful in digital, low-frequency analog, and RF designs, although, as discussed in Section 5.2, the power and ground supplies for each of these types of circuits should be isolated to avoid unwanted coupling between the different types. This can be achieved through the use of split power and ground planes. An example

[2]Images generated using Altium Designer 9 [16].

of the split ground planes on the PGRBR is illustrated in Figure 5.10[2]. The area circled in red is where the two grounds were connected through a ferrite bead on the top copper layer. With reference to Figure 5.8(b), the analog/RF circuitry was placed above the RF ground split plane and the digital circuitry was placed above (and below) the digital ground split plane. The mixed-signal front-end devices were placed above both the RF and digital ground split planes, due to their analog *and* digital nature.

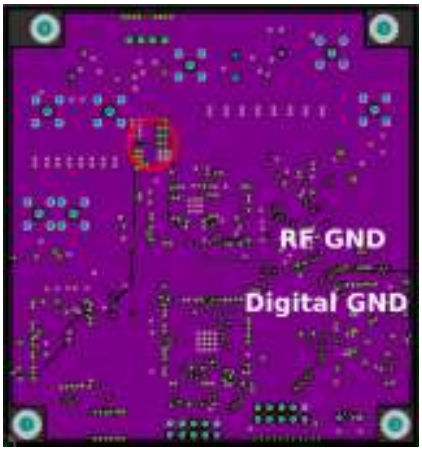


Figure 5.10: Split RF and Digital Grounds on the PGRBR PCB.

5.4 Conclusions

This chapter has discussed many of the circuit-level reductions made from the PGRBR system to the PGRBR PCB, in terms of both functionality and physical board area. Several of the PCB design techniques that aim for a compact, effective, and reliable layout that were used in the PGRBR PCB design have also been presented. Illustrations of the design reductions and layout techniques have served as examples of the topics discussed in this chapter. Future revisions of the PCB will benefit from further circuit-level and physical dimension reduction as well as more advanced PCB design techniques for RF and digital layout design.

Chapter 6

Conclusions

An extensive design of the PGRBR has been developed and detailed in this document. This chapter serves to both summarize the work presented and provide several directions to be pursued by future revisions.

6.1 Summary

The purpose of the PGRBR project was to develop an *in situ* TEC sensing instrument from a previously developed remote sensing system. The project used an open-source software radio platform (the USRP and the GNU Radio software package), along with several RF components needed to properly digitize the received signals. In order to reduce the physical size of the system, three major areas were considered: the FPGA, discussed in Chapter 3; the RF front-end design, discussed in Chapter 4; and the removal of unneeded circuitry and integration onto a single PCB, discussed in Chapter 5.

Table 1.1 presents several design requirements for this revision of the PGRBR, all of which were met through the design of the PCB. Requirement 1 constrained the PCB form factor to the PC/104 standard. The PCB developed adheres to this form factor, and it includes all the necessary circuitry, with unused PCB space. Requirement 2 constrained the power

supply of the PGRBR to a single 5-V power bus. Redesign of some elements and the use of voltage regulators allowed the system to function on the required power bus. Requirement 3 specified that the GRBR was to be reduced in size by the removal of unnecessary circuitry and logic functionality. None of the USRP's transmit functionality (hardware and logic design) was included in the design of the PGRBR, helping to ensure a more compact and optimized system. Requirement 4 specified interchangeability with the receive chain of the GRBR system (excluding antennas). By developing directly from the design of the GRBR and the USRP, design compatibility was achieved. Finally, Requirement 5 ensured that the PCB construction, verification, and testing were feasible with the currently accessible resources. By selecting hand-solderable components, all solder joints were visibly verifiable for electrical contact and physical strength.

6.2 Goals for the Next Revision

Several aspects of producing a minimized GRBR system were neglected in this first revision of the PGRBR, in order to provide a working proof-of-concept system within the allotted time frame. Several iterations of the PGRBR design will be developed, building upon this alpha revision of the PGRBR system. Specifically, the next revision of the PGRBR will address additional RF considerations, lower-power design, deviating from the USRP-based design, and the integration process with a specific CubeSat mission.

6.2.1 RF Front-End Redesign

Properly functioning RF front-end circuitry is a critical aspect for the PGRBR to obtain accurate and meaningful data. As discussed in Chapter 4, several of the components in the RF front-end did not meet the specifications of those devices used in the GRBR or failed to operate as they were intended. The next revision of the PGRBR should be designed with

a fully analyzed and verified RF front-end. A full link budget should be developed in order to set requirements on the necessary gains, insertion losses, reflections, noise figures, etc. of the RF components.

6.2.2 Noise Analysis

One important aspect of RF and communication systems is a consideration of noise factors through the transmit and receive chains. The cumulative effects of noise factors throughout the system could render the data measurements useless if the overall signal-to-noise ratio (SNR) is too high. Although noise factor measurements were not made on the prototype filters and amplifiers presented in Chapter 4 due to lack of access to proper noise analysis instrumentation, they will be necessary in system validation, calibration, and development of an accurate link budget.

6.2.3 Reduce Power

Due to the size constraints of CubeSats, on-board power generation and storage are very limited, on the order of several watts. In its current operational state, the PGRBR draws about 3.5 W continuous, which is more than the entire power budget allocation on some CubeSats, such as the Orbital System for Investigating the Response of the Ionosphere to Stimulation and Space Weather (OSIRIS) [17] and SwissCube [18] missions.

Power Regulation

Linear voltage regulators were used on the PGRBR to step down the input voltage from 5 V to the required 3.3 V, 2.5 V, and 1.8 V. For a ground-based application, this is an acceptable power regulation strategy because there are no significant restrictions on power usage and convection cooling is a feasible method of cooling devices. On a CubeSat, however,

available power is very limited, and the methods of cooling are limited to heat conduction and thermal radiation. Linear voltage regulators, in an application like this, both waste a significant amount of power and introduce thermal issues, as they operate by dissipating the excess power caused by the larger input voltage. The power dissipated in a linear voltage regulator is proportional to the amount of current pulled through the device (hence, *linear* regulator).

On a CubeSat, there will likely be a power regulation subsystem that supplies various power buses to the entire system. It will likely supply several, if not all, of the necessary power bus voltages, eliminating the need for inefficient and thermally problematic linear regulators. If there is no centralized power regulation subsystem to supply the needed power buses, the use of local switching regulators (also known as DC/DC converters) would significantly reduce the excess power dissipation and heat generation. Proper electromagnetic interference (EMI) shielding for the converters will be necessary to avoid electromagnetic coupling between the switching converters and the RF circuitry.

Low-Power Devices

Additionally, the use of lower-power devices (where appropriate) will be considered to further reduce the PGRBR's power consumption. The digital circuitry, namely the mixed-signal front-end devices, the FPGA, and the USB microcontroller, consume a significant percentage of the total power consumption. The mixed-signal front-end devices contain both ADC and DAC functionality (in addition to other signal processing elements); however, for the PGRBR, the devices are only used as high-speed ADCs, with the additional functionality idly wasting power. FPGA vendors offer a wide range of low-power FPGAs, and a further trade-study of the available FPGAs will be performed to optimize for the low power needs of the next revision. The USB microcontroller on the PGRBR was retained for interchangeability with GRBR, and will likely be unnecessary in future revisions, depending on the interface

used between the PGRBR and the CubeSat's CDH subsystem, further reducing the PGRBR power draw.

6.2.4 Mixed-Signal Front-End ADCs

As mentioned in the previous section, the mixed-signal front-end devices are used only for their high-speed ADC functionality. The DAC, digital quadrature mixer, and secondary clock functionalities of these devices are all unused in the PGRBR. Selection of dedicated high-speed ADCs will not only reduce power, but it may also reduce component footprint size, allowing the system to be further condensed. With constant advances in ADC technology, it may be possible to sample and digitize both 150-MHz and 400-MHz channels directly (or at least using digital down-conversion techniques), avoiding the need for the RFX-400 down-conversion circuitry.

6.2.5 CubeSat Integration

Because this revision of the PGRBR was not intended for integration with a CubeSat, several design requirement liberties were taken (within reason), including form factor, power, and data interface (physical and electrical). Each CubeSat mission will dictate specific requirements on these parameters, and the design will need to be adjusted accordingly for successful integration. Currently, there are plans to integrate the PGRBR instrument with a CubeSat bus produced by Dr. Hien Vo at Universidad Interamericana de Puerto Rico, Bayamón. Other opportunities to fly the PGRBR will likely appear, due their inexpensive development and launch costs.

References

[1] J. K. Hargreaves. *The Solar-Terrestrial Environment*. New York, NY: Cambridge University Press, 1992, pp. 44–97.

[2] R. F. Pfaff. *In-Situ Measurement Techniques for Ionospheric Research*. Greenbelt, MD: National Aeronautics and Space Administration: Goddard Space Flight Center, 1996, pp. 1–3.

[3] "CubeSat Kit." Internet: `http://www.cubesatkit.com/`, [11 April 2011].

[4] C. R. Johnson and W. A. Sethares. *Telecommunication Breakdown*. Upper Saddle River, NJ: Prentice Hall, 2003, pp. 11–12, 111.

[5] G. Youngblood. "A Software-Defined Radio for the Masses, Part 1." *QEX, ARRL*, p. 1, July/Aug 2002.

[6] S. Bilén. EE497E (Introduction to SDR) Lecture, Topic: "SDR: The Future of Radio." Pennsylvania State University, PA, 26 Aug 2009.

[7] M. Sunderland. "Software-Defined Radio Interoperability with Frequency Hopping Waveforms." M.S. thesis, Pennsylvania State University, PA , 2010.

[8] "Ettus Research LLC." Internet: `http://www.ettus.com/`, 5 April 2011 [12 April 2011].

[9] "GNU Radio." Internet: `http://gnuradio.org/redmine/wiki/gnuradio`, 24 Feb. 2011 [12 April 2011].

[10] M. Yamamoto, "Digital beacon receiver for ionospheric TEC measurement developed with GNU Radio," *Earth Planets Space*, vol. 60, pp. e21–e24, Nov. 2008.

[11] M. H. Jusoh, *et al.* "Determination of Ionospheric Total Electron Content (TEC): Phase Measurement Based on Leveling Technique." *Third UKSim European Symposium on Computer Modeling and Simulation*, 2009, pp. 208–213.

[12] M. Yamamoto, "GNU Radio Beacon Receiver," Website: `http://www.rish.kyoto-u.ac.jp/digitalbeacon/`

[13] "CubeSat in the News." Internet: `http://www.cubesat.org`, 6 April 2011 [13 April 2011].

[14] "The Cyclone II Power Advantage – 1/2 the Power of Competing 90-nm Low-Cost FPGAs." Internet: `http://www.altera.com/products/devices/cyclone2/features/power/cy2-power.html`, [5 April 2011].

[15] M. Hauff. "FPGA/PCB Pin Synchronization." Internet: `http://www.altium.com/files/pdfs/PinSwappingWhitePaper.pdf`, [16 April 2011].

[16] Altium Designer version 9.4. Sydney, Australia: Altium Limited, 2009.

[17] "Preliminary Design Review: OSIRIS Lite 2 Balloon Payload." The Pennsylvania State University's Student Space Programs Laboratory. Found in SSPL Sharepoint Document Library, 8 Dec. 2010 [13 April 2011], pp. 127–9.

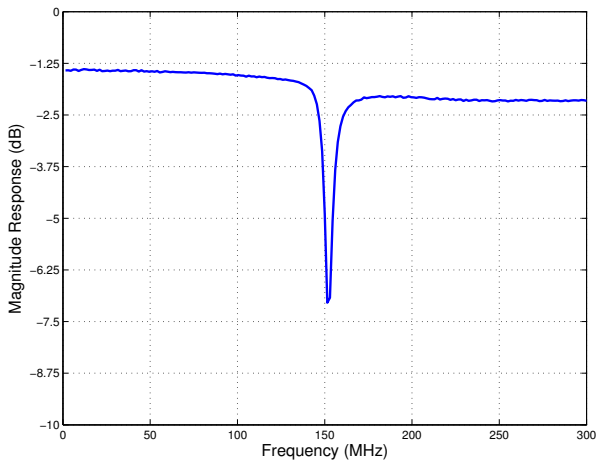
[18] F. Jordan. "SwissCube Electrical Power System." École Polytechnique Fédérale de Lausanne. Found at `http://ctsgepc7.epfl.ch/03%20-%20Power%20system/S3-B-EPS-1-1-Electrical_Power_System.pdf`, 20 Dec. 2006 [13 April 2011], p. 22.

Appendix A

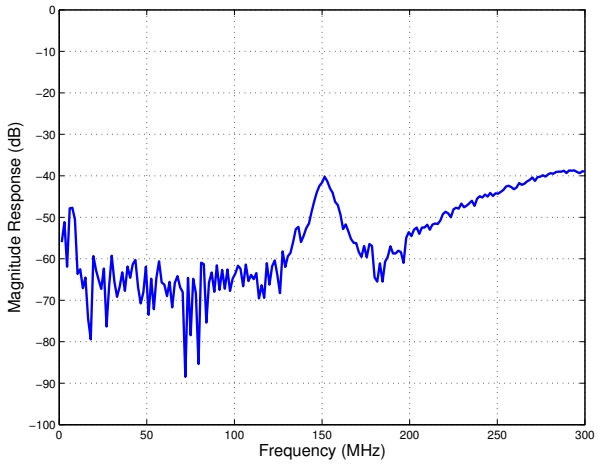
S-Parameter Plots

The following plots are the magnitude and phase *S*-parameter measurements made on the various band-pass filters and amplifiers (Chapter 4) used in the development of the PGRBR design.

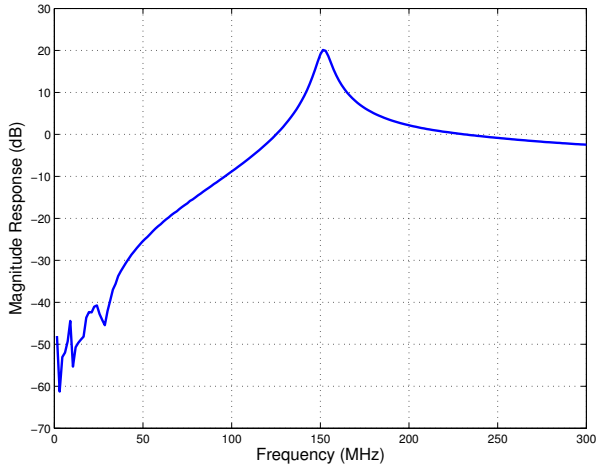
A.1 Preamplifier Responses



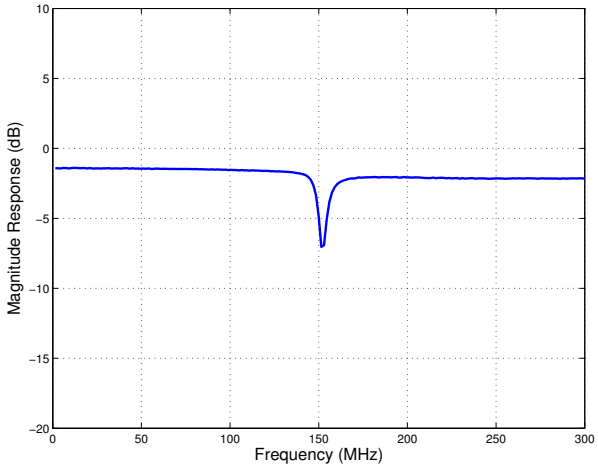
(a) S_{11} Magnitude Response



(b) S_{12} Magnitude Response

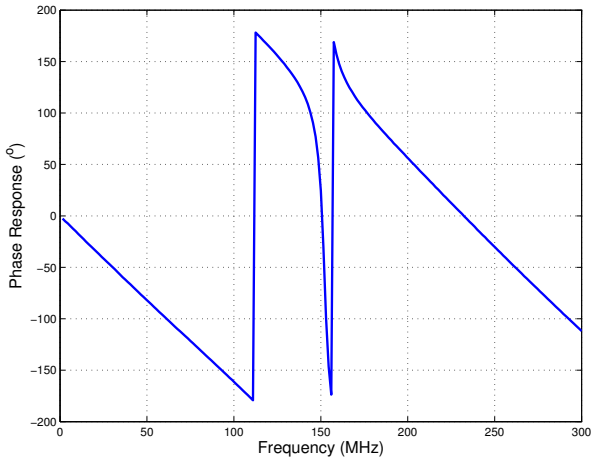


(c) S_{21} Magnitude Response

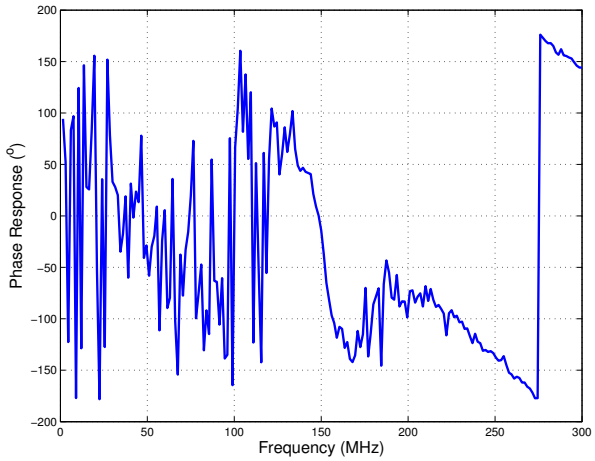


(d) S_{22} Magnitude Response

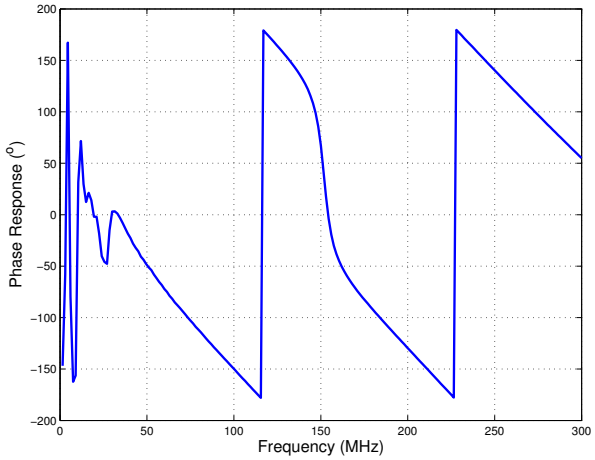
Figure A.1: S-Parameter Magnitude Responses of the Hamtronics LNK-146 Receiver Preamplifier.



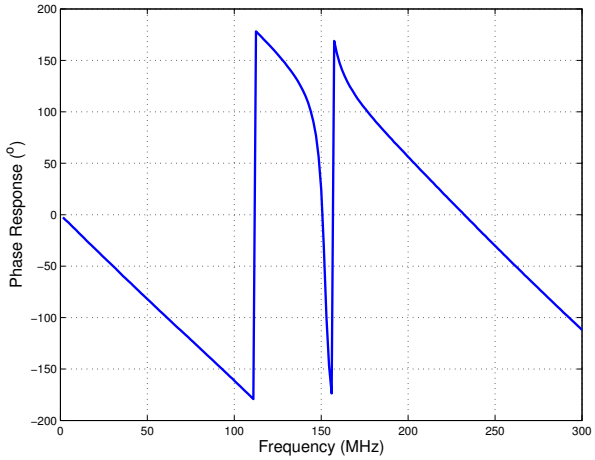
(a) S_{11} Phase Response



(b) S_{12} Phase Response

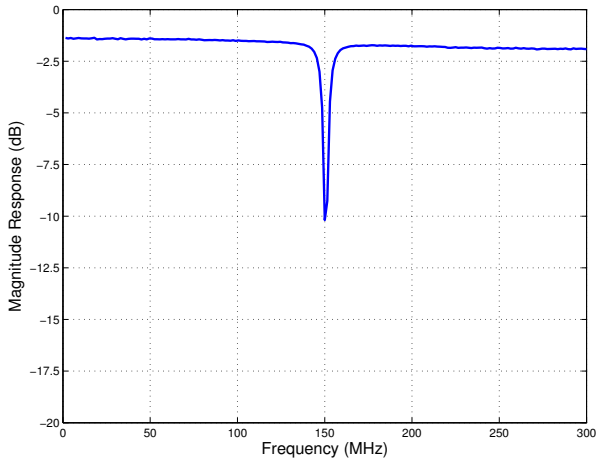


(c) S_{21} Phase Response

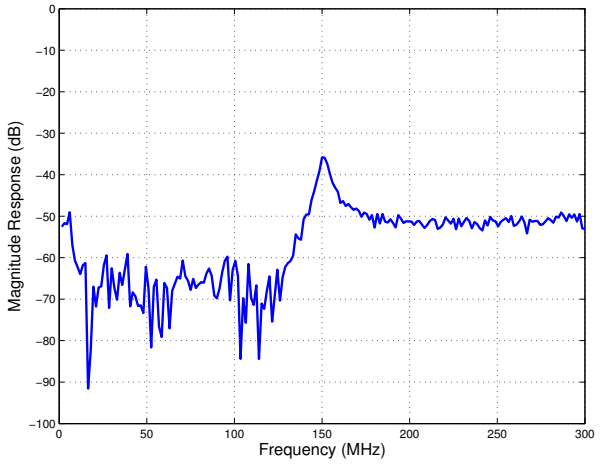


(d) S_{22} Phase Response

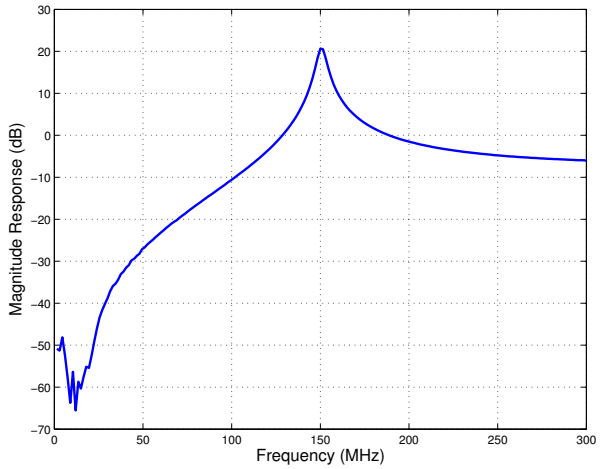
Figure A.2: *S*-Parameter Phase Responses of the Hamtronics LNK-146 Receiver Preamplifier.



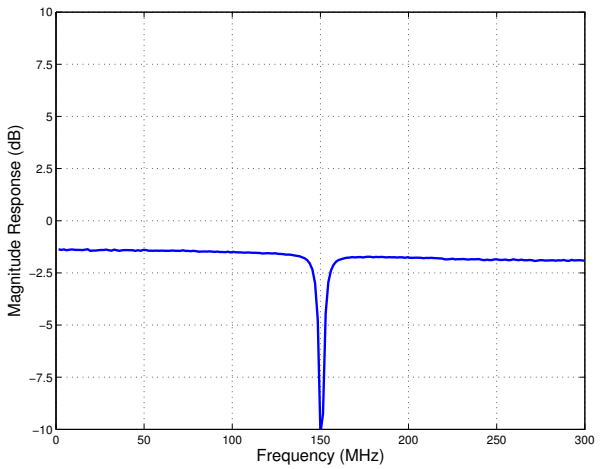
(a) S_{11} Magnitude Response



(b) S_{12} Magnitude Response

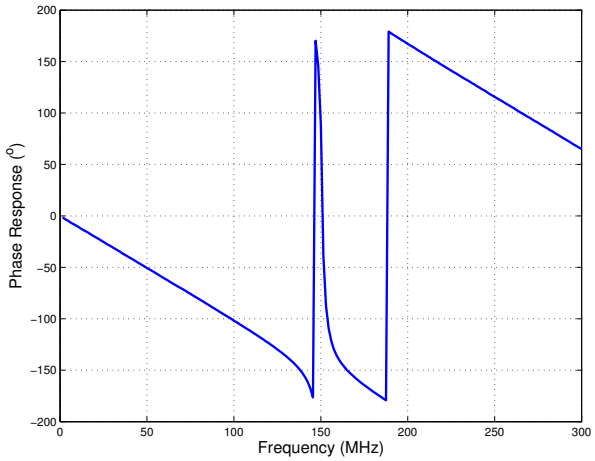


(c) S_{21} Magnitude Response

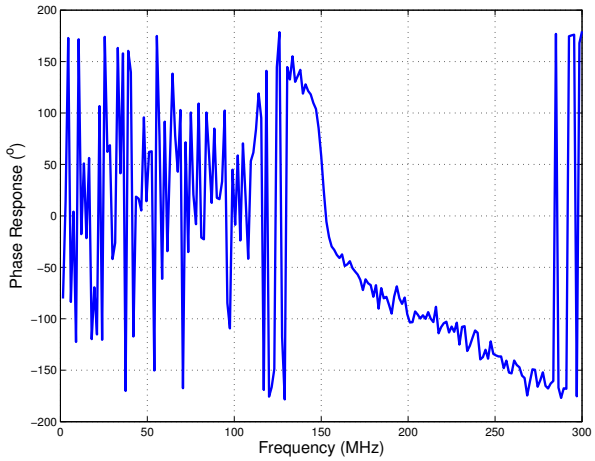


(d) S_{22} Magnitude Response

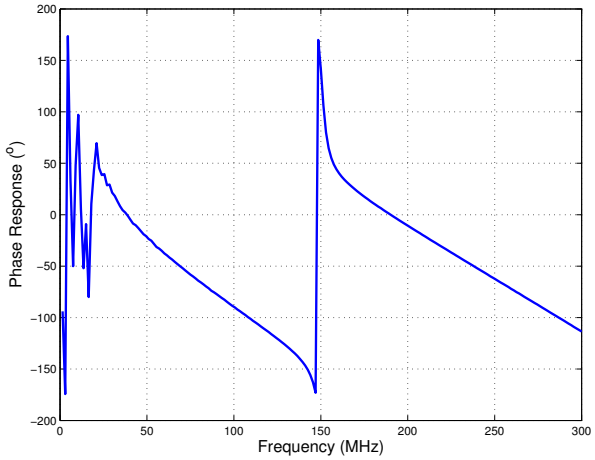
Figure A.3: S-Parameter Magnitude Responses of the Prototype LNK-146 Preamplifier.



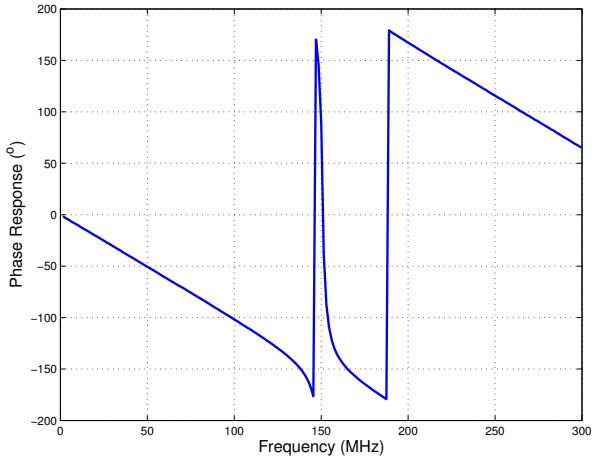
(a) S_{11} Phase Response



(b) S_{12} Phase Response

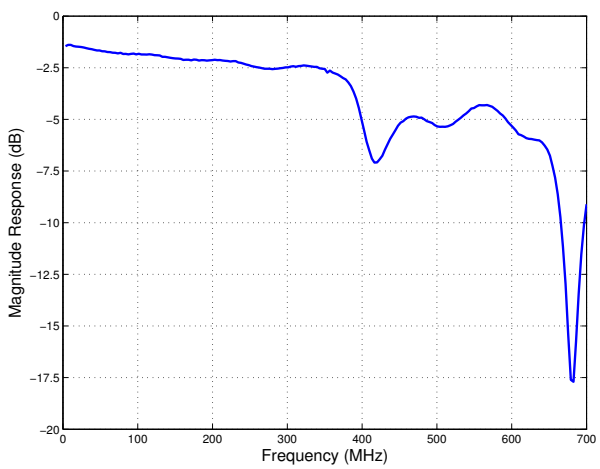


(c) S_{21} Phase Response

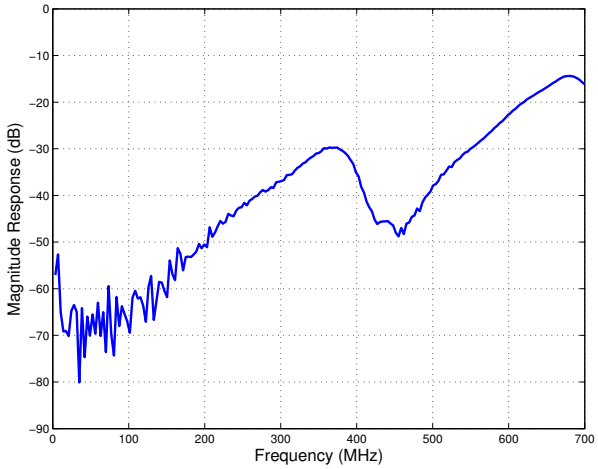


(d) S_{22} Phase Response

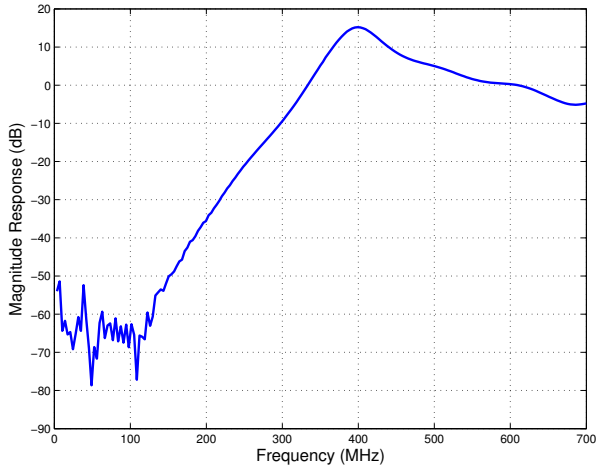
Figure A.4: *S*-Parameter Phase Responses of the Prototype LNK-146 Preamplifier.



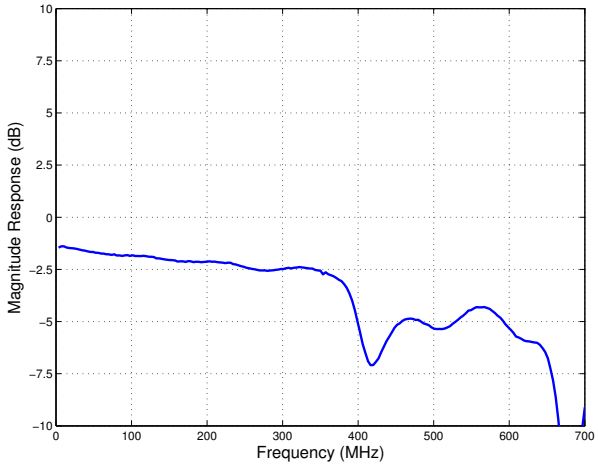
(a) S_{11} Magnitude Response



(b) S_{12} Magnitude Response

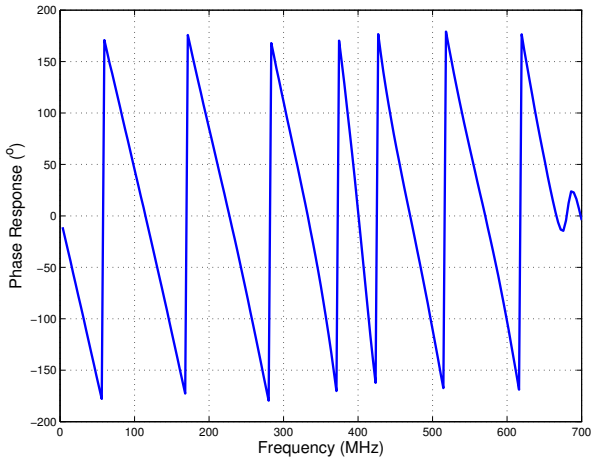


(c) S_{21} Magnitude Response

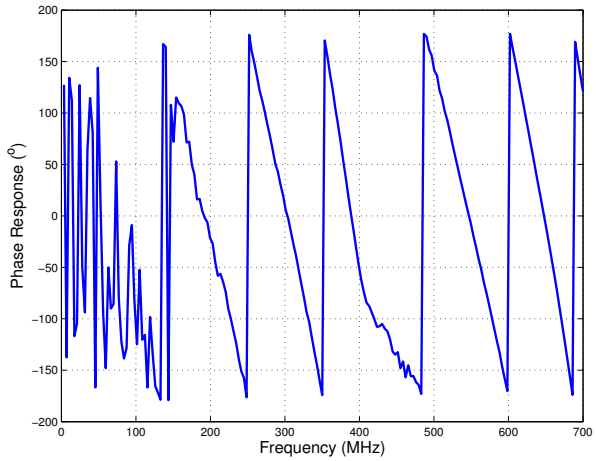


(d) S_{22} Magnitude Response

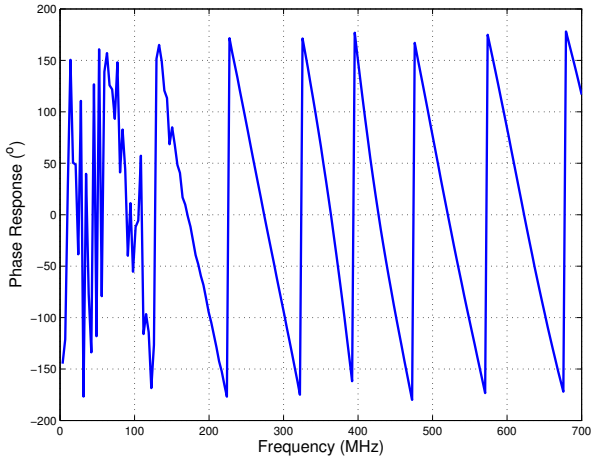
Figure A.5: S-Parameter Magnitude Responses of the Hamtronics LNK-450 Receiver Preamplifier.



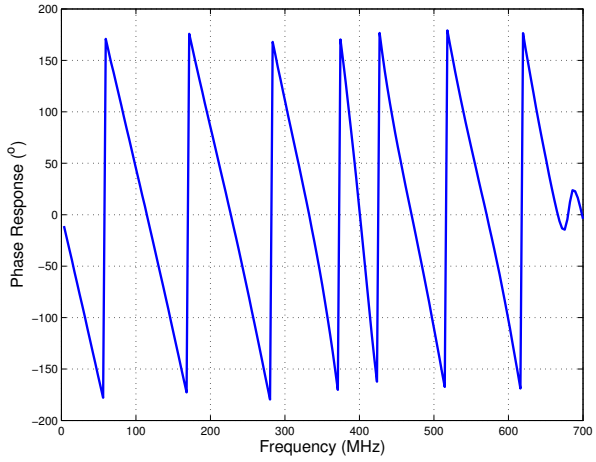
(a) S_{11} Phase Response



(b) S_{12} Phase Response

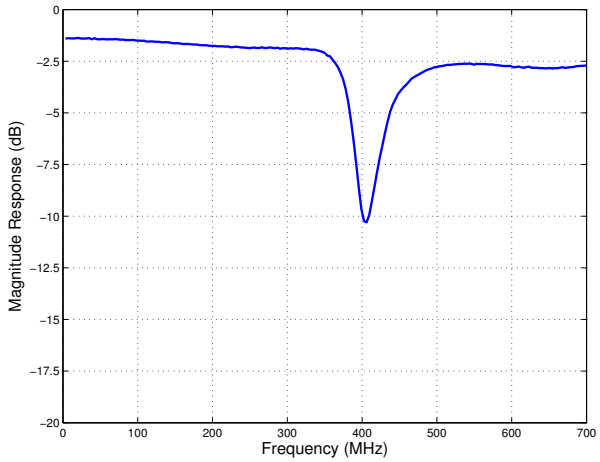


(c) S_{21} Phase Response

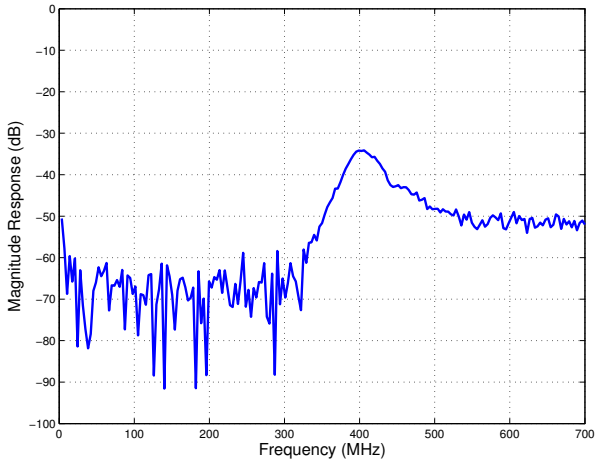


(d) S_{22} Phase Response

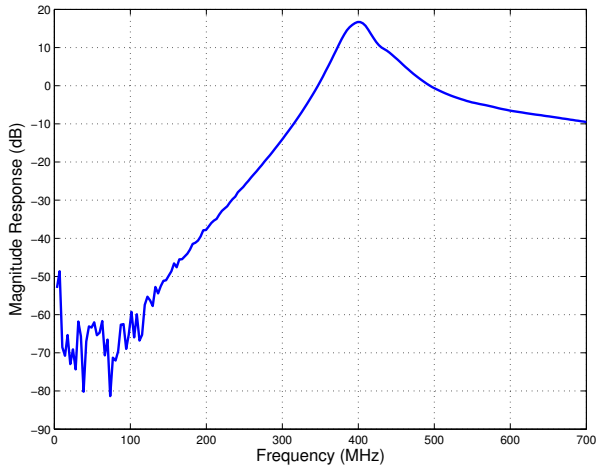
Figure A.6: *S*-Parameter Phase Responses of the Hamtronics LNK-450 Receiver Preamplifier.



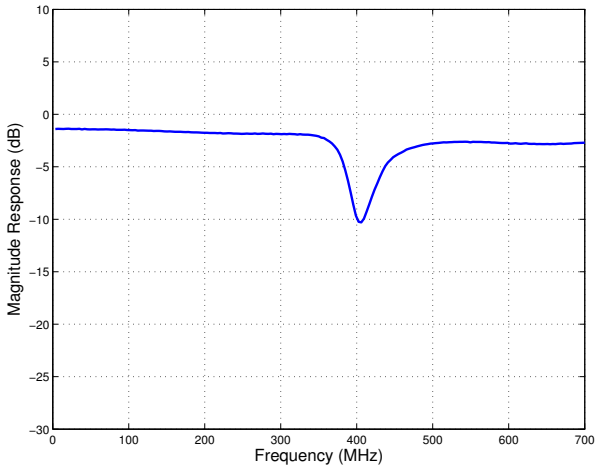
(a) S_{11} Magnitude Response



(b) S_{12} Magnitude Response

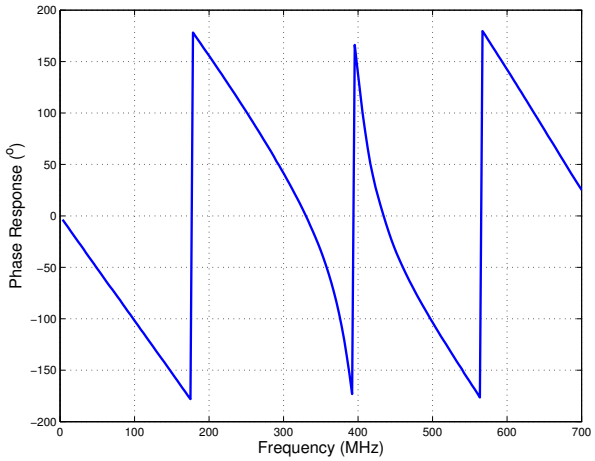


(c) S_{21} Magnitude Response

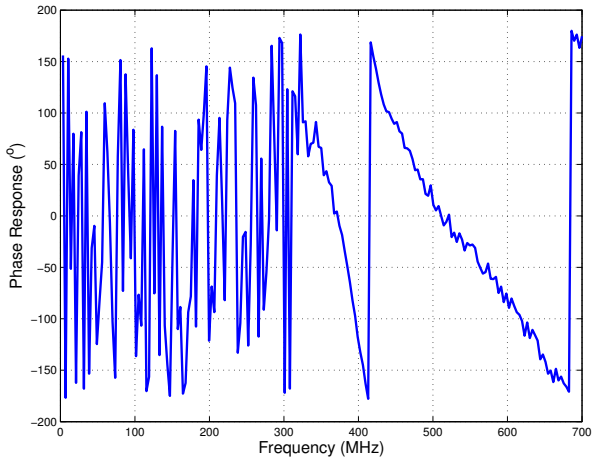


(d) S_{22} Magnitude Response

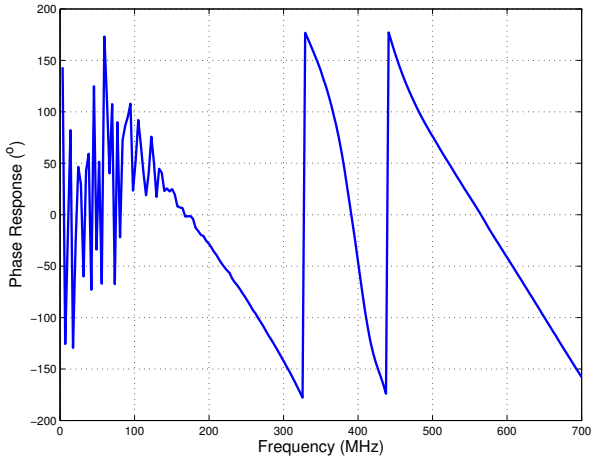
Figure A.7: S-Parameter Magnitude Responses of the Prototype LNK-450 Preamplifier.



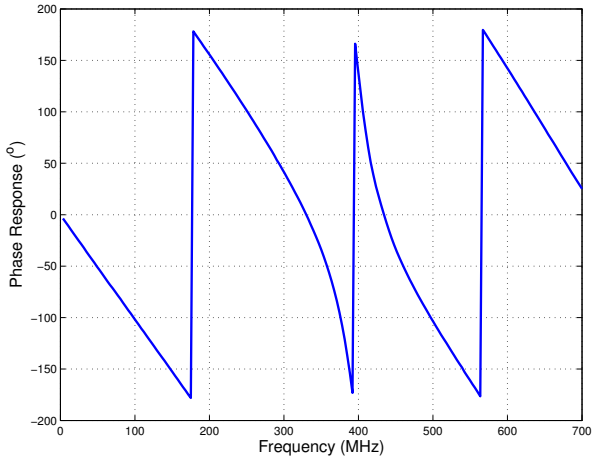
(a) S_{11} Phase Response



(b) S_{12} Phase Response



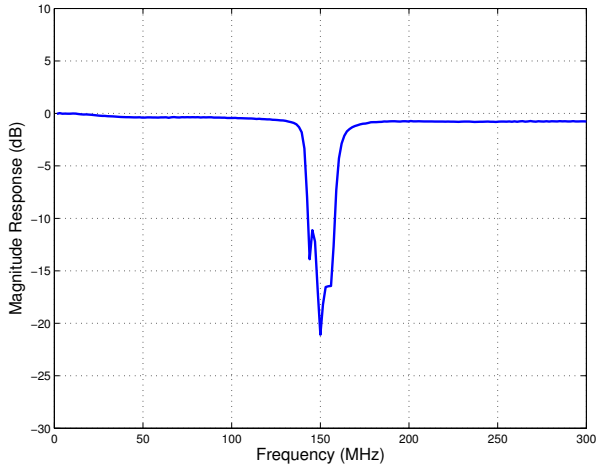
(c) S_{21} Phase Response



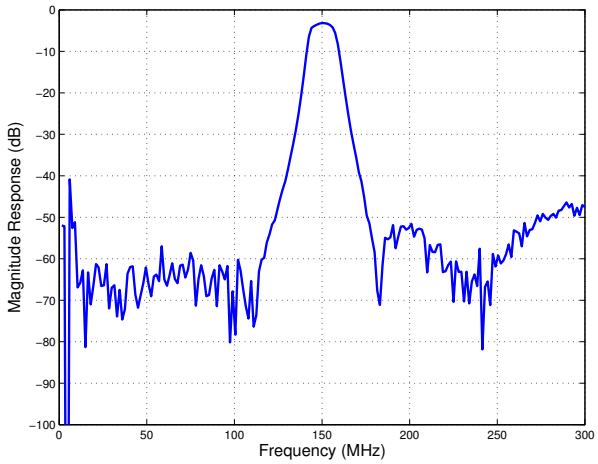
(d) S_{22} Phase Response

Figure A.8: *S*-Parameter Phase Responses of the Prototype LNK-450 Preamplifier.

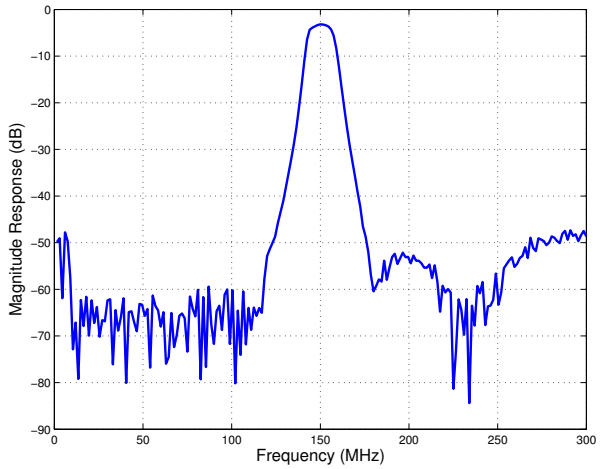
A.2 Band-Pass Filter Responses



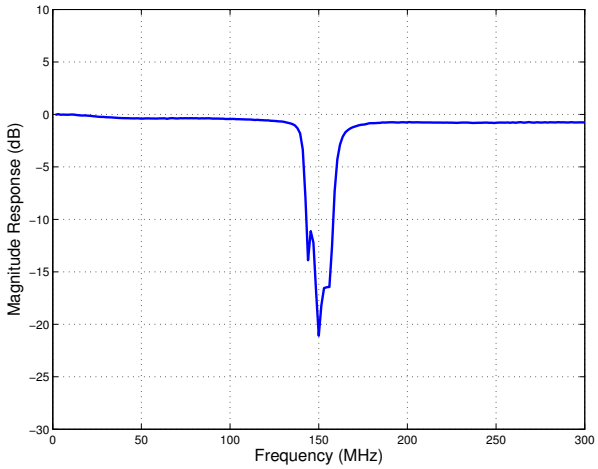
(a) S_{11} Magnitude Response



(b) S_{12} Magnitude Response

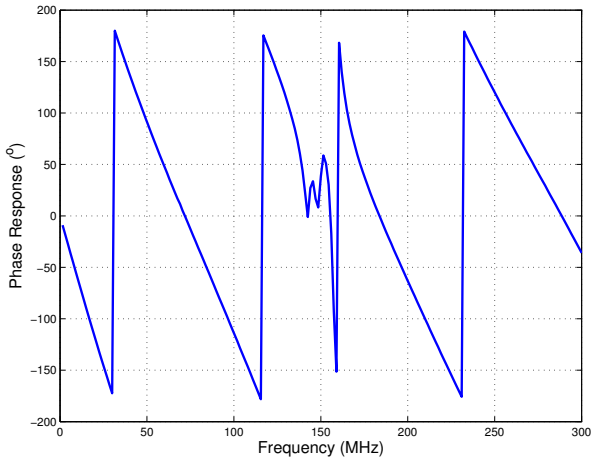


(c) S_{21} Magnitude Response

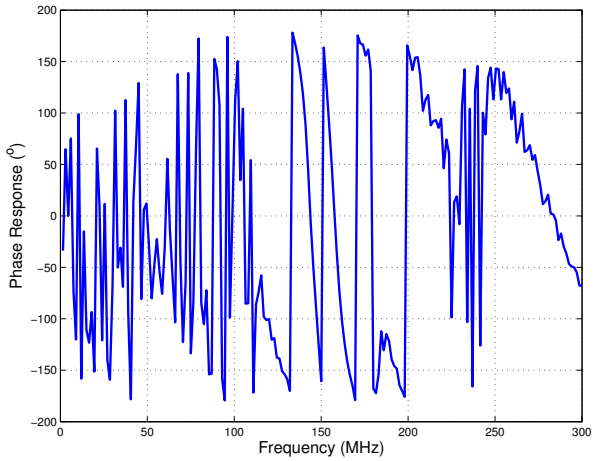


(d) S_{22} Magnitude Response

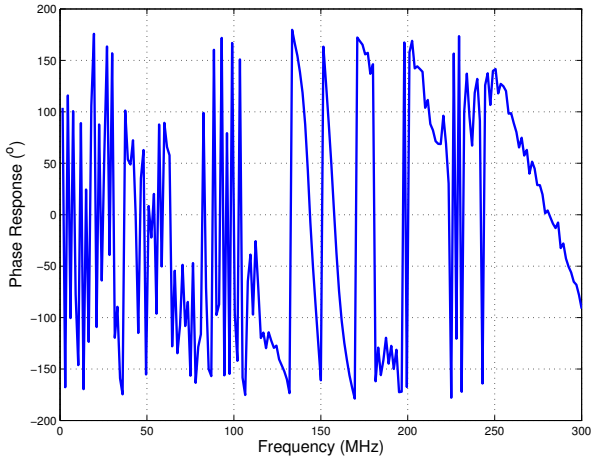
Figure A.9: S-Parameter Responses of the Lark Engineering MS150 Band-Pass Filter.



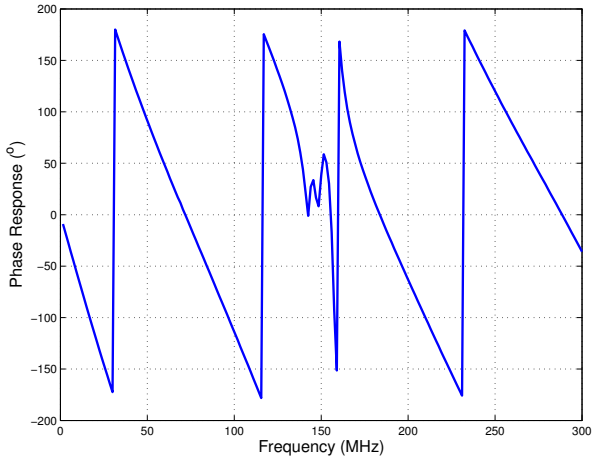
(a) S_{11} Phase Response



(b) S_{12} Phase Response

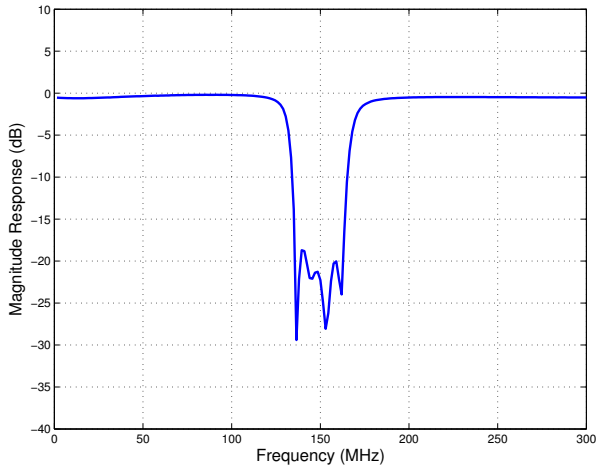


(c) S_{21} Phase Response

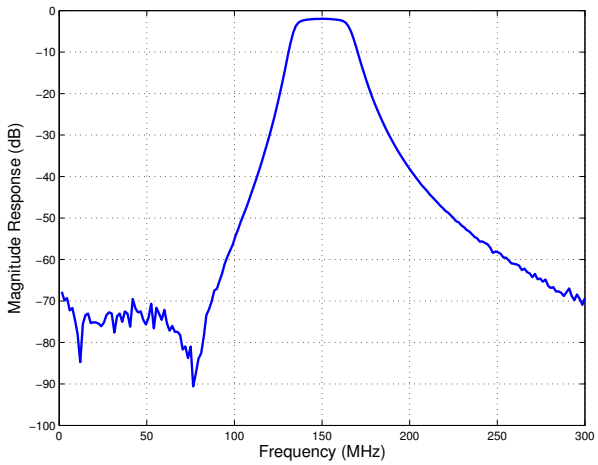


(d) S_{22} Phase Response

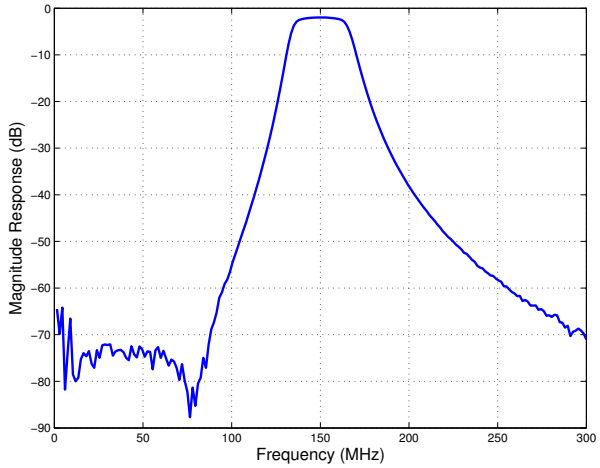
Figure A.10: S-Parameter Responses of the Lark Engineering MS150 Band-Pass Filter.



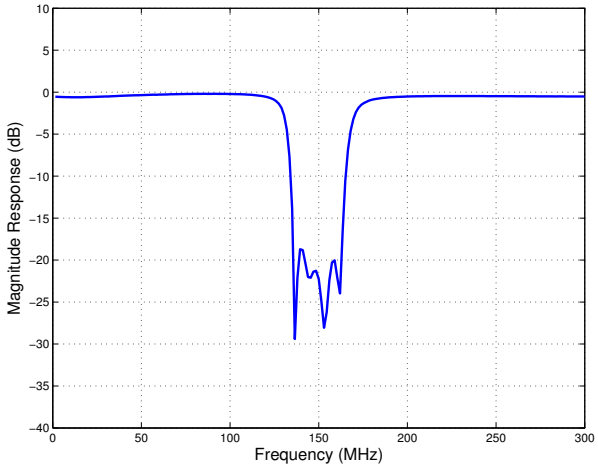
(a) S_{11} Magnitude Response



(b) S_{12} Magnitude Response

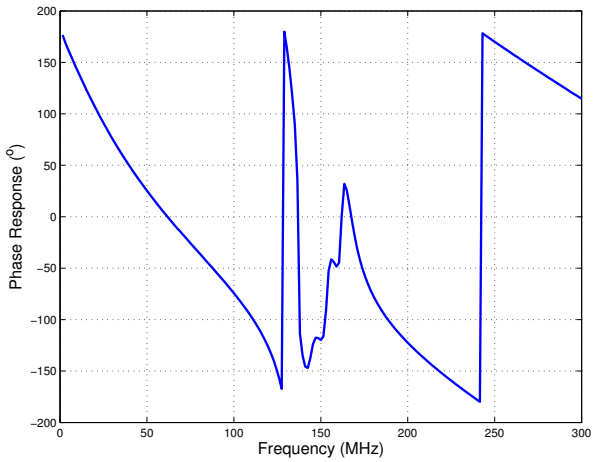


(c) S_{21} Magnitude Response

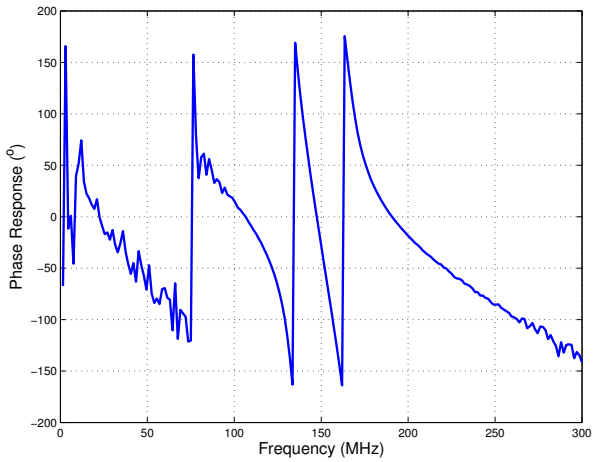


(d) S_{22} Magnitude Response

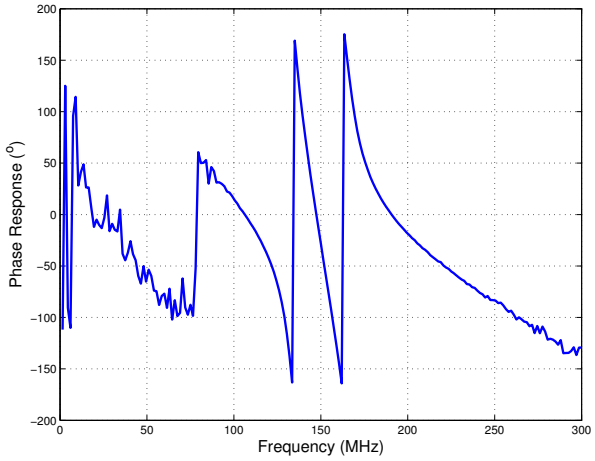
Figure A.11: S-Parameter Magnitude Responses of the Mini-Circuits SXBP-150+ Band-Pass Filter.



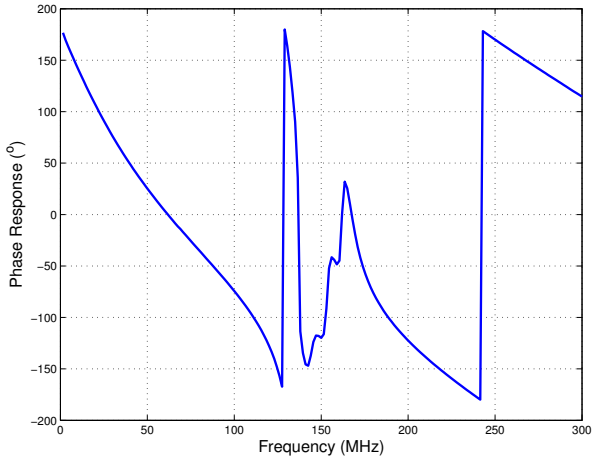
(a) S_{11} Phase Response



(b) S_{12} Phase Response

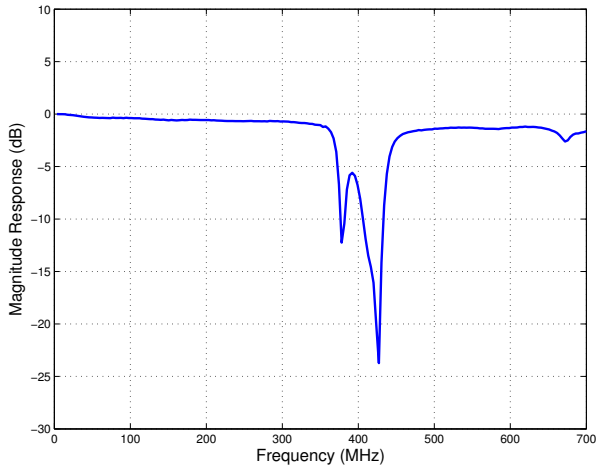


(c) S_{21} Phase Response

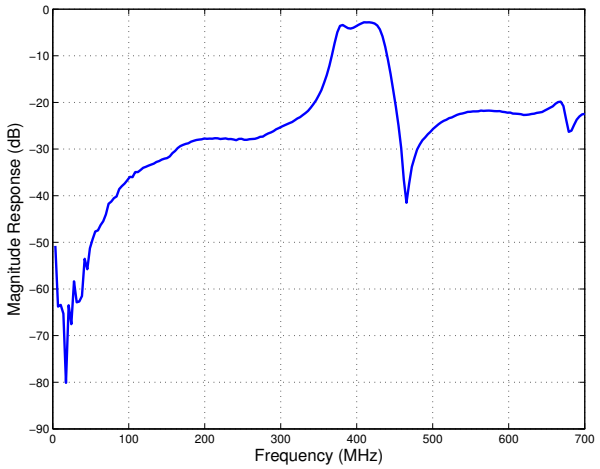


(d) S_{22} Phase Response

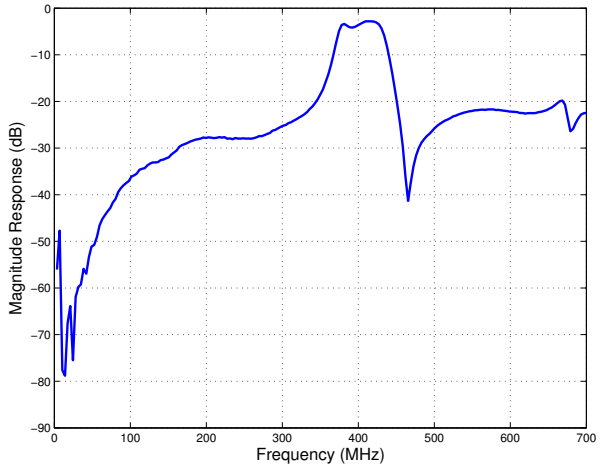
Figure A.12: *S*-Parameter Phase Responses of the Mini-Circuits SXBP-150+ Band-Pass Filter.



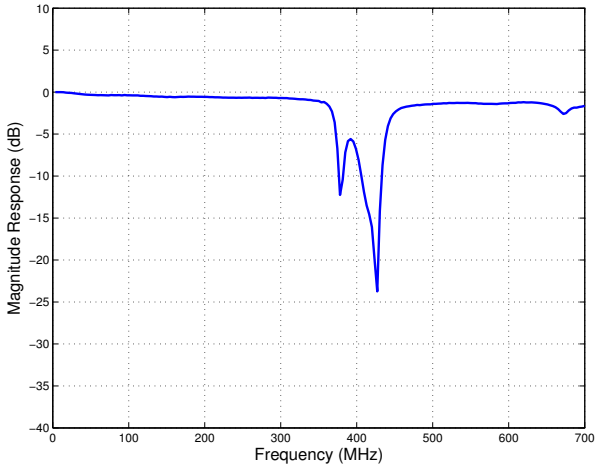
(a) S_{11} Magnitude Response



(b) S_{12} Magnitude Response

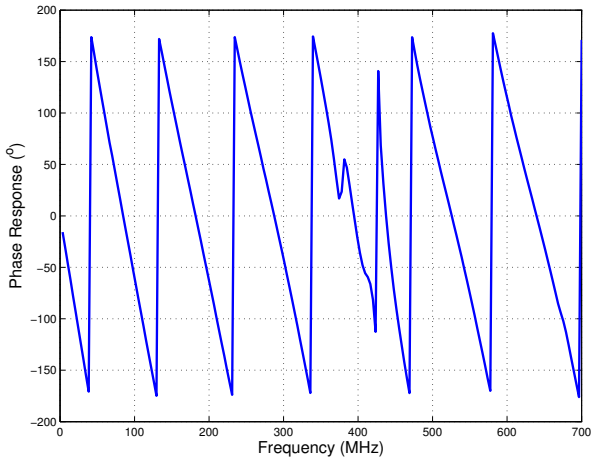


(c) S_{21} Magnitude Response

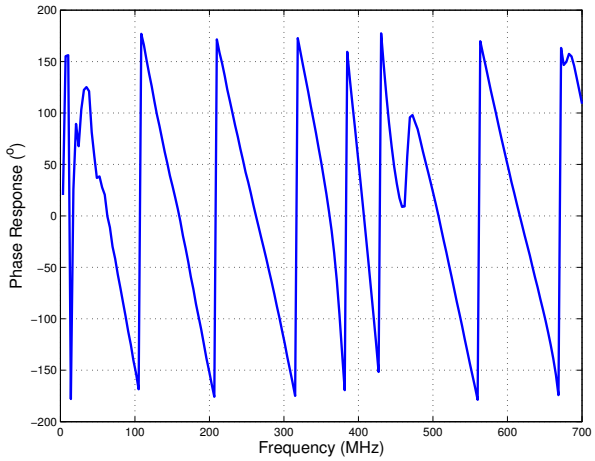


(d) S_{22} Magnitude Response

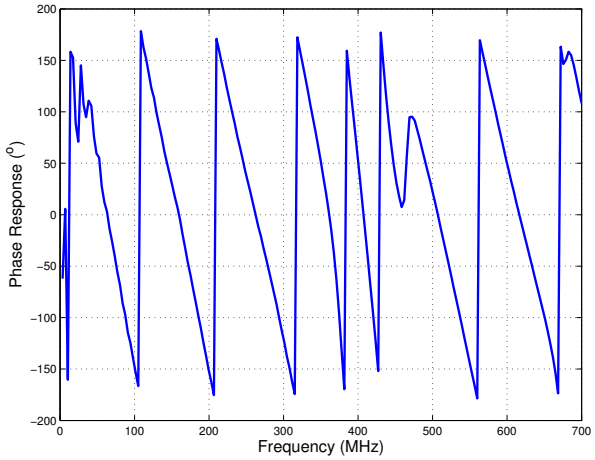
Figure A.13: S-Parameter Responses of the Lark Engineering MS400 Band-Pass Filter.



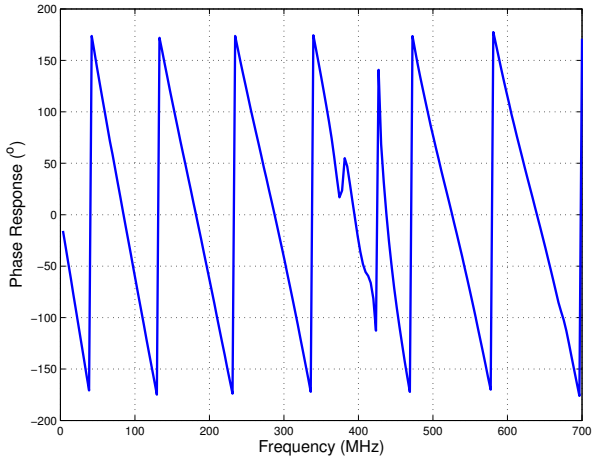
(a) S_{11} Phase Response



(b) S_{12} Phase Response

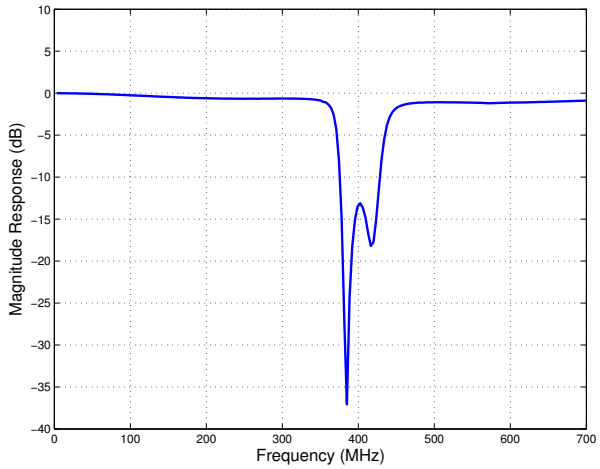


(c) S_{21} Phase Response

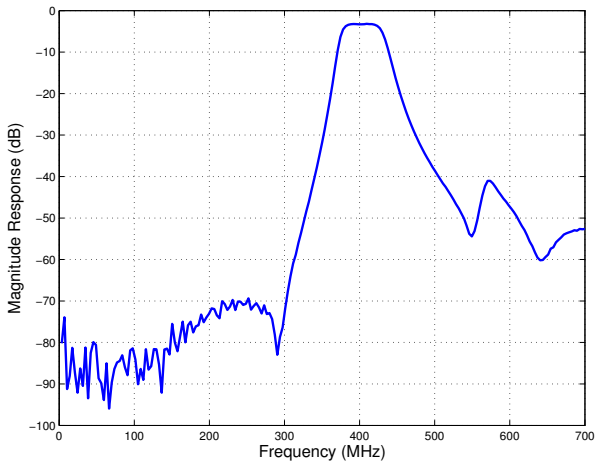


(d) S_{22} Phase Response

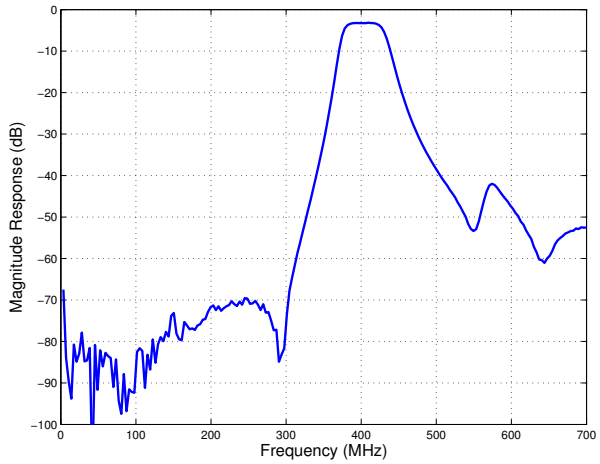
Figure A.14: *S*-Parameter Responses of the Lark Engineering MS400 Band-Pass Filter.



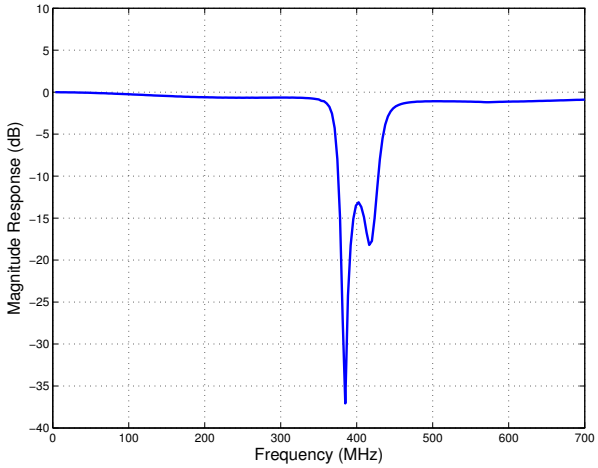
(a) S_{11} Magnitude Response



(b) S_{12} Magnitude Response

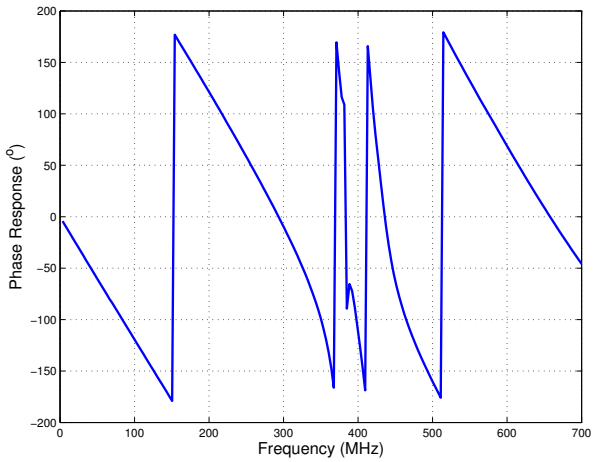


(c) S_{21} Magnitude Response

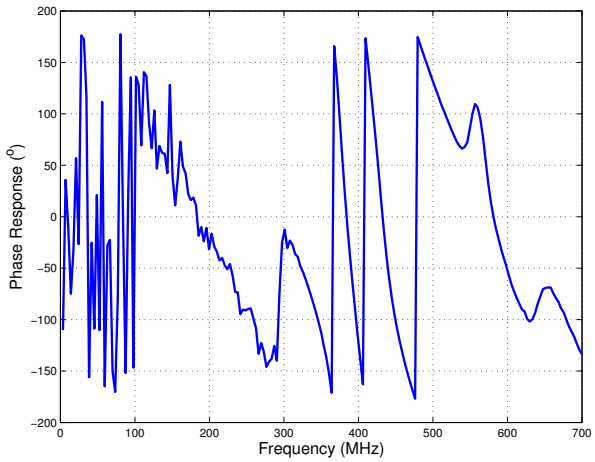


(d) S_{22} Magnitude Response

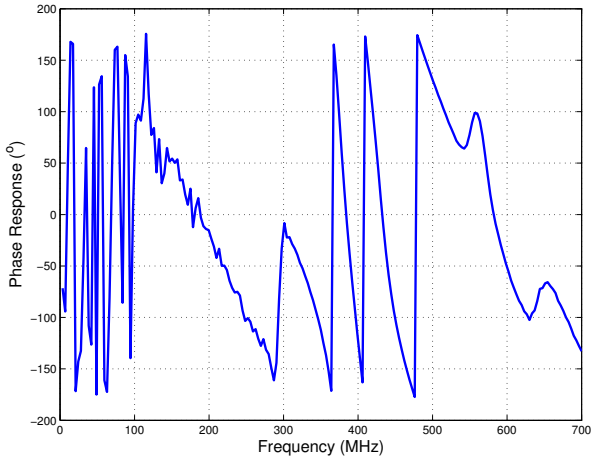
Figure A.15: S-Parameter Magnitude Responses of the Mini-Circuits BPF-A400+ Band-Pass Filter.



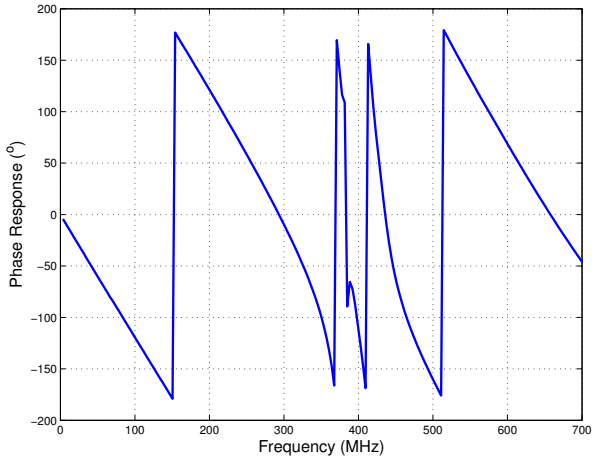
(a) S_{11} Phase Response



(b) S_{12} Phase Response



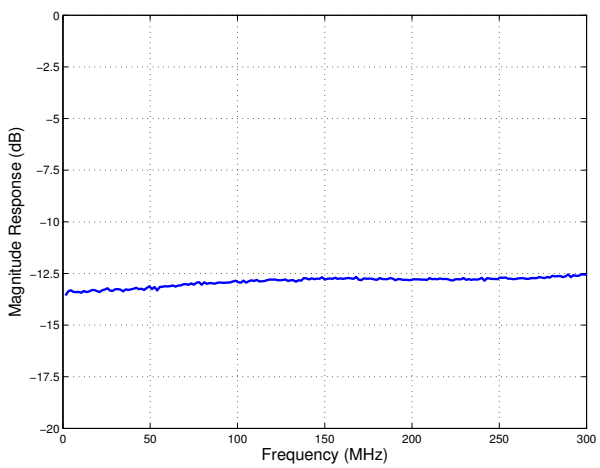
(c) S_{21} Phase Response



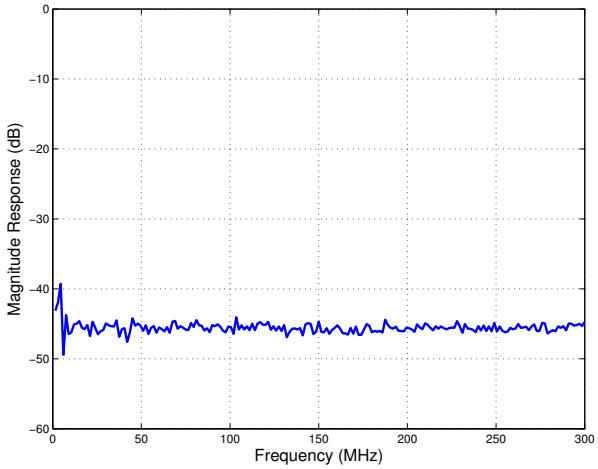
(d) S_{22} Phase Response

Figure A.16: *S*-Parameter Phase Responses of the Mini-Circuits BPF-A400+ Band-Pass Filter.

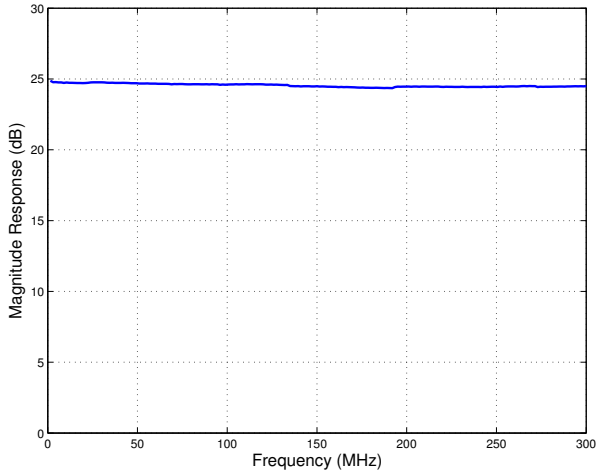
A.3 Wideband Amplifier Responses



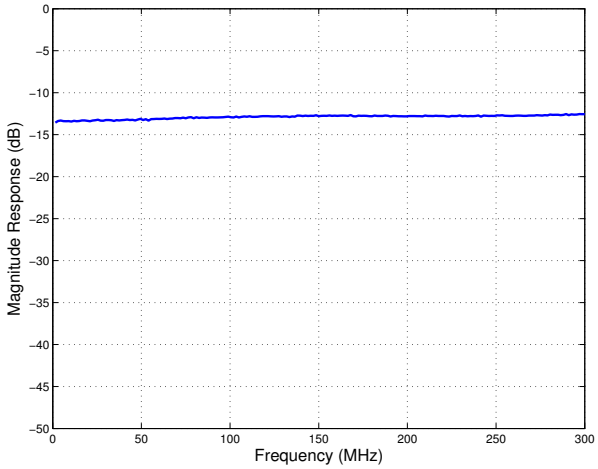
(a) S_{11} Magnitude Response



(b) S_{12} Magnitude Response

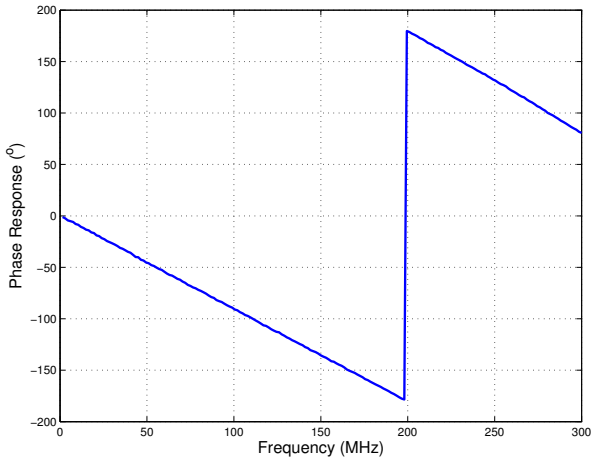


(c) S_{21} Magnitude Response

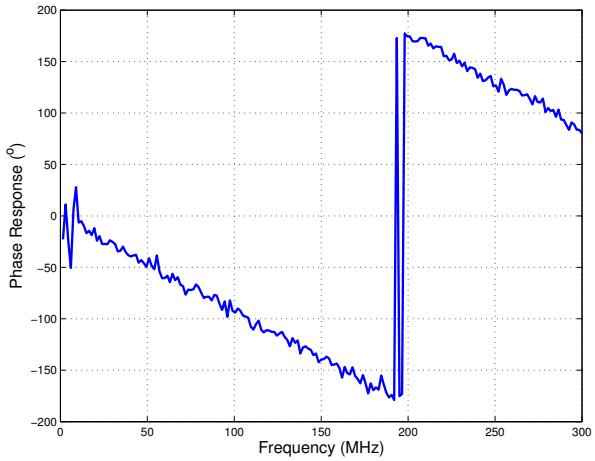


(d) S_{22} Magnitude Response

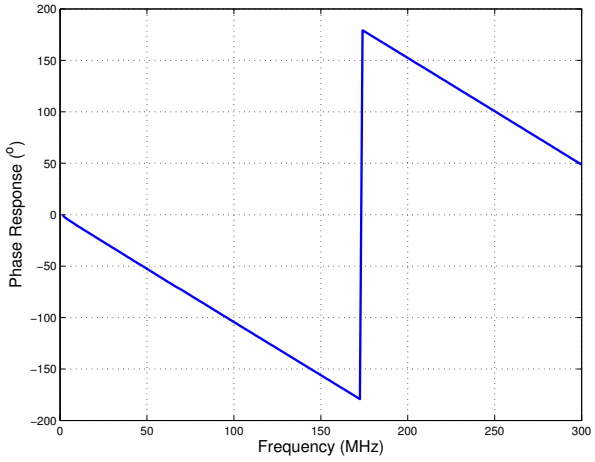
Figure A.17: *S*-Parameter Magnitude Responses of the Mini-Circuits ZFL-500LN+ Amplifier.



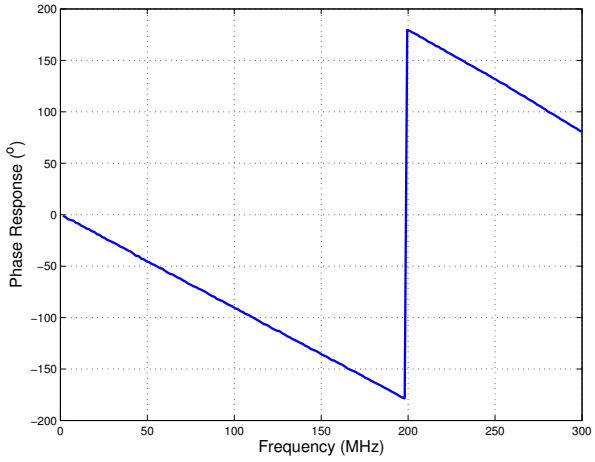
(a) S_{11} Phase Response



(b) S_{12} Phase Response

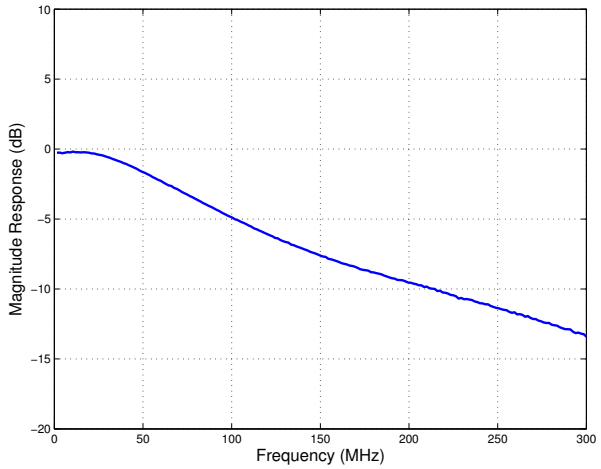


(c) S_{21} Phase Response

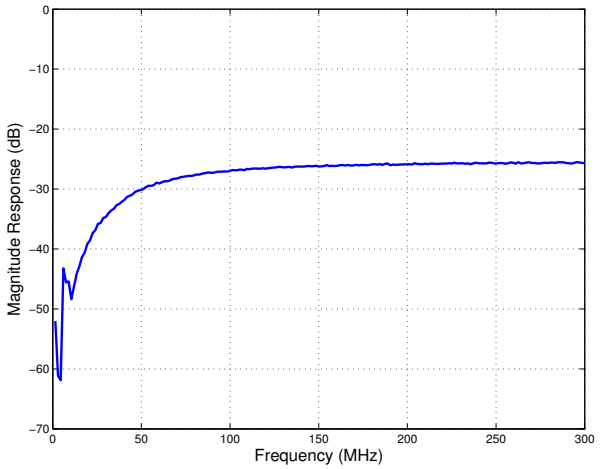


(d) S_{22} Phase Response

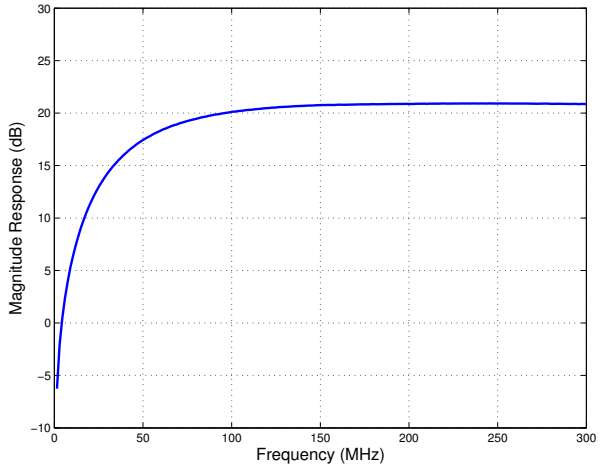
Figure A.18: *S*-Parameter Phase Responses of the Mini-Circuits ZFL-500LN+ Amplifier.



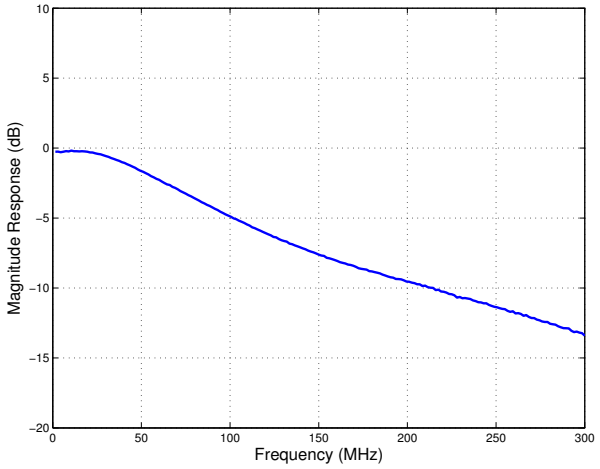
(a) S_{11} Magnitude Response



(b) S_{12} Magnitude Response

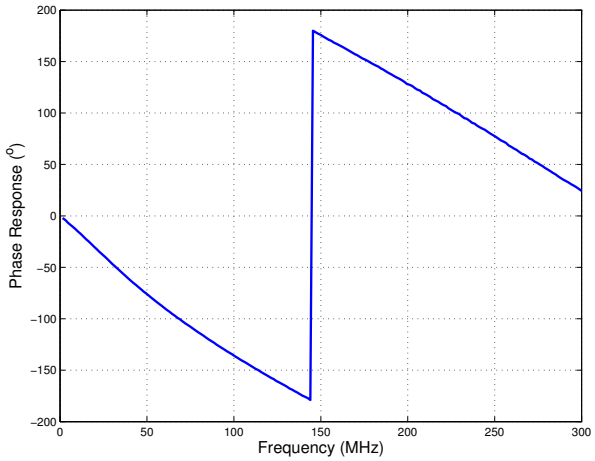


(c) S_{21} Magnitude Response

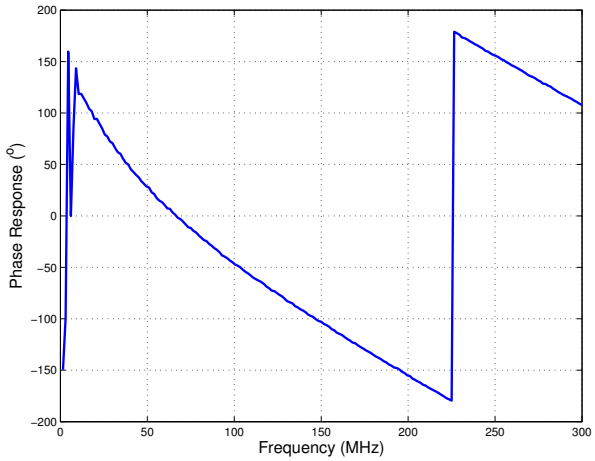


(d) S_{22} Magnitude Response

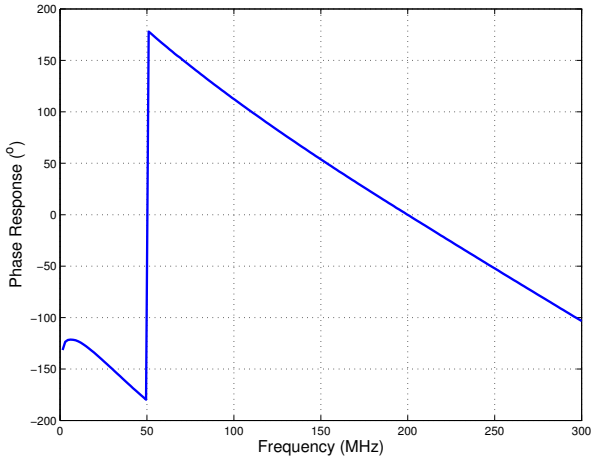
Figure A.19: *S*-Parameter Magnitude Responses of the RFX-400 Wideband Amplifier.



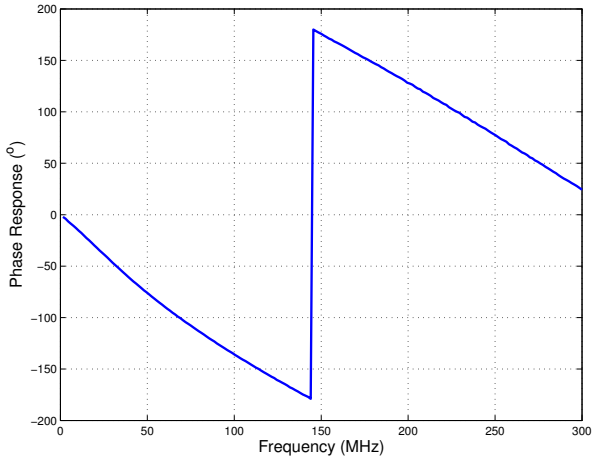
(a) S_{11} Phase Response



(b) S_{12} Phase Response



(c) S_{21} Phase Response



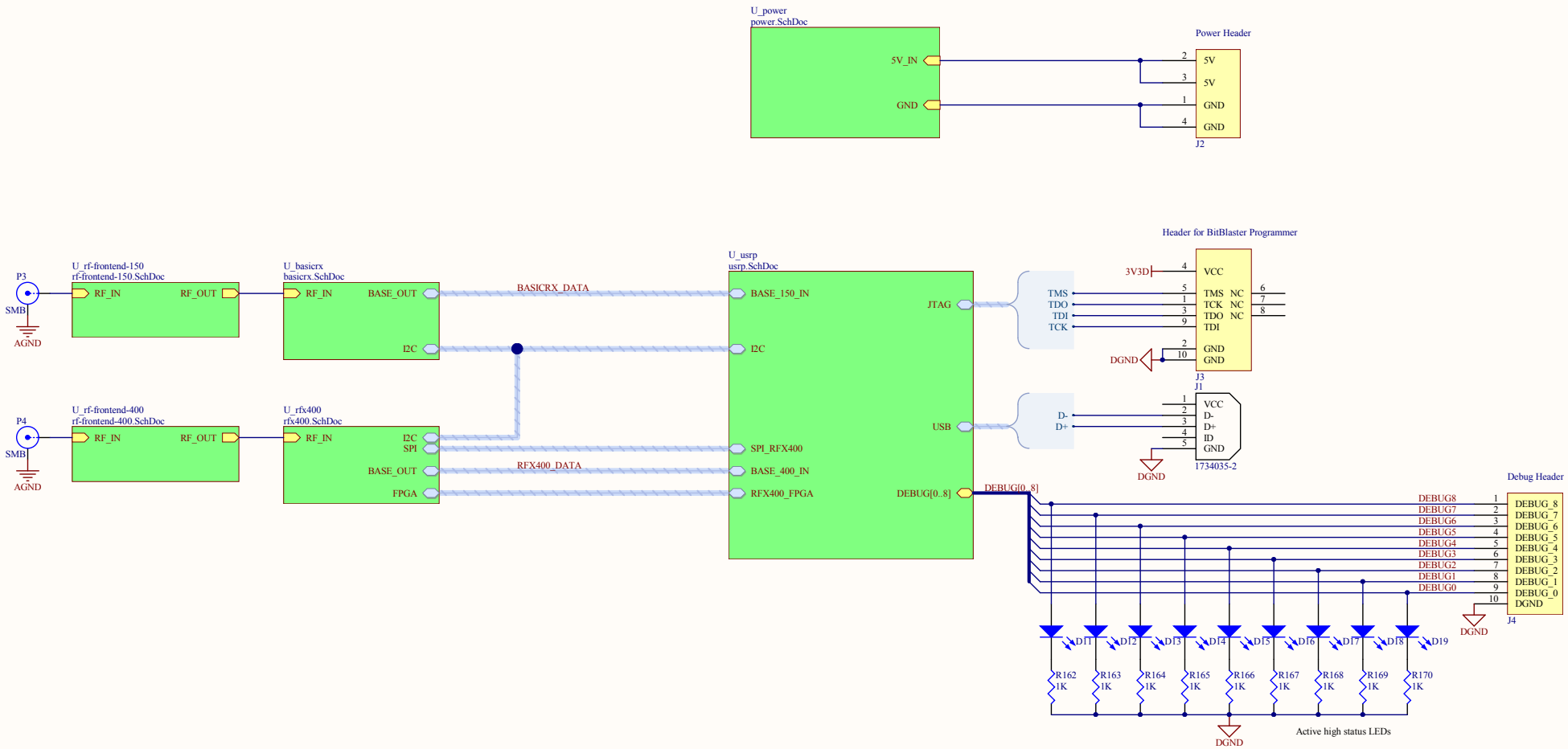
(d) S_{22} Phase Response

Figure A.20: *S*-Parameter Phase Responses of the RFX-400 Wideband Amplifier.

Appendix B

Electrical Schematic Diagrams

The following schematics illustrate the design used in the PGRBR PCB. These schematics were generated using Altium Designer 9. Post-manufacturing changes have been labeled as "white-wired."



Title: PGRBR		
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Date: 4/9/2011	Sheet 1 of 28	
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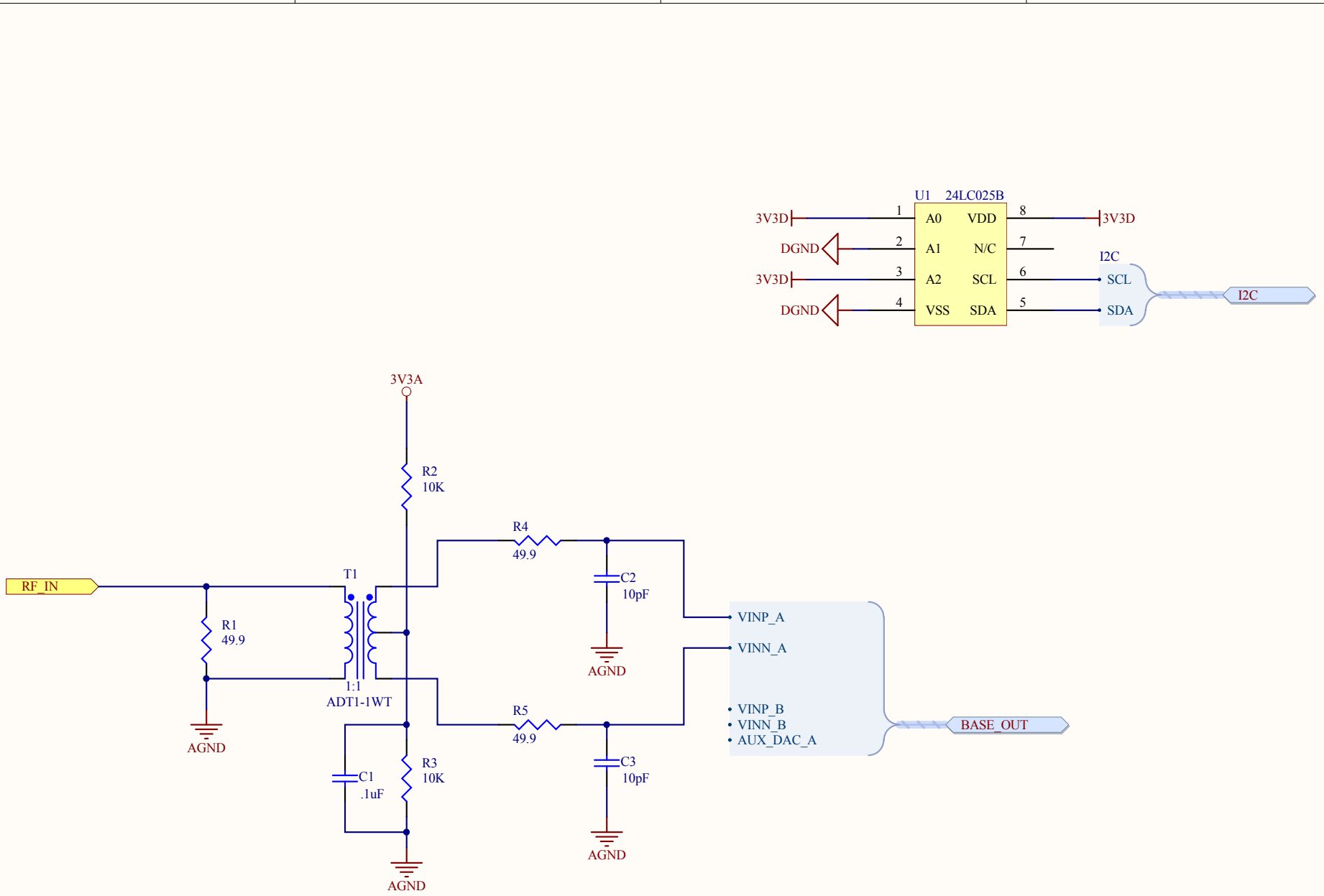
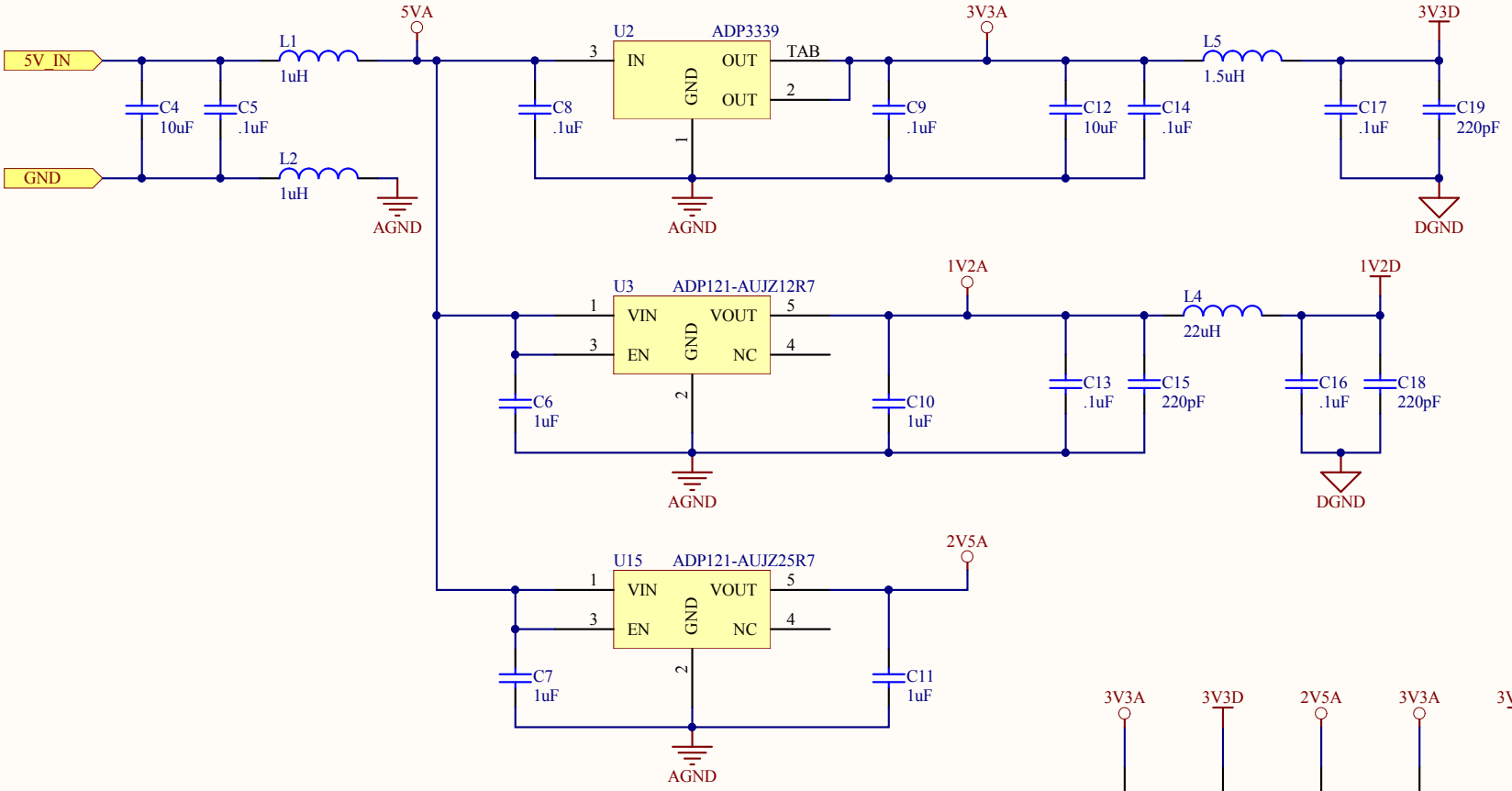
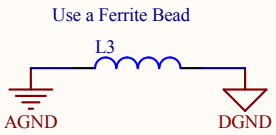
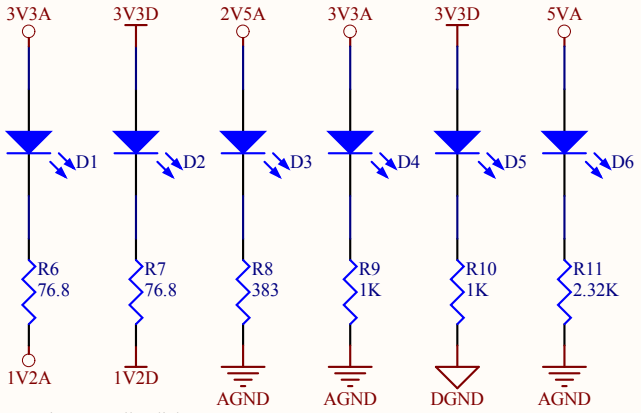


Title: **BasicRX**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011		Sheet 2 of 28
File: C:\Documents and Settings\..\basicrx.SchDoc		Drawn By: Alexander Hackett

These filter values are not exact and can be changed

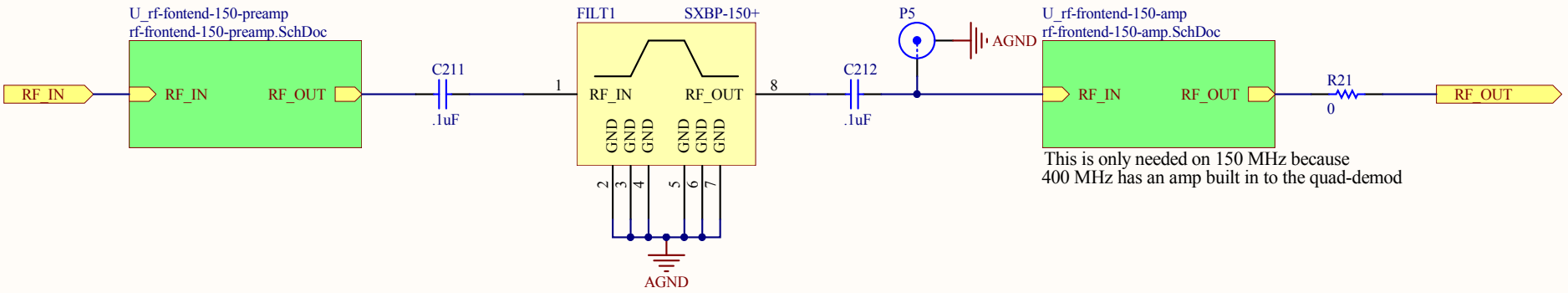






1.2V is too small to light an LED
This checks to make sure 1V2A/D aren't floating

Title: **Power**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011		Sheet 3 of 28
File: C:\Documents and Settings\..\power.SchDoc		Drawn By: Alexander Hackett



Title: **150 MHz RF Frontend**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 4 of 28	
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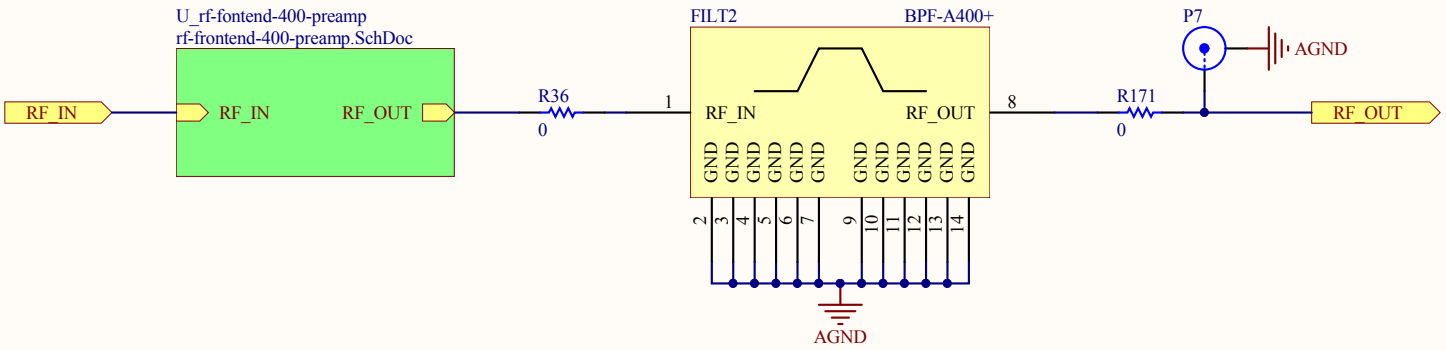

Title	**400 MHz RF Frontend**	
Size: A	Number:	Revision: 1.0
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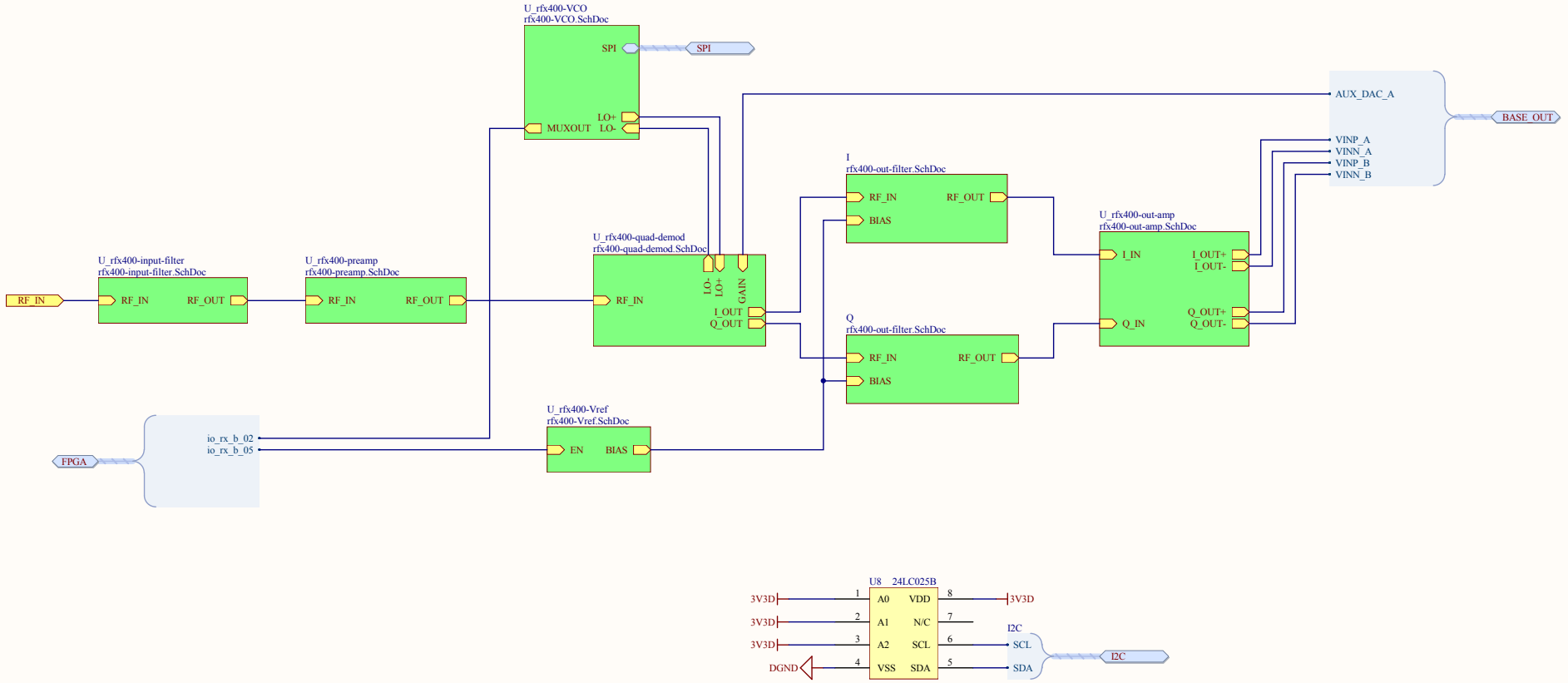
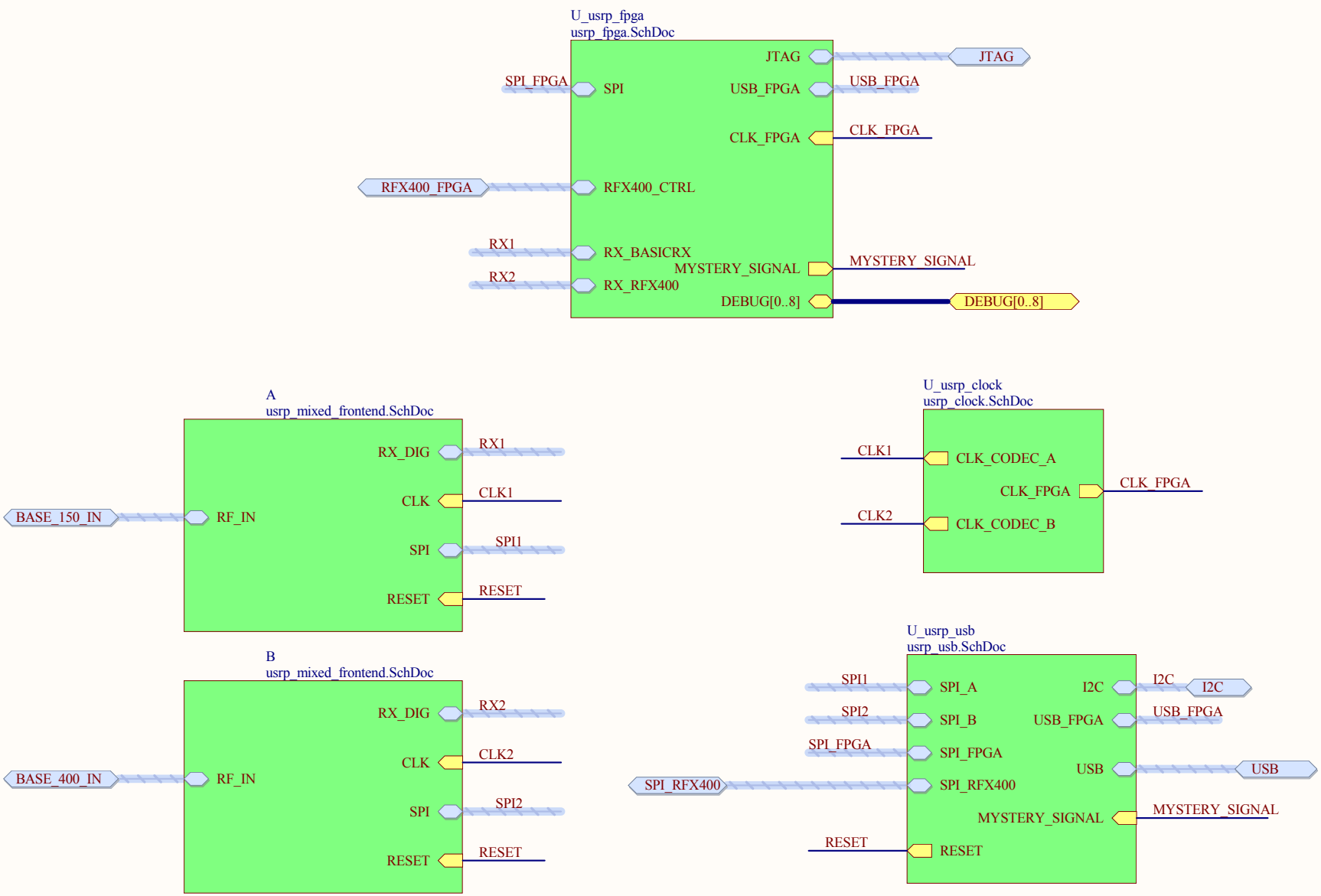
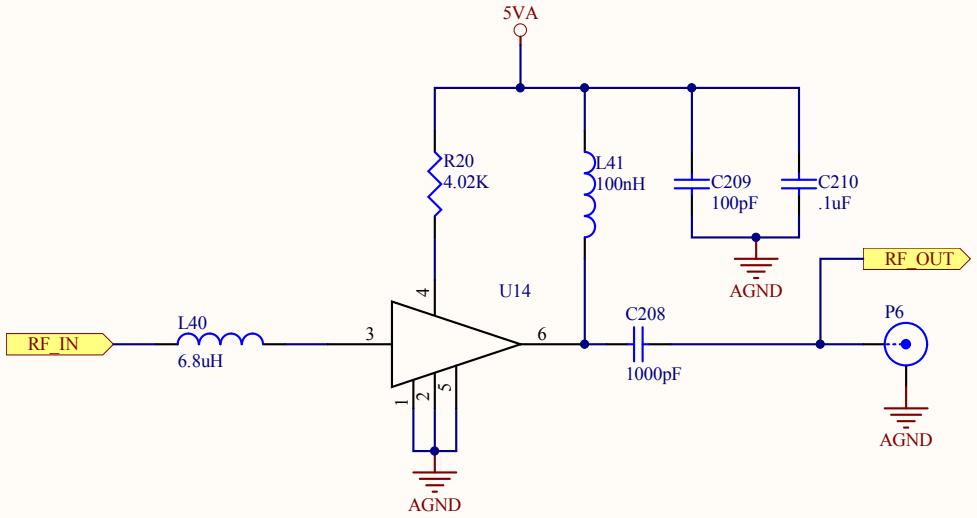
File: C:\Documents and Settings\..\rf-frontend-400.SchDoc		Drawn By: Alexander Hackett



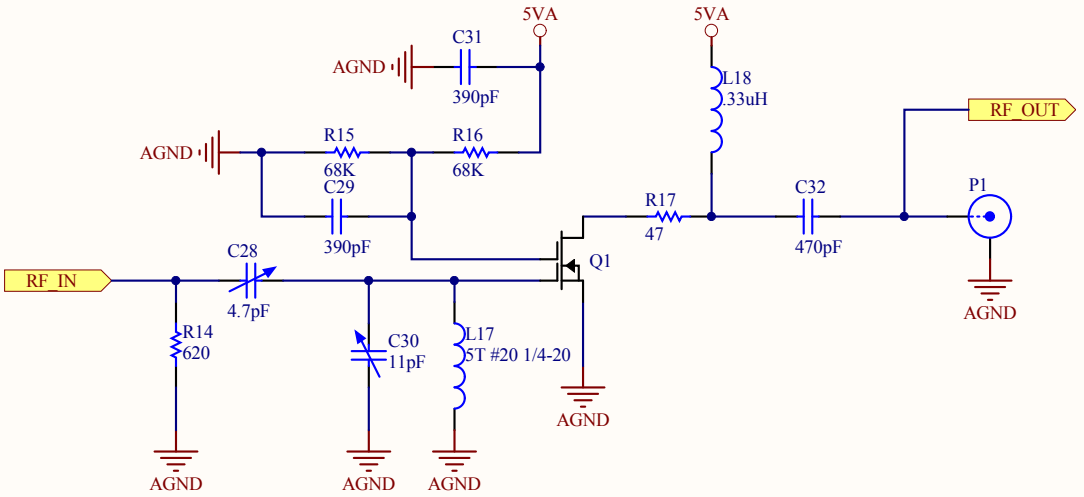
Title: **RFX400**		
Size: B	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 6 of 28	
File: C:\Documents and Settings\...\rfx400.SchDoc	Drawn By: Alexander Hackett	



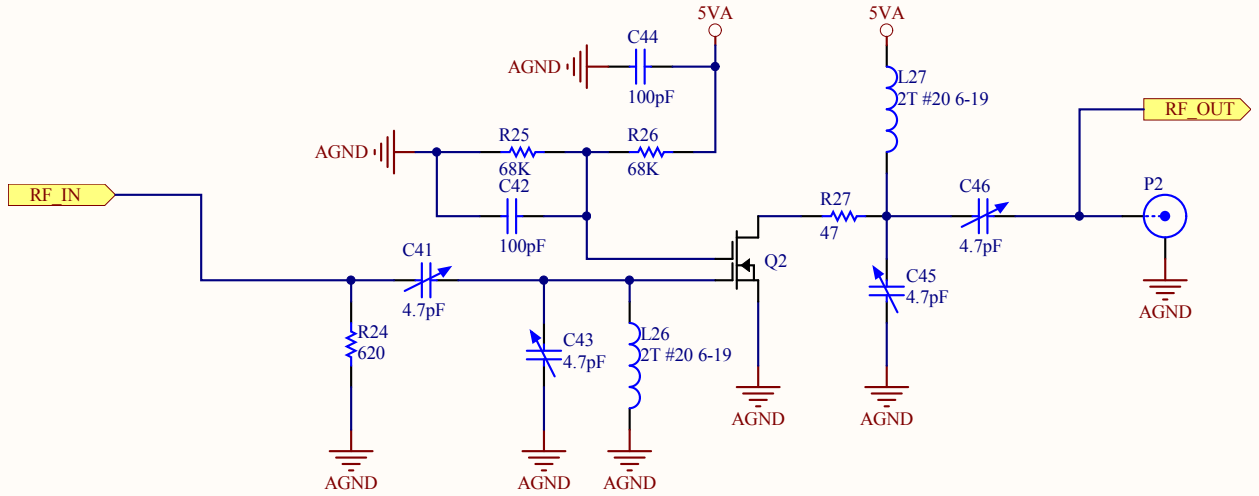
Title: **USRP**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011		Sheet 7 of 28
File: C:\Documents and Settings\..\usrp.SchDoc		Drawn By: Alexander Hackett



Title	**150 MHz Amplifier**		
Size: A	Number:		Revision: 1.0
Date: 4/9/2011		Sheet 8 of 28	
File: C:\Documents and Settings\...\rf-frontend-150amp.SchDoc		Drawn By:	Alexander Hackett



Title	**150 MHz Preamplifier**		
Size: A	Number:		Revision: 1.0
Date: 4/9/2011		Sheet 9 of 28	
File: C:\Documents and Settings\..\rf-frontend-150\preamp.SchDoc			Alexander Hackett



Title: **400 MHz Preamplifier**		
Size: A	Number:	Revision: 1.0
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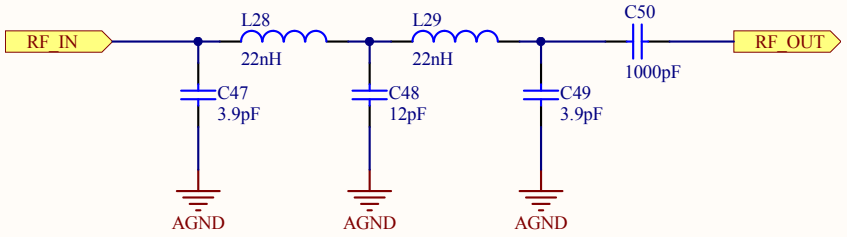
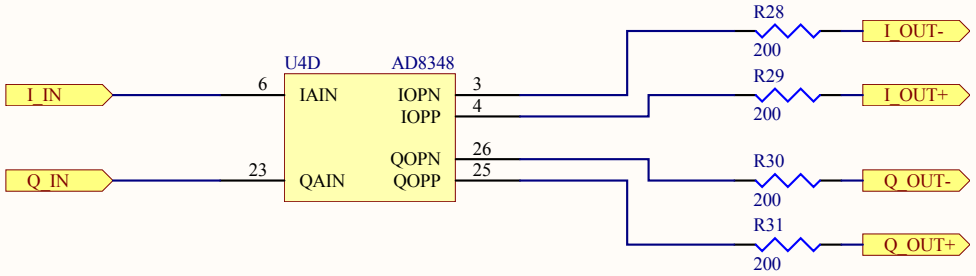
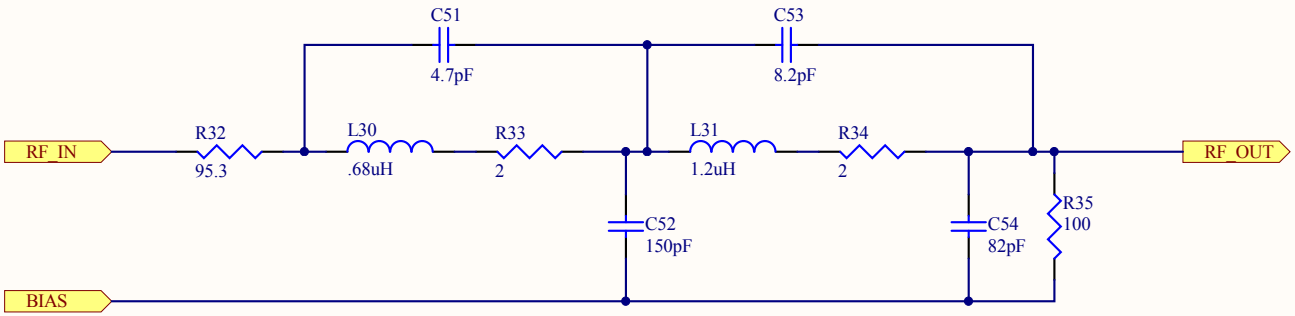
File: C:\Documents and Settings\..\rf-frontend-400Preamp.SchDoc	Alexander Hackett	



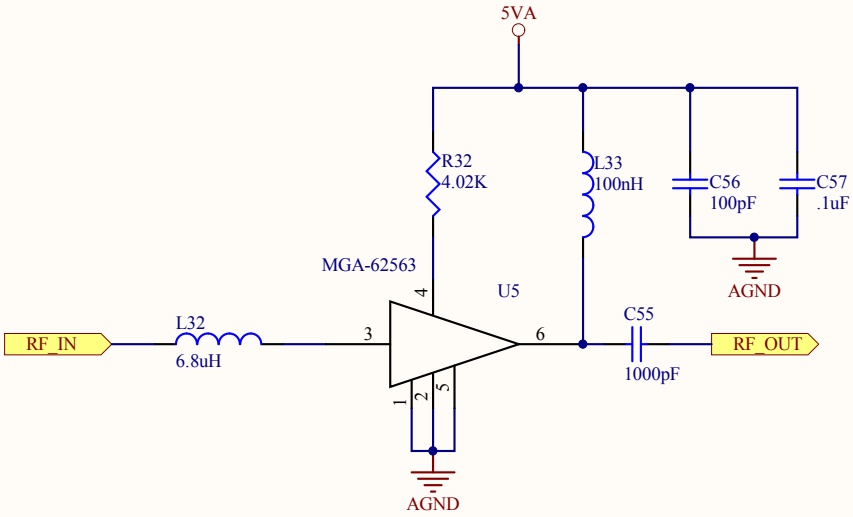
Title: **RFX400: Input Filter**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 1 of 28	
File: C:\Documents and Settings\..\rfx400-input-filter.SchDoc	Drawn By: Alexander Hackett	



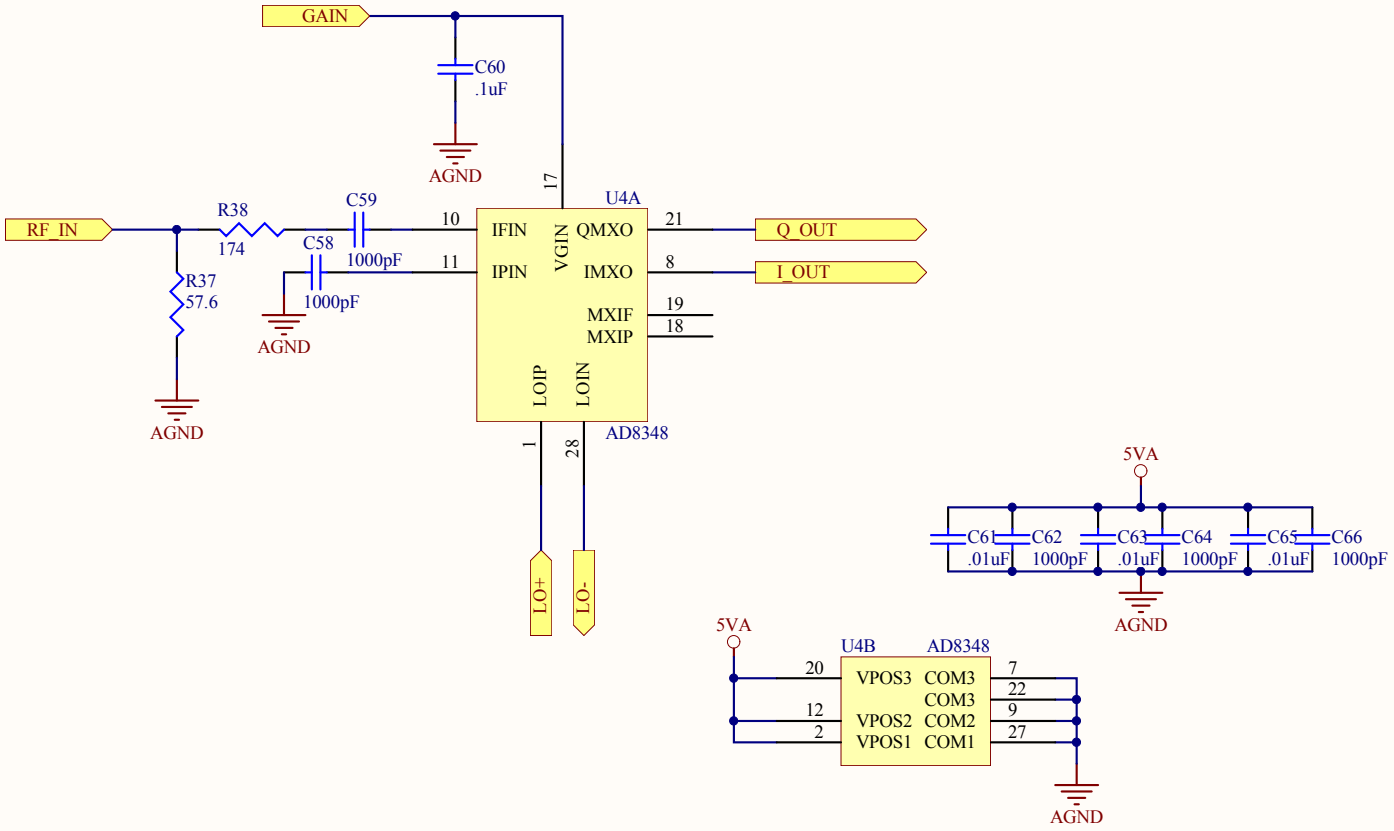
Title: **RFX400: Output Amplifier**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 12 of 28	
File: C:\Documents and Settings\..\rfx400-out-amp.SchDoc	Drawn By: Alexander Hackett	



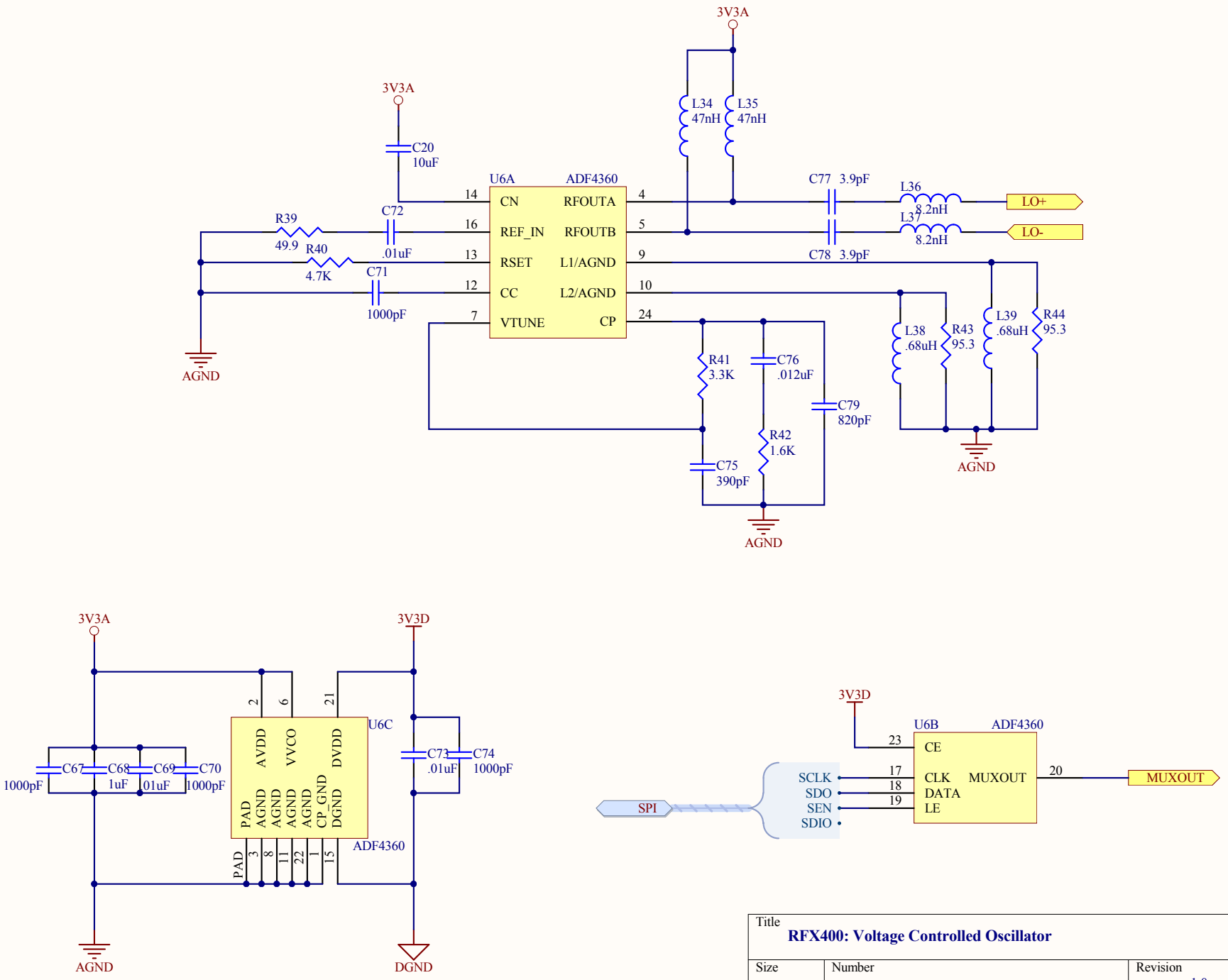
Title: **RFX400: Output Filter**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 13 of 28	
File: C:\Documents and Settings\..\rfx400-out-filter.SchDoc	Drawn By: Alexander Hackett	



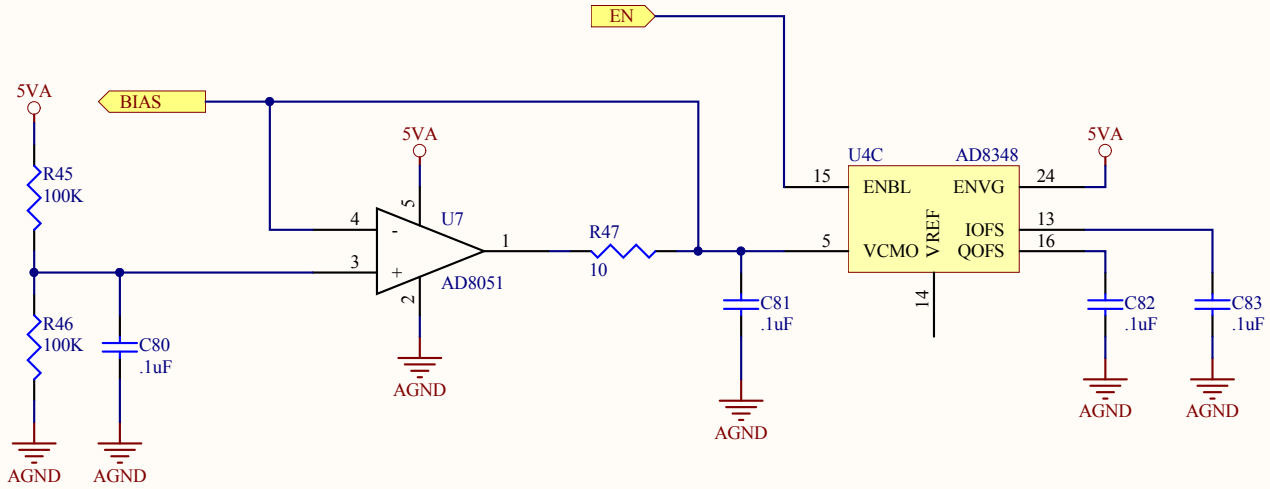
Title	**RFX400: Preamplifier**		
Size: A	Number:		Revision: 1.0
Date:	4/9/2011	Sheet 14 of 28	
File:	C:\Documents and Settings\..\rfx400-preamp.SchDoc	Drawn By:	Alexander Hackett



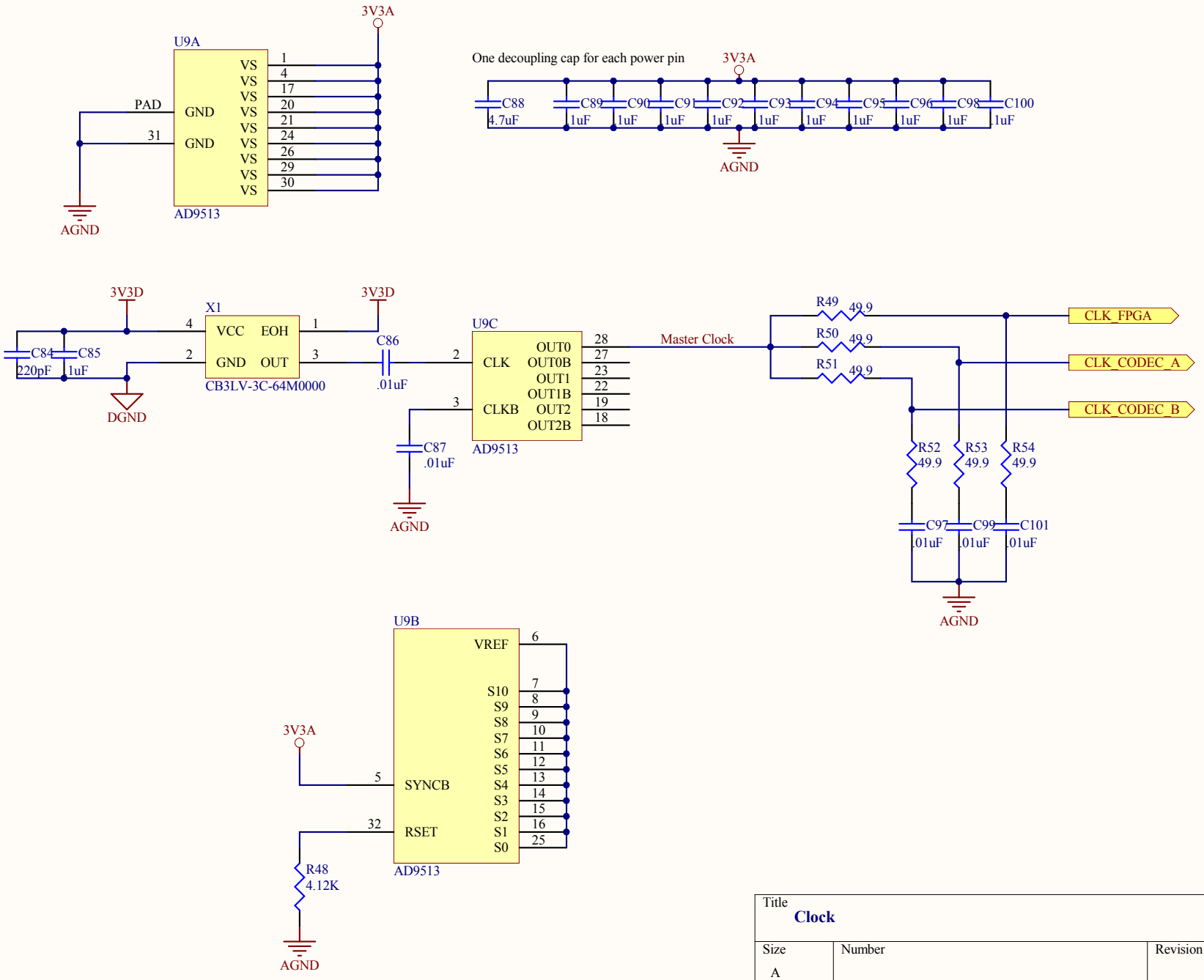
Title: **RFX400: Quadrature Demodulator**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 15 of 28	
File: C:\Documents and Settings\..\rfx400-quad-demod.SchDoc	Drawn By: Alexander Hackett	



Title	**RFX400: Voltage Controlled Oscillator**	
Size: A	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 16 of 28	
File: C:\Documents and Settings\..\rfx400-VCO.SchDoc	Drawn By: Alexander Hackett	



Title: **RFX400: Voltage Reference**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 17 of 28	
File: C:\Documents and Settings\..\rfx400-Vref.SchDoc	Drawn By: Alexander Hackett	



Title: **Clock**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011		Sheet 18 of 28
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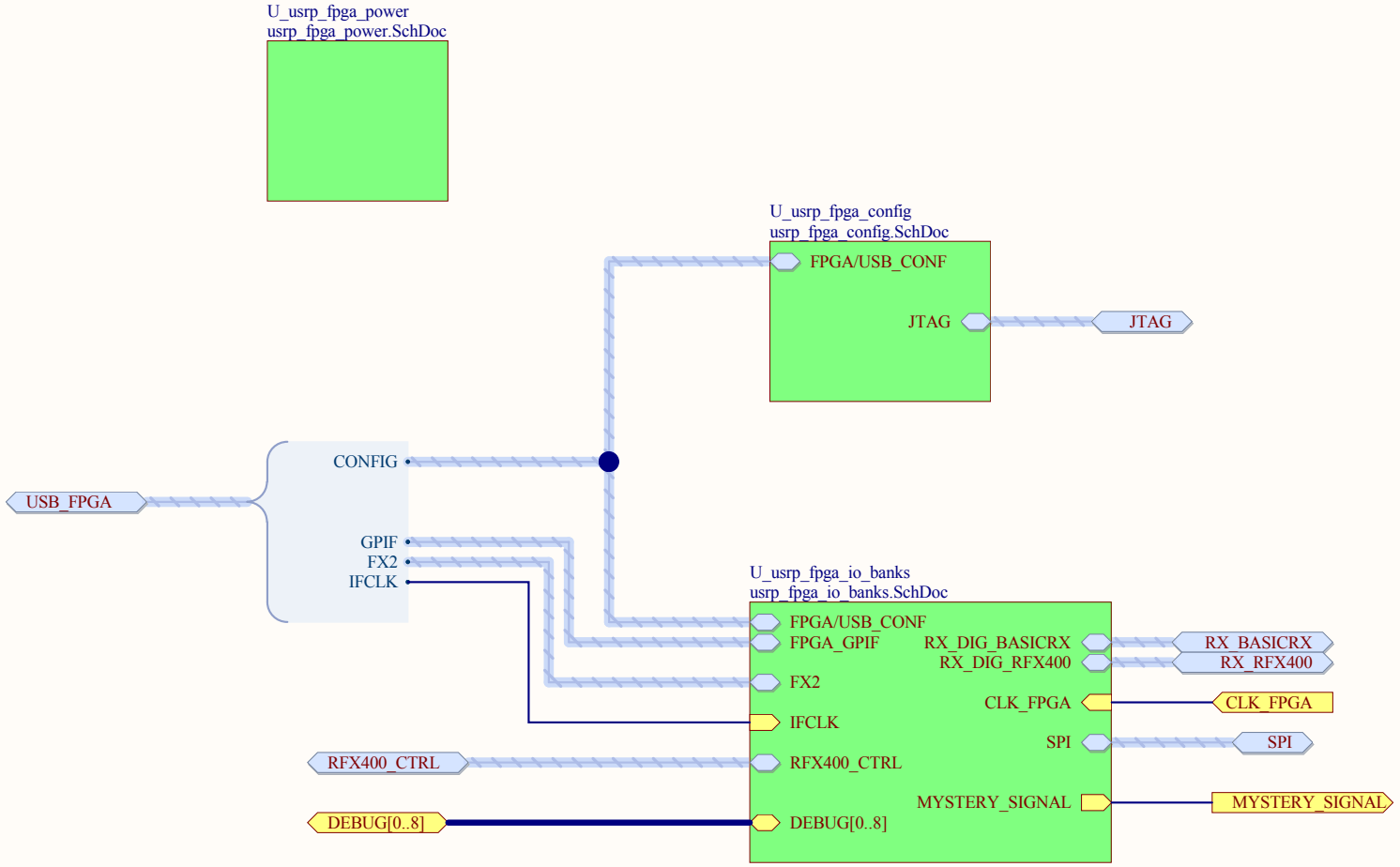

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Size A	Number	Revision 1.0
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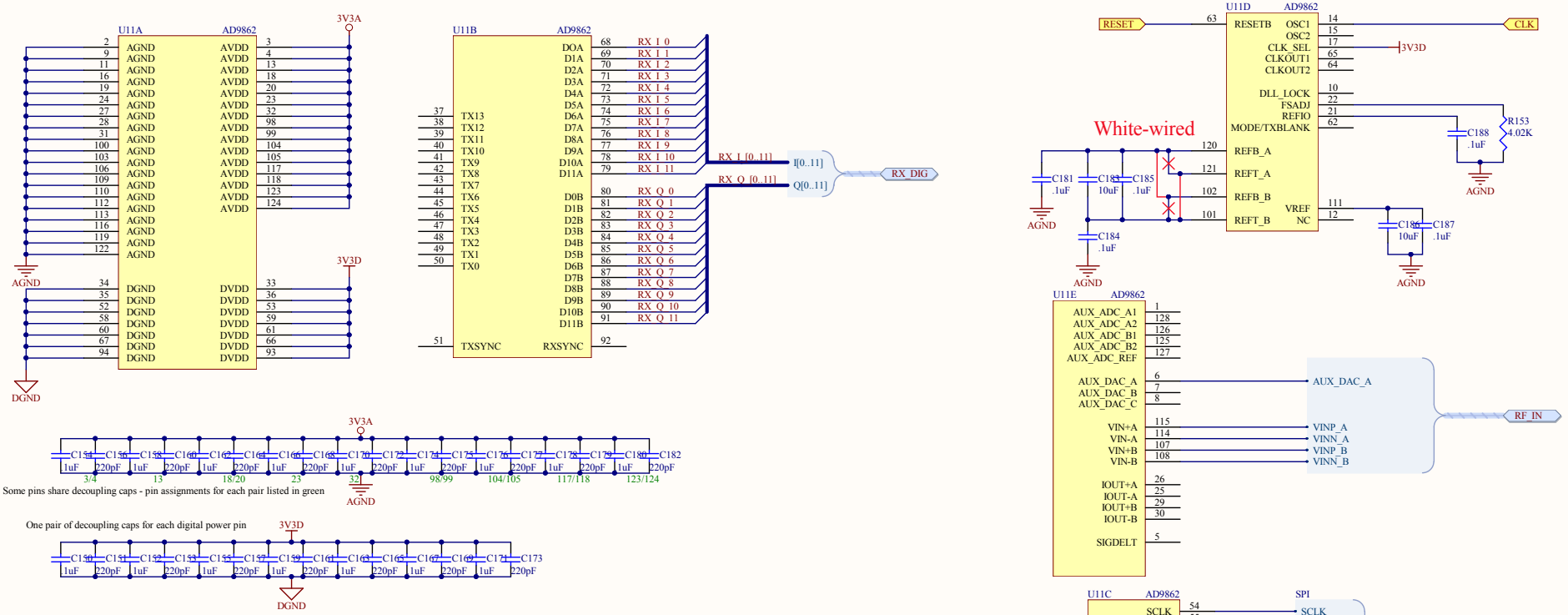
File: C:\Documents and Settings\..\usrp_fpga.SchDoc	Drawn By: Alexander Hackett	



Title	**Mixed Signal Frontend**	
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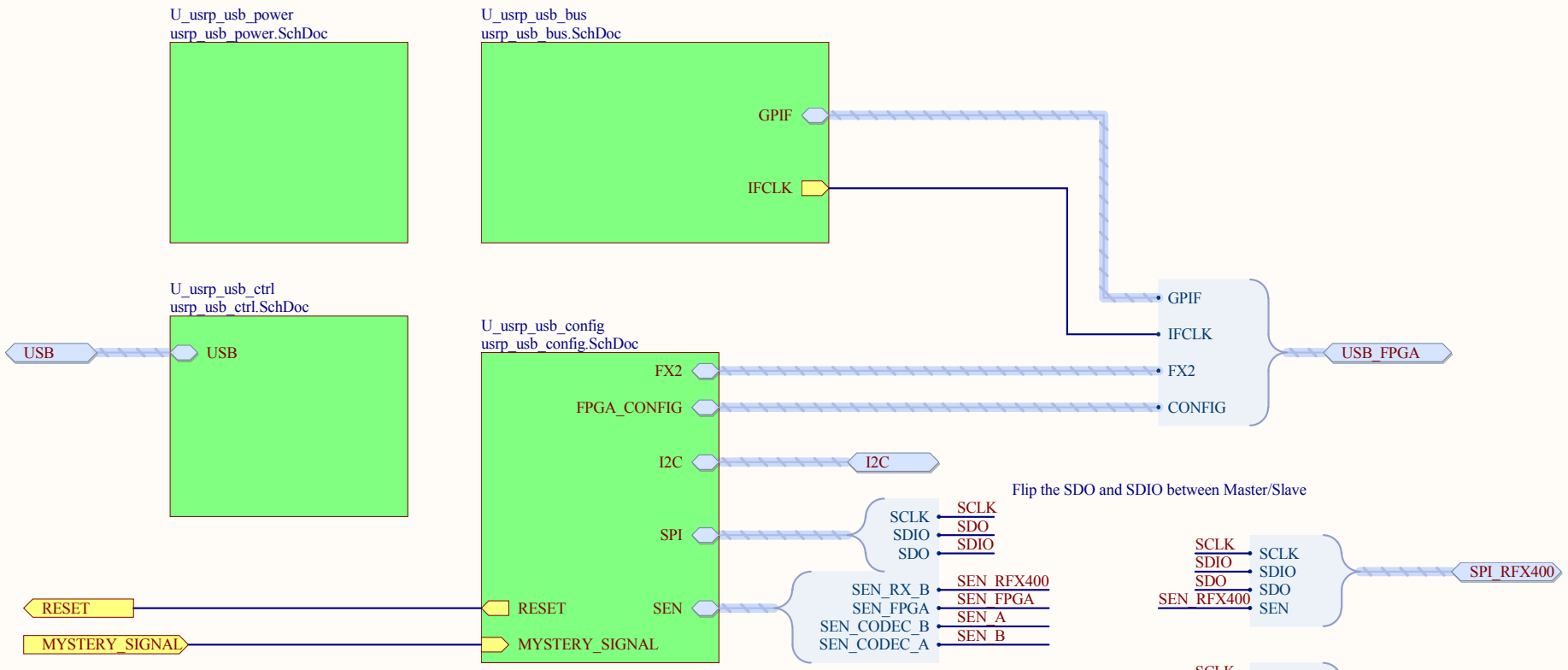
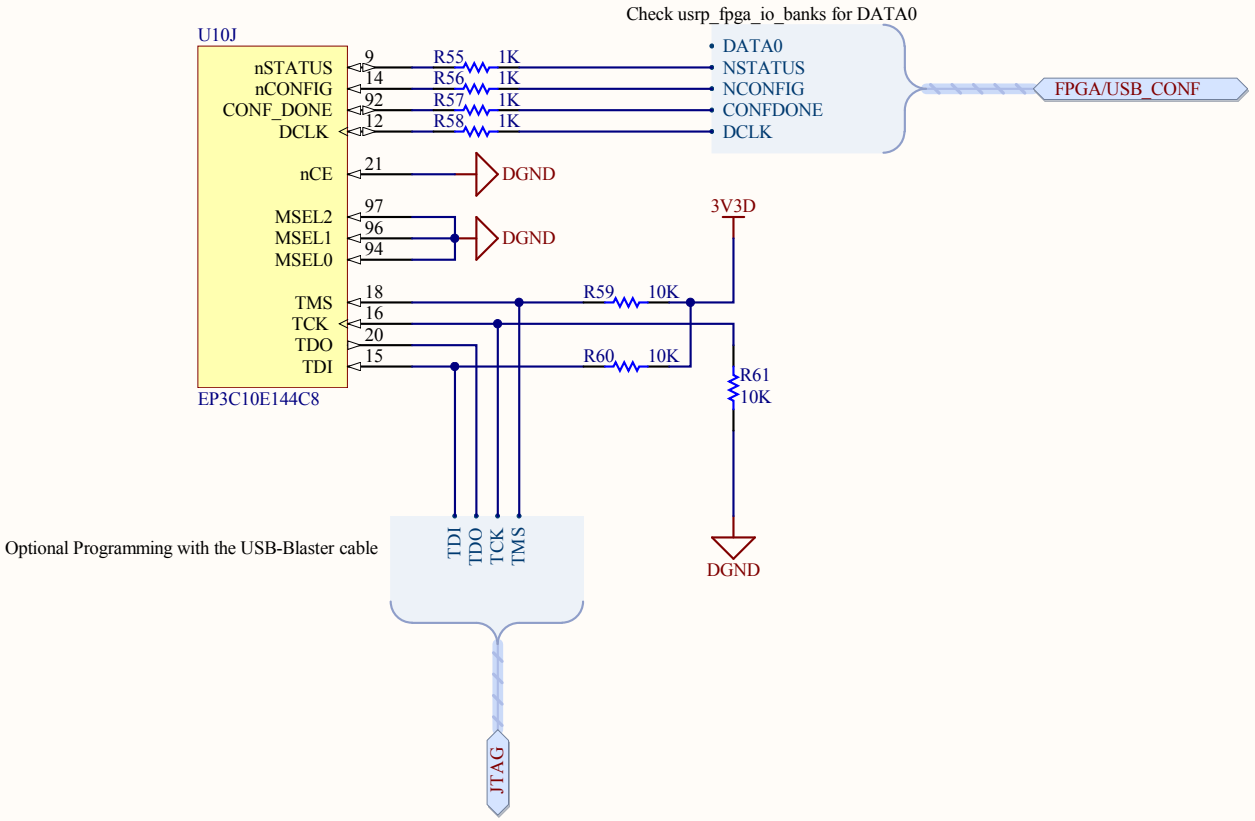
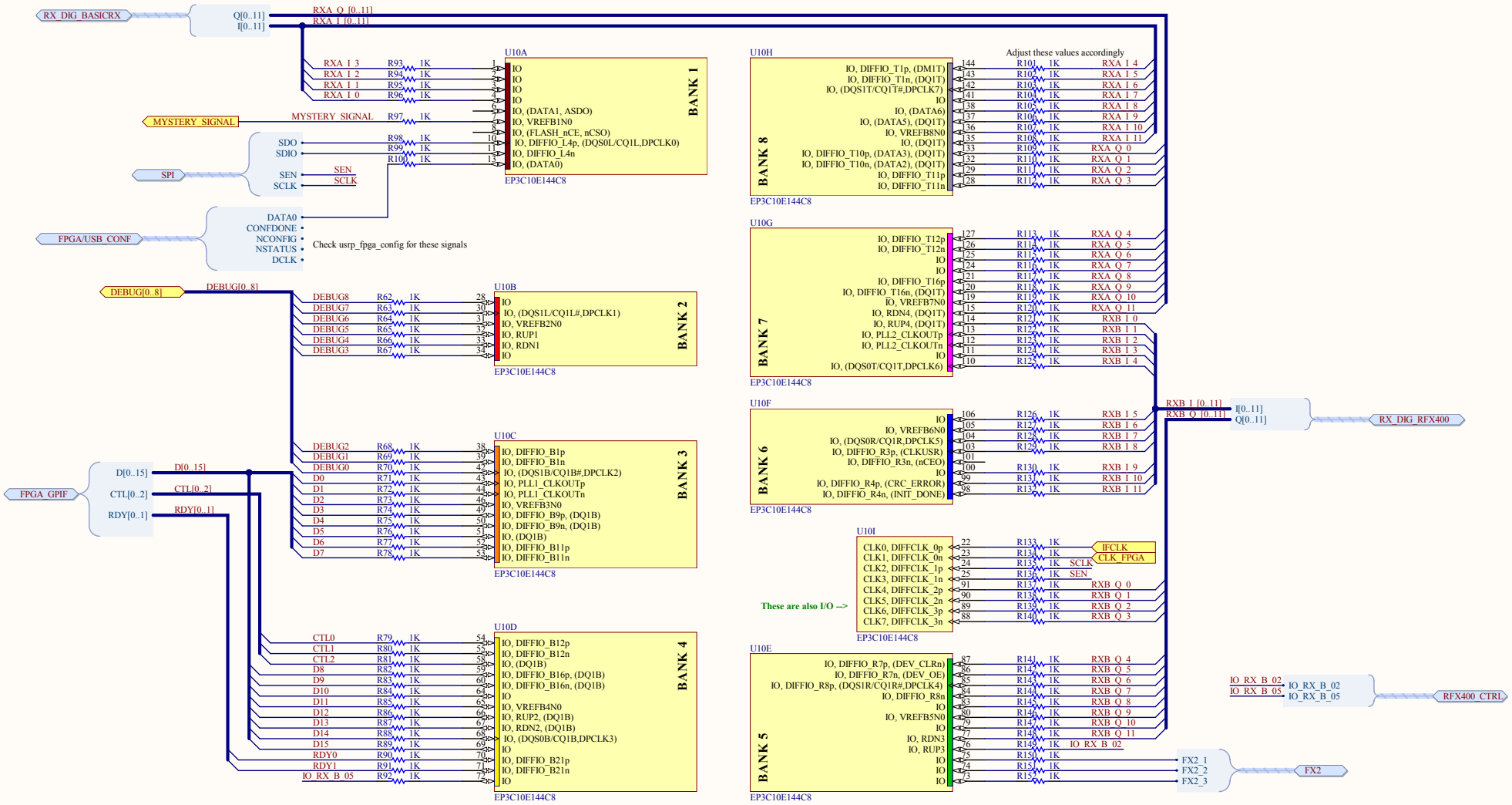
Date: 4/9/2011	Sheet 20 of 28	
File: C:\Documents and Settings\...\usrp_mixed_frontend.SchDoc	Drawn By: Alexander Hackett	



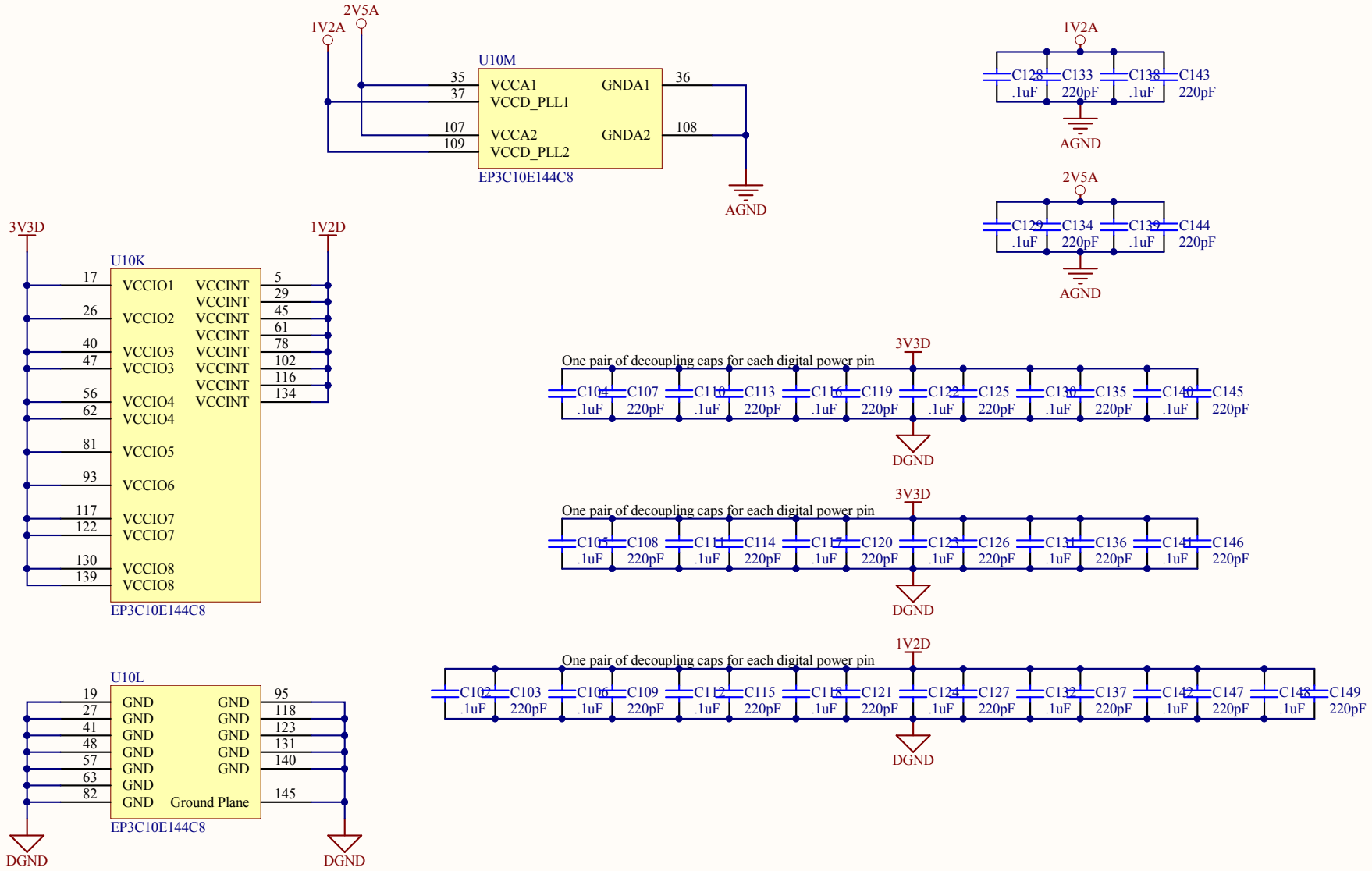
Title: **USB**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011		Sheet 2 of 28
File: C:\Documents and Settings\..\usrp_usb.SchDoc		Drawn By: Alexander Hackett

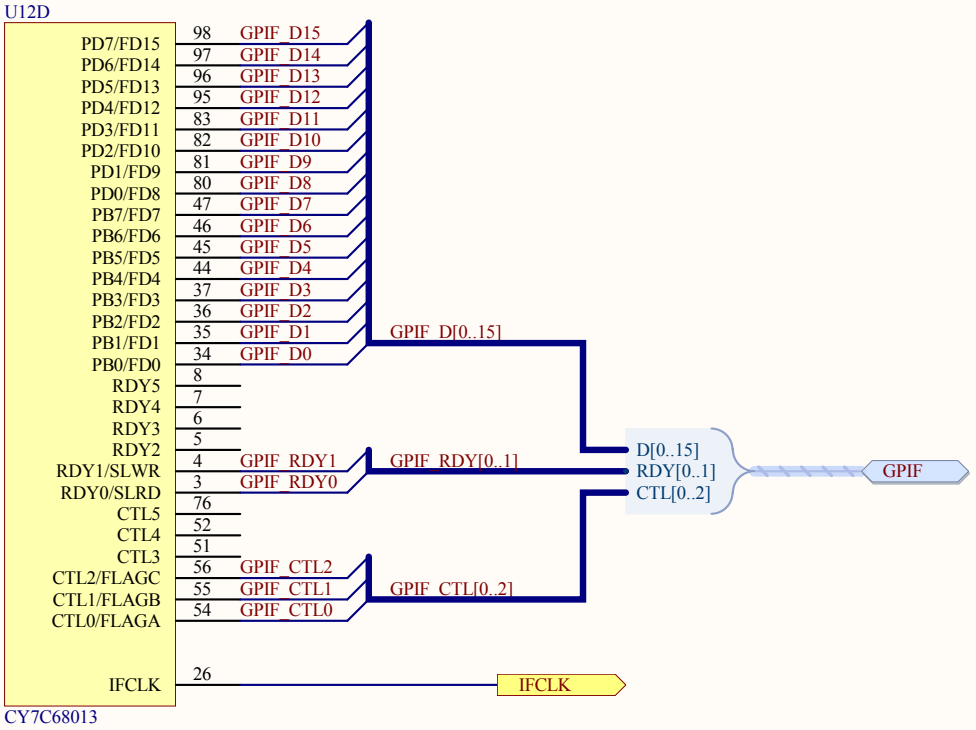


Title: **FPGA Configuration**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 2 of 28	
File: C:\Documents and Settings\..\usrp_fpga_configSch.Dsn	Drawn By: Alexander Hackett	

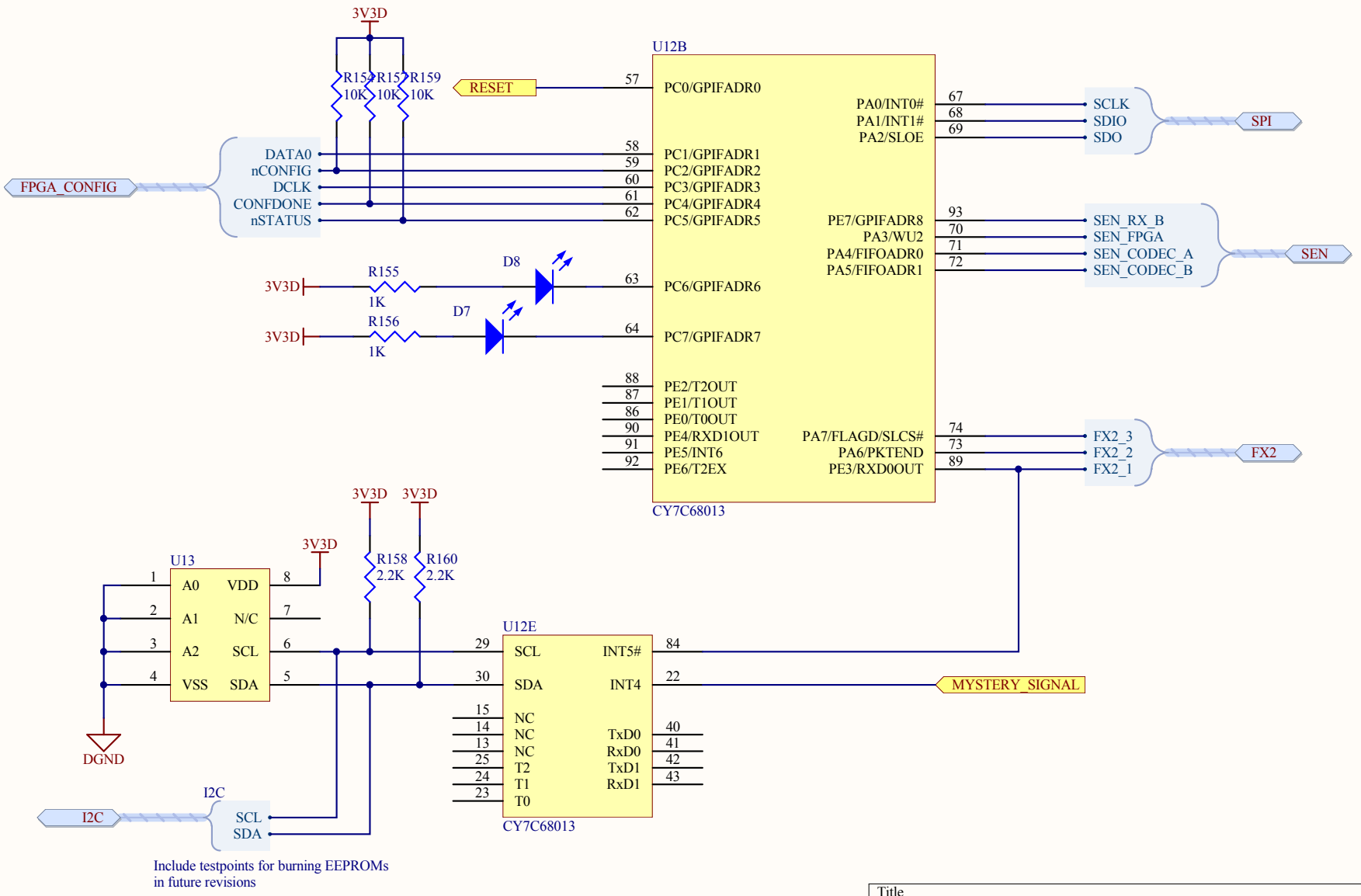


Title	FPGA I/O	
Size: B	Number	Revision: 1.0
Date: 4/9/2011	Sheet 2 of 28	
File: C:\Documents and Settings\...\usrp_fpga_io.SchDoc	Drawn By: Alexander Hackett	

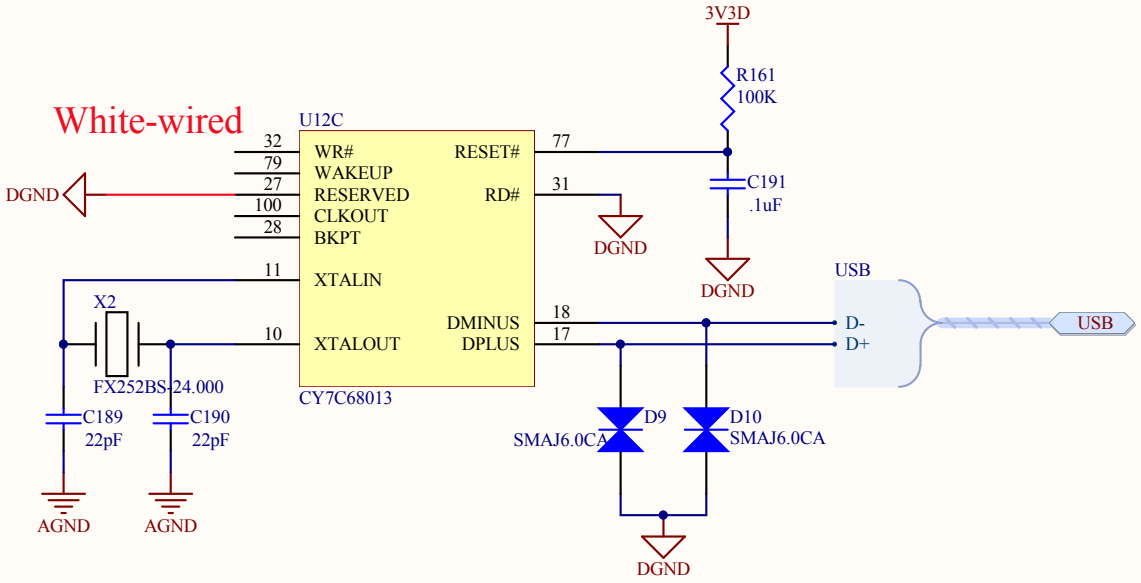

2V5A
1V2A
U10M
35
37
107
109
VCCA1
VCCD_PLL1
VCCA2
VCCD_PLL2
GNDA1
GNDA2
36
108
EP3C10E144C8
AGND
1V2A
C128 .1uF
C133 220pF
C138 .1uF
C143 220pF
AGND
2V5A
C129 .1uF
C134 220pF
C139 .1uF
C144 220pF
AGND
3V3D
1V2D
U10K
17
26
40
47
56
62
81
93
117
122
130
139
VCCIO1
VCCIO2
VCCIO3
VCCIO3
VCCIO4
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO7
VCCIO8
VCCIO8
VCCINT
5
29
45
61
78
102
116
134
EP3C10E144C8
One pair of decoupling caps for each digital power pin
3V3D
C104 .1uF
C107 220pF
C110 .1uF
C113 220pF
C116 .1uF
C119 220pF
C122 .1uF
C125 220pF
C130 .1uF
C135 220pF
C140 .1uF
C145 220pF
DGND
One pair of decoupling caps for each digital power pin
3V3D
C105 .1uF
C108 220pF
C111 .1uF
C114 220pF
C117 .1uF
C120 220pF
C123 .1uF
C126 220pF
C131 .1uF
C136 220pF
C141 .1uF
C146 220pF
DGND
One pair of decoupling caps for each digital power pin
1V2D
C102 .1uF
C103 220pF
C106 .1uF
C109 220pF
C112 .1uF
C115 220pF
C118 .1uF
C121 220pF
C124 .1uF
C127 220pF
C132 .1uF
C137 220pF
C142 .1uF
C147 220pF
C148 .1uF
C149 220pF
DGND
U10L
19
27
41
48
57
63
82
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
Ground Plane
95
118
123
131
140
145
EP3C10E144C8
DGND
DGND
Title
FPGA Power
Size
A
Number
Revision
1.0
Date:
4/9/2011
Sheet 24 of 28
File:
C:\Documents and Settings\..\usrp_fpga_power.SchDoc
Drawn By:
Alexander Hackett



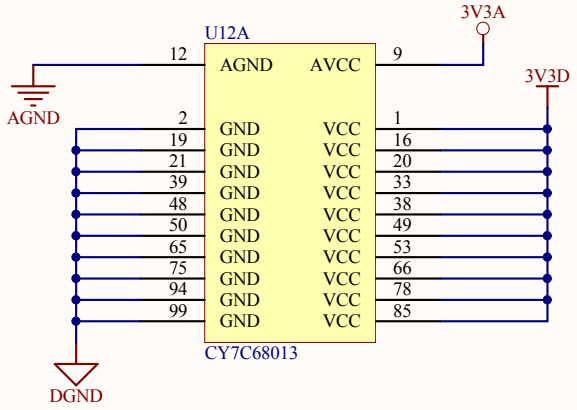
Title: **USB Signals**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 25 of 28	
File: C:\Documents and Settings\..\usrp_usb_bus.SchDoc	Drawn By: Alexander Hackett	



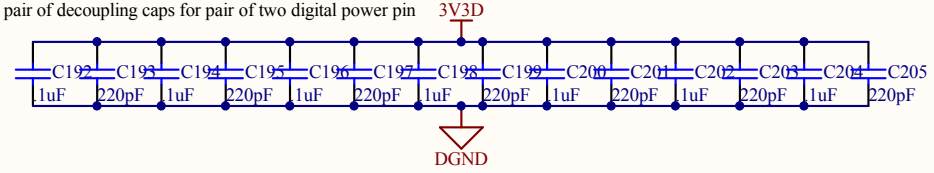
Title: **USB Configuration**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 26 of 28	
File: C:\Documents and Settings\..\usrp_usb_config.SchDoc	Drawn By: Alexander Hackett	

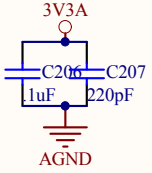


Title: **USB Control**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011		Sheet 27 of 28
File: C:\Documents and Settings\..\usrp_usb_ctrl.SchDoc		Drawn By: Alexander Hackett



One pair of decoupling caps for pair of two digital power pin





Title: **USB Power**		
Size: A	Number:	Revision: 1.0
Date: 4/9/2011	Sheet 28 of 28	
File: C:\Documents and Settings\..\usrp_usb_power.SchDoc	Drawn By: Alexander Hackett	

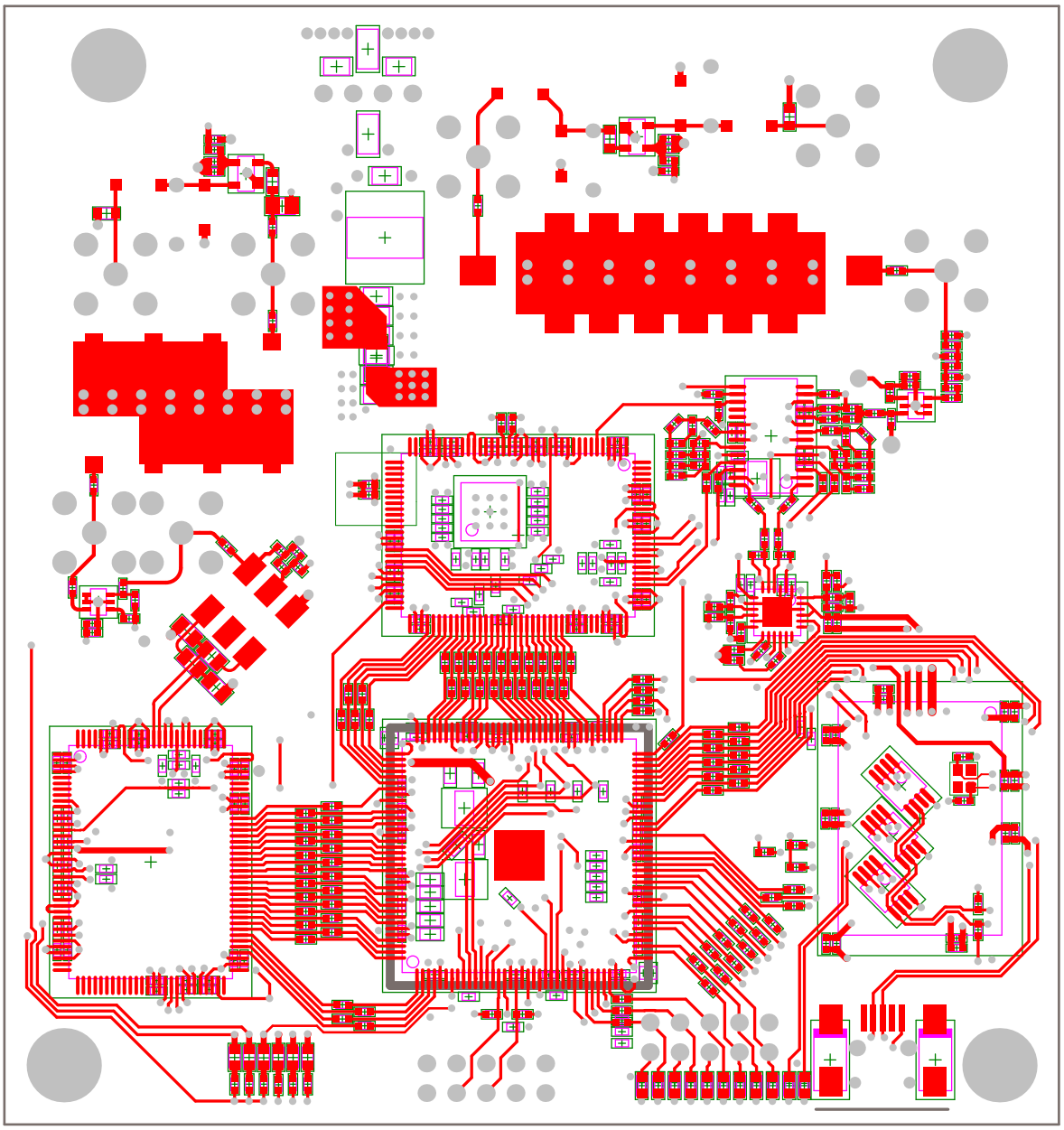
Appendix C

Printed Circuit Board Layout Design

The following plots illustrate the layout and artwork design developed for the PGRBR PCB. In all plots, mechanical layers are shown in green and magenta, and drill holes are shown in gray. These plots were generated using Altium Designer 9.

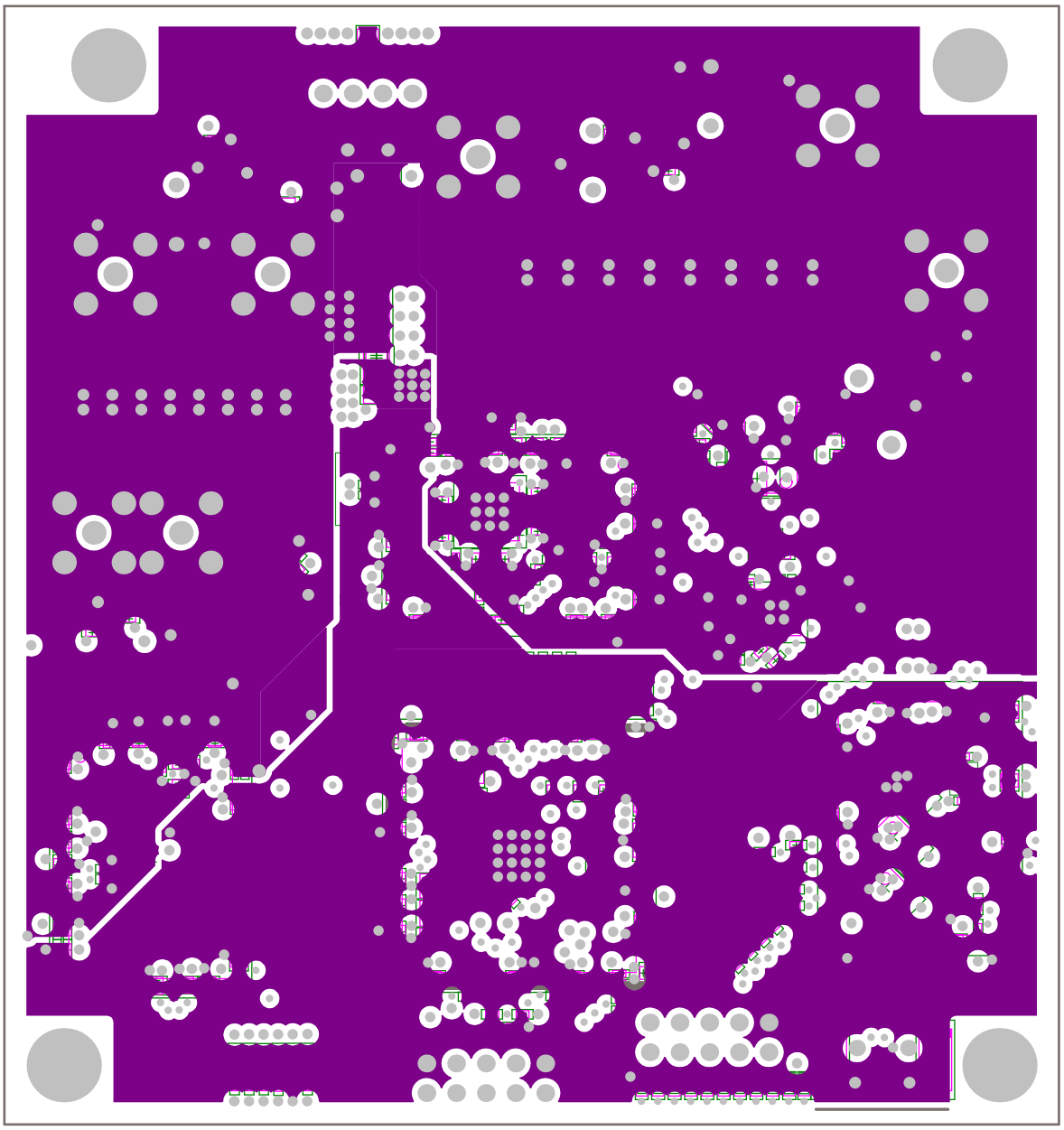
C.1 Top Layer

Copper shown in red.



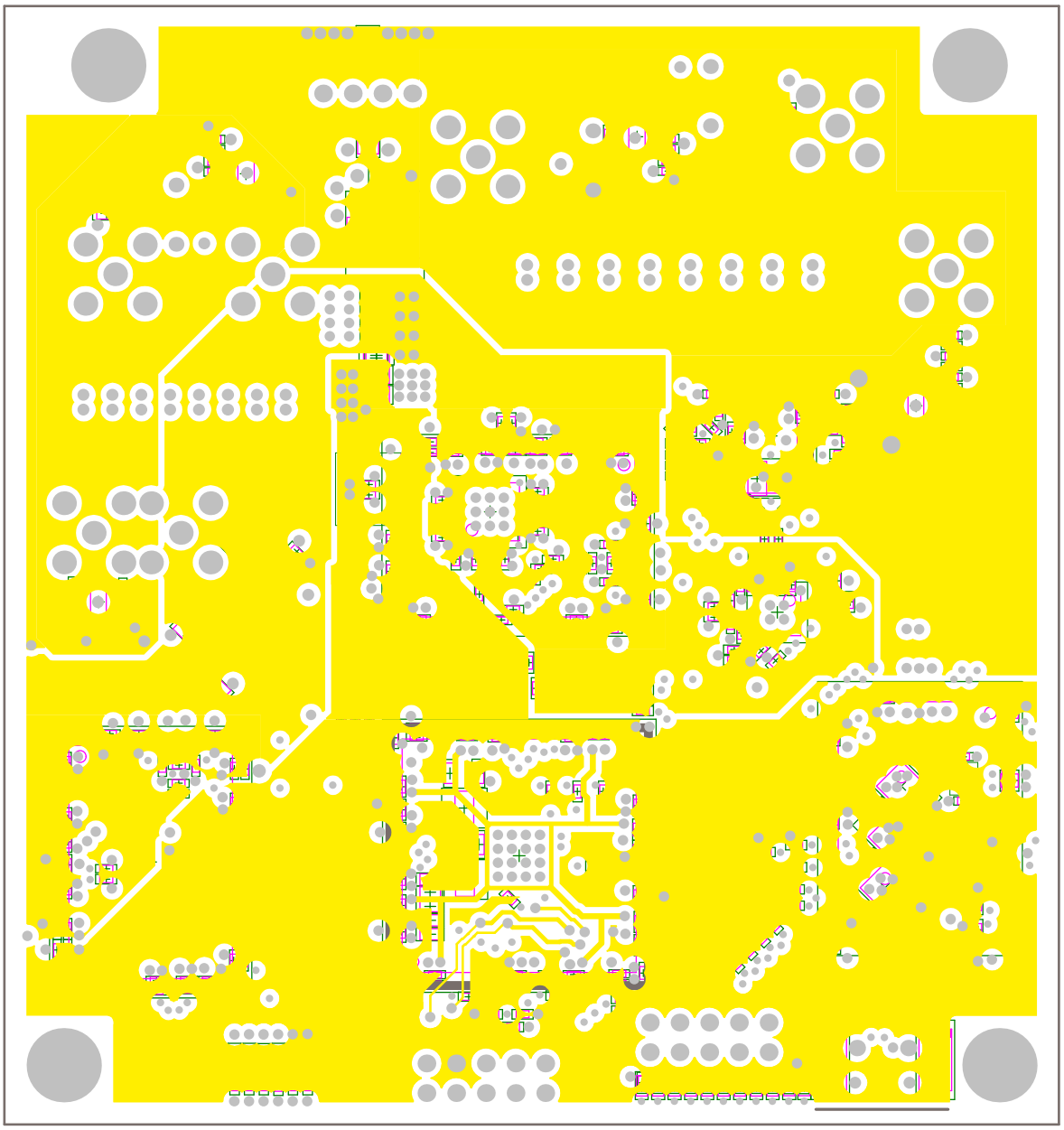
C.2 Ground Plane (Inner Layer)

Copper shown in purple.



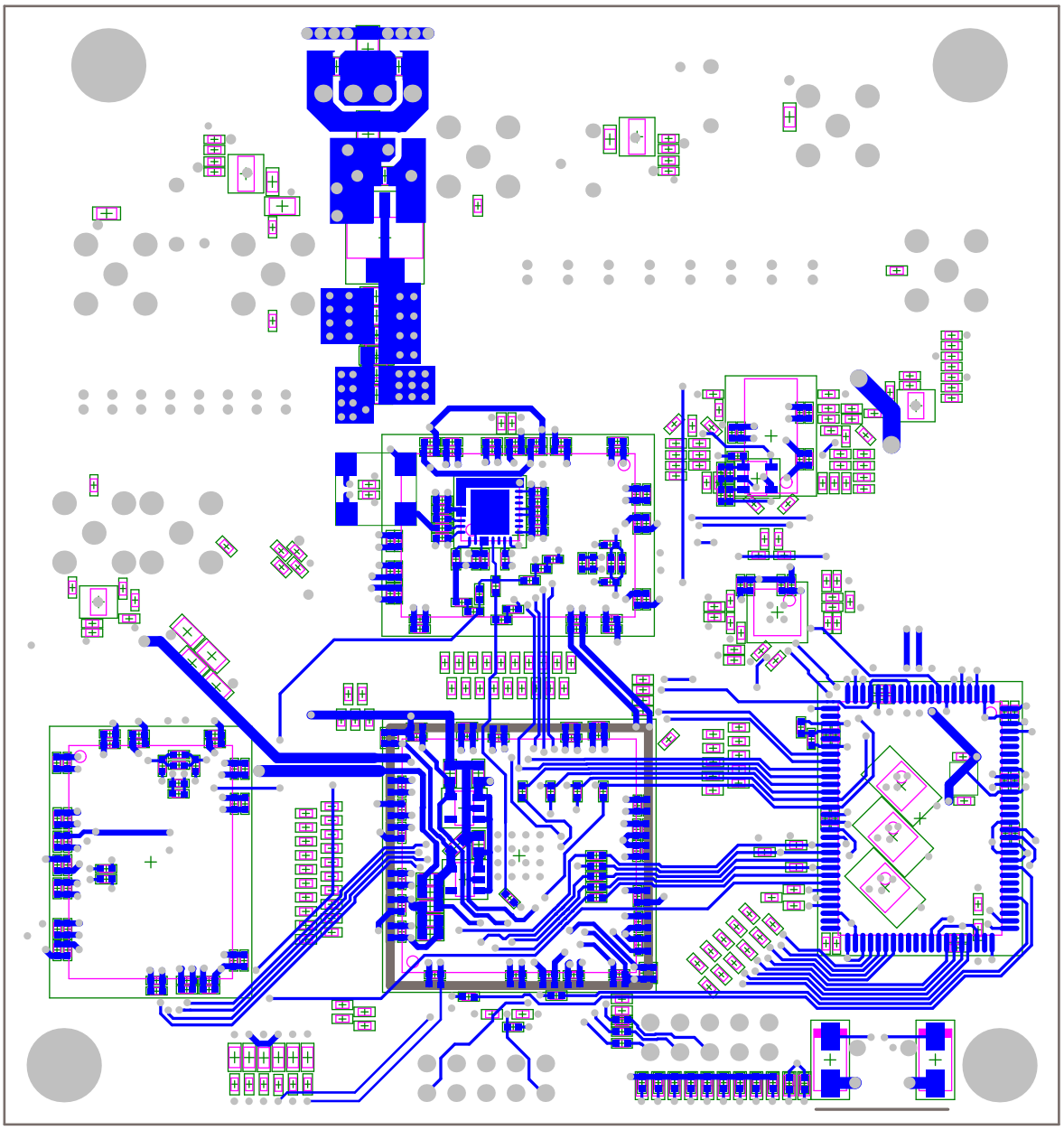
C.3 Power Plane (Inner Layer)

Copper shown in yellow.



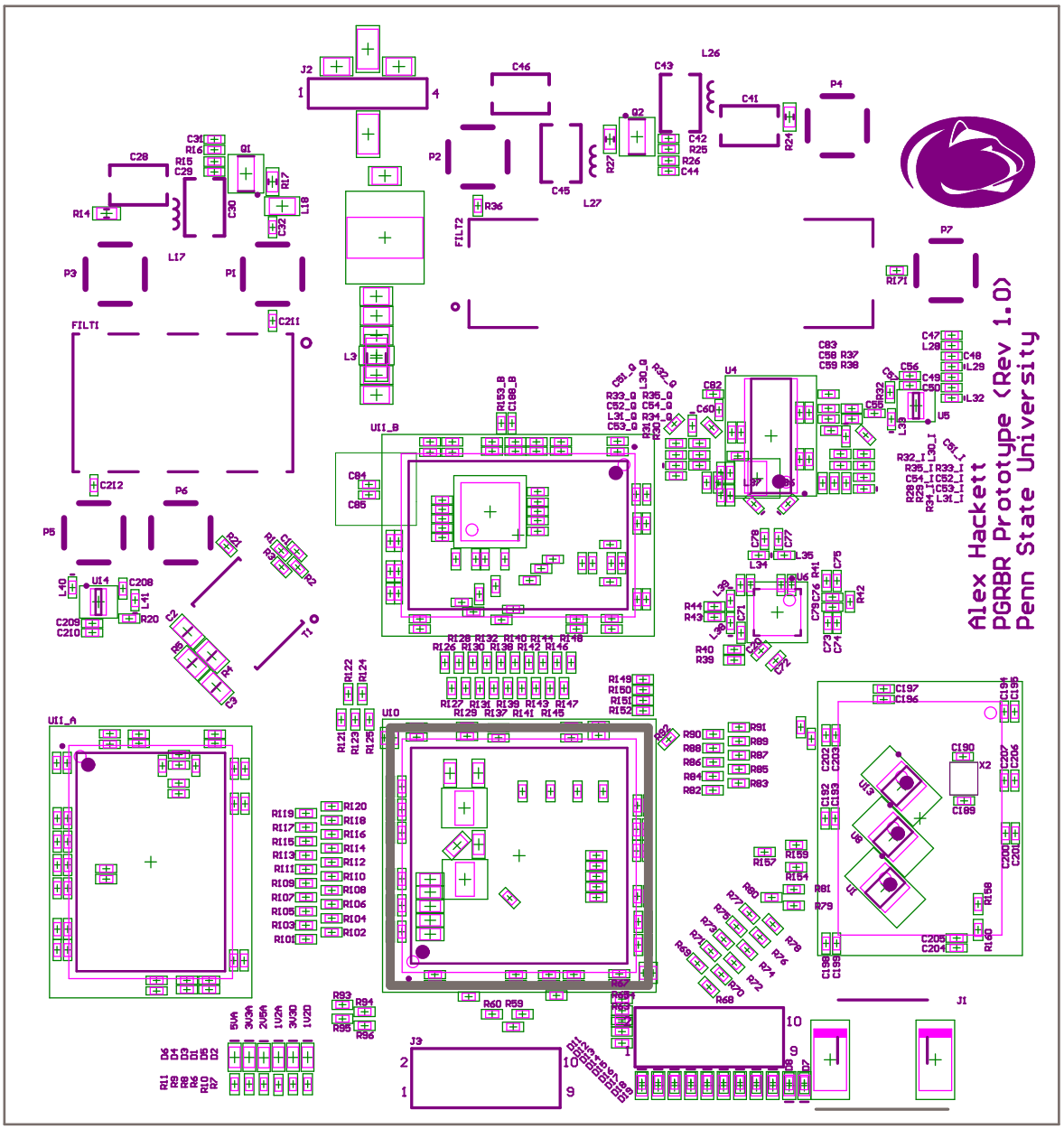
C.4 Bottom Layer

Copper shown in blue.



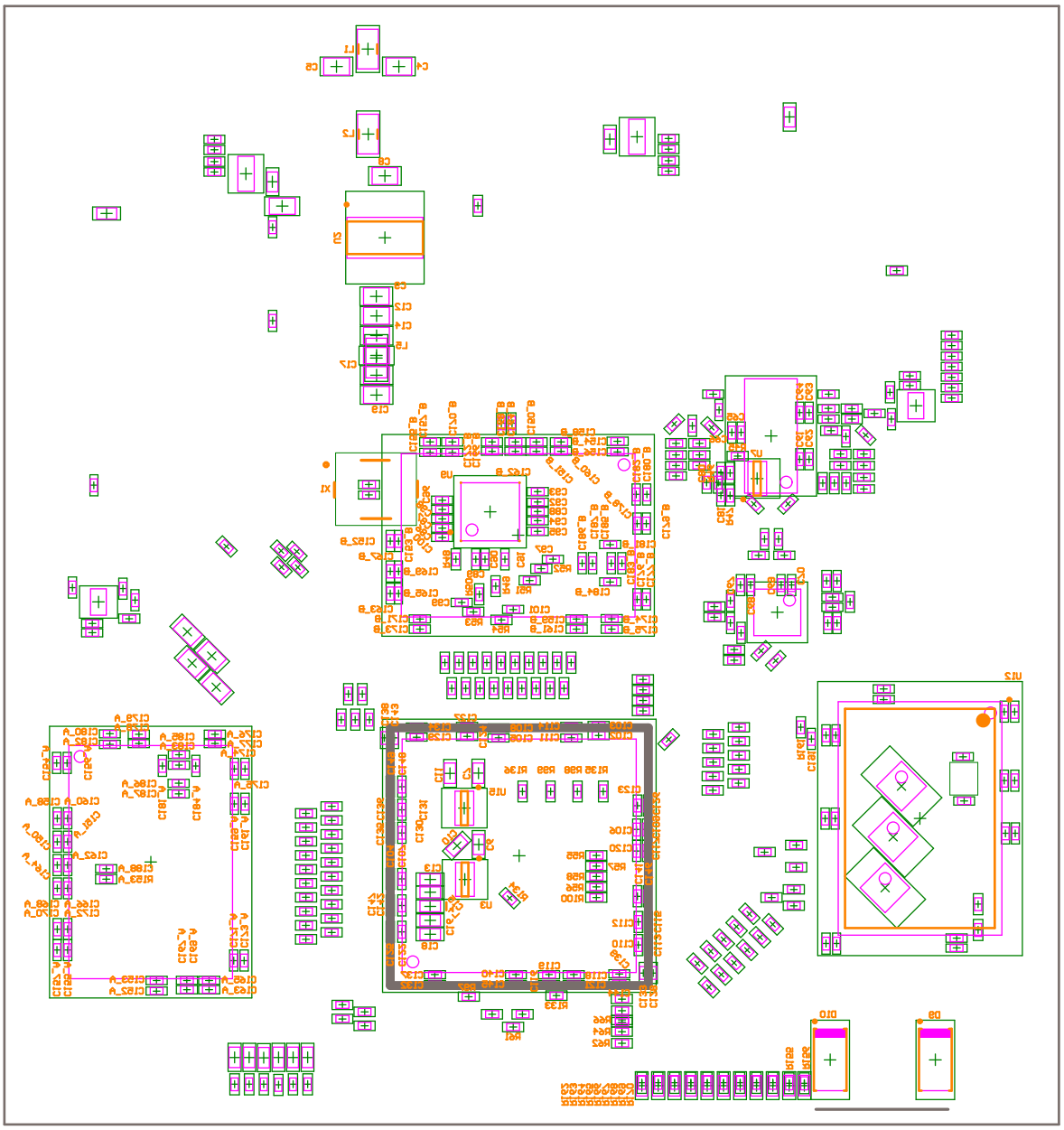
C.5 Top Silkscreen Layer

Silkscreen shown in purple.



C.6 Bottom Silkscreen Layer

Silkscreen shown in orange.



Appendix D

Preliminary Procedures

D.1 EEPROM

The EEPROM devices on board the USRP contain an initial configuration for the USB microcontroller to appear as a USRP device to the GPC.

Prior to the first use of the PGRBR, the EEPROM devices must be configured appropriately. One method of burning these devices is by using an existing USRP to both supply and burn the EEPROM data to the PGRBR. The following procedure outlines the process to initialize the EEPROM devices on the PGRBR.

D.1.1 Materials

The following materials are needed to complete the procedure:

- USRP motherboard, power supply, and USB cable
- BasicRX or BasicTX daughterboard
- PGRBR PCB, power supply, and USB cable
- GPC running Linux with Python and GNU Radio installed
- Three jumper wires (solderless)

D.1.2 Procedure

1. Power on the USRP with BasicRX or BasicTX daughterboard.
2. Jumper wire the I^2C breakout pins (SDA, SCK, GND) on the daughterboard to the respective nodes on the PGRBR PCB.
3. Power on the PGRBR PCB.
4. Connect the USRP to the GPC via USB.
5. Open the Python interactive shell ("python" from a terminal command line).
6. Run the following commands in the Python shell (>>> indicates the Python prompt).

```
>>> from gnuradio import usrp
>>> u = usrp.source_c(0)
>>> s = u.read_eeprom(80, 0, 2048)
>>> u.write_eeprom(80, 0, s)
```

7. Exit the Python shell.
8. Unplug the USB connection between the USRP and the GPC.
9. Power off both the USRP and the PGRBR PCB.
10. Power on the PGRBR PCB.
11. Connect the PGRBR PCB to the GPC via USB.
12. From a terminal command line, run `lsusb`. One of the devices listed will have a device ID of `fffe:0002` – this is the PGRBR PCB and it indicates that procedure was successful. The second light-emitting diode (LED) left of the USB connector will also blink at a rate of about 3 Hz.

D.2 Firmware & FPGA Bitstream

When powered on, the FPGA on the USRP starts uninitialized, and the USB microcontroller starts with a minimal configuration (provided by the EEPROM) to communicate with the GPC. When starting a software radio flowgraph in GNU Radio, the appropriate USB firmware and FPGA bitstream are automatically loaded from the GPC via USB, as a feature of the GNU Radio run-time interface. In some cases, it may be desired or necessary

to load the USB microcontroller firmware and FPGA bitstream manually. Fortunately, GNU Radio provides a standalone tool, called `usrper`, that allows manual configuration. The following procedure outlines the process of downloading the USB microcontroller firmware and configuring the FPGA manually.

D.2.1 Materials

The following materials are needed to complete the procedure:

- PGRBR PCB, power supply, and USB cable
- GPC running Linux with GNU Radio installed

D.2.2 Procedure

1. If this is the first time the PGRBR is connected, the EEPROM devices must be configured, as described in Section D.1.
2. Copy the PGRBR FPGA bitstream file (`pgrbr.rbf`) from the PGRBR project file directory to `/usr/local/share/usrp/rev4/`. Depending on the GPC system configuration, root privileges may be necessary. Note: this step only needs to be completed once per GPC.
3. Power on the PGRBR PCB.
4. Connect the PGRBR PCB to the GPC via USB.
5. From a terminal command line, run the following commands ($ indicates the terminal prompt):

   ```
   $ usrper load_firmware /usr/local/share/usrp/rev4/std.ihx
   $ usrper load_fpga /usr/local/share/usrp/rev4/pgrbr.rbf
   ```

   If successful, a three-LED "bar" will be "sliding" across the LED bank.

Alexander L. Hackett

Academic Vita

Education & Honors

- B.S. in Electrical Engineering, Pennsylvania State University (*May 2011*)
  - Schreyer Honors Scholar (*Aug. 2007 – May 2011*)
  - Leonhard Engineering Honors Scholar (*Aug. 2007 – May 2011*)
- M.S. in Electrical Engineering, Pennsylvania State University (*beginning Aug. 2011*)

Honors Thesis

- **An Open-Source Beacon Receiver for CubeSat Missions** - Adapting the GNU Radio Beacon Receiver for satellite and sounding rocket use (*Jan 2010 – Apr. 2011*)

Employment

- NASA Goddard Space Flight Center (*June 2010 – Aug. 2010*)
  - Developed and tested high-speed signal distortion models for TDRS communications simulator
  - Analyzed non-ideal performance of a COTS RF Wireless link system
- Cornell University @ Arecibo Observatory (*May 2009 – Aug. 2009*)
  - Completed design for, implemented, and tested an FPGA-based radar controller
- Pennsylvania State University (*May 2008 – May 2011*)
  - Undergraduate research with FPGAs, Software-Defined Radio, Radar systems, and radio devices
  - Teaching assistant for Electrical Engineering First-Year Seminar

Projects

- Student Space Programs Laboratory (SSPL)
  - **Power Subsystem Lead** (*Aug. 2010 – May 2011*)
  - OSIRIS Cubesat (*Aug. 2009 – May 2011*)
    - Developed battery profiling software
  - OLITE Long Duration Balloon (*Jan. 2009 – May 2011*)
    - Designed and tested power regulation system
    - Designed flight computer PCB
  - Cansat Competition (*Sept. 2008 – June 2009*)
    - Project Manager, designed/tested power regulation system
  - USERS Sounding Rocket (*Feb. 2008 – Sept. 2008*)
    - Designed wiring book, constructed wiring harness, tested electrical systems
- Applied Signal Processing and Instrumentation Research Laboratory (ASPIRL)
  - Constructed various radar arrays in Bermuda, University of Illinois, and Penn State University
  - FPGA research on the Xilinx Spartan 3E platform
  - Software-defined radio research using the Universal Software Radio Peripheral (USRP) and GNU Radio
- Coursework
  - *Linear Electronic Design*: Designed and constructed high-speed operational amplifier from discrete components (*Mar. 2010 – May 2010*)
  - *Introduction to Software Defined Radio*: Constructed multi-purpose software-defined transceiver system using the Universal Software Radio Peripheral (USRP) (*Nov. 2009 – Dec. 2009*)
  - *Digital Design using Field Programmable Devices*: Designing and implementing an FPGA-based electronic door lock system, utilizing a touchscreen (*Oct. 2010 – Dec. 2010*)

Areas of Interest & Research

Space Systems	Power Electronics	Analog/RF Circuit Design	PCB Layout Design
Communication Systems	Digital Circuit Design	Digital Signal Processing	Software-Defined Radio

Technical Skills

- PCB Layout Design
  - Altium Designer (*2 years*)
  - Orcad (*3 months*)
- Circuit Design (*2.5 years*)
- FPGA Architecture Design
  - Verilog (*1.5 years*)
  - VHDL (*3 months*)
- Linux Administration (*5+ years*)
- Computer Programming
  - C/C++ (*5+ years*)
  - MATLAB (*2.5 years*)
  - Python (*6 months*)

Certifications

- General Class Amateur Radio License (*Oct. 2010*)