THE PENNSYLVANIA STATE UNIVERSITY
SCHREYER HONORS COLLEGE

DEPARTMENT OF CHEMICAL ENGINEERING

IMPLEMENTING STRATEGIES TO OPTIMIZE C8-BTBT THIN-FILM TRANSISTOR PERFORMANCE

HUNTER MILLER
SPRING 2019

A thesis
submitted in partial fulfillment
of the requirements
for a baccalaureate degree
in Chemical Engineering
with honors in Chemical Engineering

Reviewed and approved* by the following:

Enrique D. Gomez
Professor of Chemical Engineering
Thesis Supervisor

Ali Borhan
Professor of Chemical Engineering
Honors Adviser

* Signatures are on file in the Schreyer Honors College.

ABSTRACT

Organic thin-film transistors are studied for their high charge mobility and low space requirement, which makes them excellent for electronics in today's society. Research demonstrates that altering variables within the fabrication process can lead to a transistor with higher or lower charge mobility. In this investigation, 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT) was applied to a silicon dioxide wafer via spin coating. Properties such as the application of a hexymethyldisilazine (HMDS) surface treatment, quench temperature, melt temperature, and quench duration, were varied throughout the process to achieve the optimal results desired.

By passing charge through the transistors via a sourcemeter, the transistor with the greatest charge mobility with an average value of 1.31 cm^2/Vs between gate voltages of -25 to -75 volts was the one with a HMDS surface treatment, melted at 110℃ for one minute, and quenched at 80℃ for three minutes. This was then analyzed optically via a UV-Vis absorbance spectrum to view shifts caused by crystallization of the small molecule. These shifts showed a correlation between optimal preparation conditions and absorbance that demonstrates that localization of electrons during crystallization.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

I would like to express my gratitude to Dr. Enrique D. Gomez, my thesis supervisor, who was instrumental in guidance, critiques, and encouragement throughout my undergraduate research. Dr. Gomez was extremely helpful in presenting me with opportunities to further my research into new fields. Additionally, I would like to thank Dr. Ali Borhan, my honors advisor, who provided me with advice throughout my studies to complete my undergraduate objectives.

Furthermore, several members of the Gomez lab team, including Brooke Kuei, Sang Yoo and Brandon Smith, were helpful in training and resources throughout my research. I would like to thank them for their efforts and time.

Lastly, I would like to thank my family and friends for their support and encouragement throughout my life. They instilled in me values that have promoted me to the position in my studies I am today.

Chapter 1

Introduction

As society progresses, the demand for advances in technology increases along with it. Each day a new electronic device is released that capitalizes on either higher performance capability, low-cost, flexibility, or all of the above. With these demands comes an opportunity to research advanced materials, such as organic thin-film transistors, in order to discover optimal performance characteristics that will yield these high performance, low-cost, and flexible devices.[3]

Specifically, organic semiconductors, such as an organic thin-film transistor, must be analyzed for their ability to provide high-charge carrier mobilities. This ability has been applied to several products today, most namely flat-panel display televisions such as the widely advertised LCD television. In such a system, the transistors are embedded in the panel, which allows for an overall improved image stability. However, other typical applications of transistors may include complementary integrated circuits and radio-frequency identification tags (RFIDs) as well.[2]

The charge carrier mobility of any given organic semiconductor is largely influenced by the molecular packing structure of the organic thin-film polymer and the crystallization of the material. Crystallization refers to the crystal alignment of the solution-processed organic thin-film transistor. In general, there are a small number of van der Waals interactions between organic molecules, such as 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT), which causes the fabrication process to be critical in regard to crystallization, ordered crystal

alignment, and thus charge mobility as a whole.[6] There are several properties that can be altered in order to produce an overall more or less efficient crystallized transistor. These properties include but are not limited to quench temperature, melt temperature, application of a hexymethyldisilazane (HMDS) surface treatment, and quench duration. However, the application of the small molecule to the transistor and the preparation of the transistor itself are also key in determining overall charge mobility. Crystallization alone can either achieve low-resistance charge conduction or allow the maximization of charge hopping within grains in the crystalline material.[1] Both promote the charge mobility overall and allow for greater performance within the transistor.

Overall, there are two instruments that can be utilized to achieve crystallization of the organic thin-film. The first of which is via a hot plate annealing process. This would involve melting the transistor for a duration before quenching and reforming/realigning the crystals within the small molecule. The second tool used is a zone annealing apparatus in which the transistor is placed beneath a heated line at the melt temperature of the given polymer and passed underneath the line at a given rate. This setup involves cooling blocks for the base of the transistor and a certain gap at the heated wire between the cooling blocks for proper crystallization of the transistor.

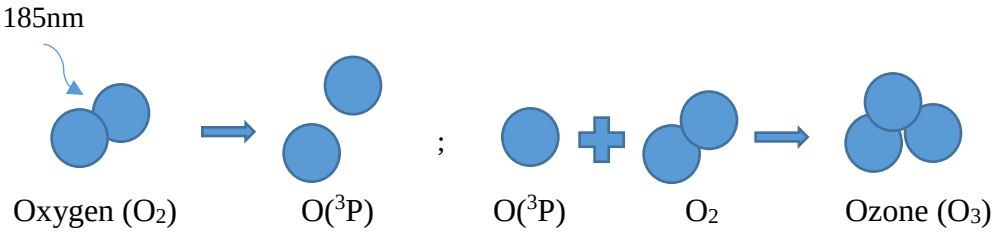
This heating/crystallization process overall allows electrons to be more localized within the molecule. This localization allows for easy passage or transfer of charge throughout the transistor. This is what promotes the overall charge mobility of the substrates. Therefore, it is also critical to view how the substrate is affected after crystallization via a UV-Vis absorbance spectrum. This is crucial in observing key absorbance peak shifts after crystallization occurs.

Furthermore, choosing the right melt and quench temperatures are key aspects of the transistor creation process. By annealing semiconductors above the melting point, it allows for enhanced alignment in the active layer, which lead to a device with an overall greater mobility. However, it is key not to surpass the melting point by a large amount as this can lead to degradation of the small molecule, which will restrict the transistor from transmitting charge if the temperature becomes too great at any point. This also applies to the duration of the melt. Applying the melt step for too long could also lead to a poor transistor. Furthermore, by utilizing a quench after the melt it allows for a degree of local order enhancement within the thin-film. This allows for greater control of crystallization, which allows for a better transistor.

As mentioned previously, the hexamethyldisilazane surface treatment is also a key part of the fabrication process. For this research, gold electrodes were printed on silicon dioxide wafers with highly doped silicon located on the bottom utilized as the gate electrode. These were used as the substrate to which C8-BTBT would be applied. Therefore, in order to enhance crystallization, the surface treatment is necessary. HMDS forms monolayers on the silicon dioxide surface during the spin coating process. The alkane chains within the C8-BTBT allow for the silicon dioxide dielectric layer to change from hydrophilic to hydrophobic character. Typically, inorganic oxide surfaces such as silicon dioxide exhibit hydrophilic states. On the other hand, organic semiconductors, such as C8-BTBT, typically exhibit hydrophobic states. This negatively impacts the crystallization of the thin-film. The surfaces are less reactive with each other than they could be. The surface treatment solves this problem and thus increases crystallinity and overall charge carrier mobility. This also yields an overall smaller value for surface free energy and a larger value for contact angle.[4] However, in order to still allow contact between the silicone dioxide wafer and the organic semiconductor, the HMDS must be applied at

extremely thin levels. This requires a high rpm value when spin coating on or around 4000.[1] At this rate, the HMDS should have no net result on the difference of grain size within the organic semiconductor, which in this instance is C8-BTBT.

During the substrate preparation process, it is also imperative that the substrate is properly cleaned in order to promote contact angle and adhesion of the small molecule to the substrate. There are several steps to this creation process, which will be described in detail later, however, one of particular importance is the use of a UV-ozone cleaning device. The ultraviolet lamp within a UV-ozone cleaning device emits two types of radiation at respective wavelengths of 185 and 254 nanometers. The 185 nm light works to dissociate O_2 into triplet atomic oxygen $O(^3P)$. This triplet atomic oxygen then reacts with O_2 in order to yield ozone O_3. This ozone is almost immediately broken down by the other wavelength light emitted, 254 nm. In comparison to the 185 nm light, the 254 nm light dissociates ozone versus typical atmospheric oxygen. The breakdown of ozone creates more O_2 and singlet atomic oxygen $O(^1D)$. This singlet atomic oxygen is the desired product in the sequence of these reactions. It possesses strong oxidation powers that allows for cleaning of inorganic substrates, such as silicon wafers. This progression is shown in further detail in Figure 1 below.



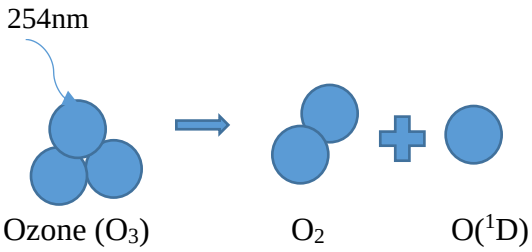


Figure 1: UV-Ozone Reaction Diagram

There are several advantages to the UV-ozone cleaning method. One is that this system uses oxygen radicals instead of releasing plasma discharge, which can cause charging damage. Furthermore, the process is completely liquid free which eliminates the need for disposal of waste chemicals.[5]

Chapter 2

Method and Procedure

2.1 Materials and Equipment

The following is a list of materials that were used throughout the experimentation process:

- 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT)
- Hexymethyldisilazane (HMDS)
- Anhydrous Toluene
- Tetrahydrofuran (THF)
- Silicon Dioxide wafer
- Plate glass slides
- Isopropyl Alcohol (IPA)
- Methanol
- Acetone

The following is a list of equipment that was used throughout the experimentation process:

- Hot plate
- Spin coater
- Brown glass vials
- Divided petri dishes
- UV-ozone cleaner
- Ultrasonic bath
- Stir bar
- Tweezers
- Substrate pick
- Glove box
- Air gun
- Deionized water dispenser
- Aluminum foil
- Sourcemeter/Probe station
- Glass substrates
- Zone annealing system

2.2 Methods and Procedure

This experiment was carried out using both a hot plate annealing technique and a zone annealing technique. Both electrical and optical characteristics were measured for this experiment in order to determine an overall correlation between the two. Furthermore, absorbance and conductivity were enhanced using different preparation temperatures and durations.

2.2.1 Recrystallization of C8-BTBT

Prior to solution creation and annealing, the C8-BTBT needed purified beyond its form from the manufacturer. In order to achieve this, a recrystallization process was used. The C8-BTBT solution was dissolved in anhydrous toluene at a ratio of 75 mg/mL. A stir bar was added, and the mixture was heated to 45℃ and stirred for approximately one hour. After one hour, the solution was placed in a fridge measuring approximately 5℃ in temperature. The solution was allowed to remain overnight, however, five hours is the true time necessary in order to observe C8-BTBT crystallization. The recovered mixture was then filtered and the C8-BTBT crystals were recovered in a yield of approximately 22%. In comparison to the C8-BTBT from the manufacturer, the recovered crystals appeared white and did not maintain their original yellow tint.

2.2.2 Cleaning Equipment

Each time the experiment was carried out one brown glass vial, one divided petri dish, one set of tweezers, and one stir bar needed to be cleaned. In order to clean the brown vials, they were first sprayed with an air gun. Next, they were filled with THF in order to degrade and residual chemicals. After disposal of the THF, methanol was then used to clean the vial followed by acetone. The vial was then dried via the use of the air gun and placed on an aluminum foil

tent in order to dry further. The petri dish was cleaned simply using the air gun and a quick rinse of acetone. The tweezers were cleaned using the exact same series of chemicals as the brown vials. Finally, the stir bar was cleaned using an ultrasonic bath/sonicator. The stir bar was placed in a 50 mL glass vial filled with THF and covered. The sonication bath was then applied for 20 minutes. This employs the use of sound energy in order to agitate residue particles on the stir bar and loosen those particles from adhering to the surface. This is critical in the solution creation process, because it ensures that no unwanted chemicals or residues are present in the vial prior to solution preparation. After the ultrasonic bath, the stir bar was further cleaned with THF, methanol, and acetone just like the brown vials and tweezers.

2.2.3 Solution Creation

Using the purified C8-BTBT and the clean brown vial/stir bar, a solution was prepared using a C8-BTBT to anhydrous toluene ration of 10 mg/mL. This solution was held at ambient temperature and allowed to stir for approximately one hour. Typically, the solution was prepared using 20 mg of C8-BTBT and 2 mL of anhydrous toluene. This is enough to cover approximately eight substrates with the solution via spin coating.

2.2.4 Substrate Preparation

When silicone dioxide wafers were used it was first necessary to cut the substrates into smaller 4 x 4 squares. Originally, the wafer comes in a large circular disc. Therefore, a substrate pick was used to break the wafer along square boundaries into these smaller pieces. The optimal testing zone on these substrates would be the inner 2 x 2 square on each 4 x 4 square. This would be the area most evenly coated and free of contaminants. The glass slides already came in small sections, so it was not necessary to break these any further. Using the cleaned tweezers, the substrates were held and first sprayed with IPA. They were then each dried with the air gun.

After this, the substrates were placed in a UV-ozone scrubber in order to clean the surface of each substrate via the reaction described previously. This was carried out for 20 minutes. At the end of this duration, the substrates were removed and rinsed with distilled water. This was done at a certain distance so that gravity created enough force for the water to impact the substrate efficiently. Each substrate was again dried using the air gun. Once again, they were then each placed in the UV-ozone scrubber for another 20 minutes. Following completion, the substrates are sufficiently cleaned and ready for spin coating.

2.2.5 Spin Coating

Once the solution and the substrates are both placed in the glove box, the spin coating process can begin. Each substrate was placed on the center of the spin coating device in order to allow for a vacuum between the two to be created. First, when applicable a HMDS surface treatment was applied. This was done on all of the plate glass slides and only the designated silicon wafers. Approximately 250 μL of HMDS was dropped onto the substrate. It was then spin coated at 4000 rpm for 60 seconds. After spin coating, the substrate was immediately annealed for 90 seconds at 90℃. Following this process, the C8-BTBT solution can then be applied. Approximately 250 μL of C8-BTBT in anhydrous toluene solution was dropped onto each substrate. These were then spin coated for 60 seconds at 700 rpm. This was in order to ensure an approximately 45 nm thick film on the substrate. The substrates were then ready to be annealed in order to ensure optimal electrical performance and absorbance.

2.2.6 Annealing

As mentioned previously, the quench duration, quench temperature, melt temperature, and application of the HMDS surface were all differentiating factors in the method of preparation for each substrate. Table 1 below shows the various options for the parameters altered on each

substrate. Each one had a specific combination of these parameters in order to determine which methods and preparation specifications created an ideal transistor with the largest charge mobility and highest absorbance.

Table 1: Variables altered to achieve optimal transistor performance.

Quench Temperatures (°C)	70	80	90
Melt Temperatures (°C)	110	120	130
HMDS treatment?	Yes	No	
Quench Duration (min)	2	3	4

It is important that the melt and quench steps are done in succession. As such, all the substrates were transferred to another glove box, which had side by side hot plates. The general process utilized one hot plate as the melt plate and one as the quench. First, the melt step was carried out. The designated substrate was placed on the melt plate and the given temperature for approximately one minute in order to ensure the molecule is melted properly, but that the molecule is also not overheated and degraded. After the substrate is taken off the melt plate it is then placed on the quench plate at the given temperature and for the given duration. Following the quench, the substrate was placed on a metal block in order to allow for proper cooling. Experimentation was done in which the substrates were left on the hot plate as both cooled simultaneously. However, this made no appreciable difference in the overall charge mobility of the transistors. Following annealing, the transistors had achieved crystallization and were ready be placed on the probe station/source meter in order to undergo testing to determine overall charge mobility.

2.2.7 Zone Annealing

Alternatively to hot plate annealing, zone annealing was also used on plate glass substrates in order to directionally induce crystallization in a more uniform manner and determine the absorbance spectrums of these substrates. The zone annealing setup utilized two nichrome wires of approximately 0.02-inch diameter. These wires were heated to a melt temperature of 110℃. The substrate was then placed in front of a moving mechanical arm, which works to push the substrate underneath the wires at a given rate. The substrate passes over two cooling blocks throughout the process that are held at approximately 22℃. A gap between the two blocks at the wires prevents overheating and melting of the substrate. This gap can ideally be varied from ¼-inch to 1/16-inch. This setup is displayed in Figure 2 with the substrate moving in the direction of the arrow. After crystallization, the plate glass substrates were tested for absorbance.

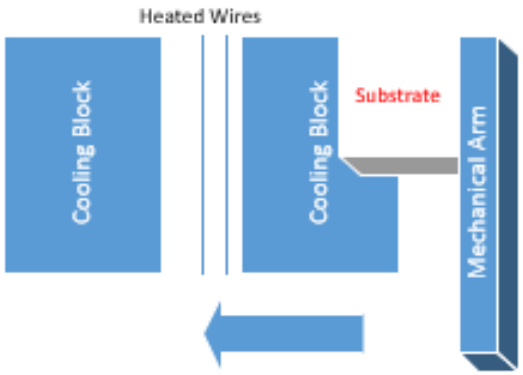


Figure 2: Zone Annealing Setup

2.2.8 Charge Mobility Testing

Prior to testing, the bottoms of each of the silicon dioxide wafers were scratched in order to create a better contact angle between the transistor and testing plate. Each substrate was then individually placed on the probe station. A scratching probe was first used to scratch the surface and isolate individual cells/devices. For the sake of this experiment, approximately five

cells/devices were tested and averaged over a certain range in order to determine the charge mobility of that transistor as a whole. Two probes were placed on each side of the respective device/cell and a current was passed through. The data was collected and charge mobility was calculated based off of the data.

2.2.9 UV-Vis Absorbance Spectrum

The plate glass substrates that were prepared both via hot plate annealing and zone annealing were tested for their absorbance spectrum using a UV-Vis spectrophotometer. The spot with the least imperfections on each substrate was chosen and the substrate was fastened into the spectrophotometer accordingly. The substrates were tested from wavelengths of 200-900 nm. The system utilized a single cycle, double beam, medium speed operation pattern in order to obtain that most accurate absorbance spectrum.

Chapter 3

Results and Discussion

First and foremost, the electrical properties of the given transistors were measured in order to determine optimal performance characteristics. The first property varied was quench temperature for its potential to have the largest alteration to electrical performance. As mentioned previously, the three quench temperatures used were 70℃, 80℃, and 90℃. Other variables were held constant. An HMDS surface treatment was applied, a melt temperature of 110℃ was used, and a quench duration of three minutes was used. The results of the most optimal quench temperature as well as the averages of each quench temperature are displayed below in Figure 3.

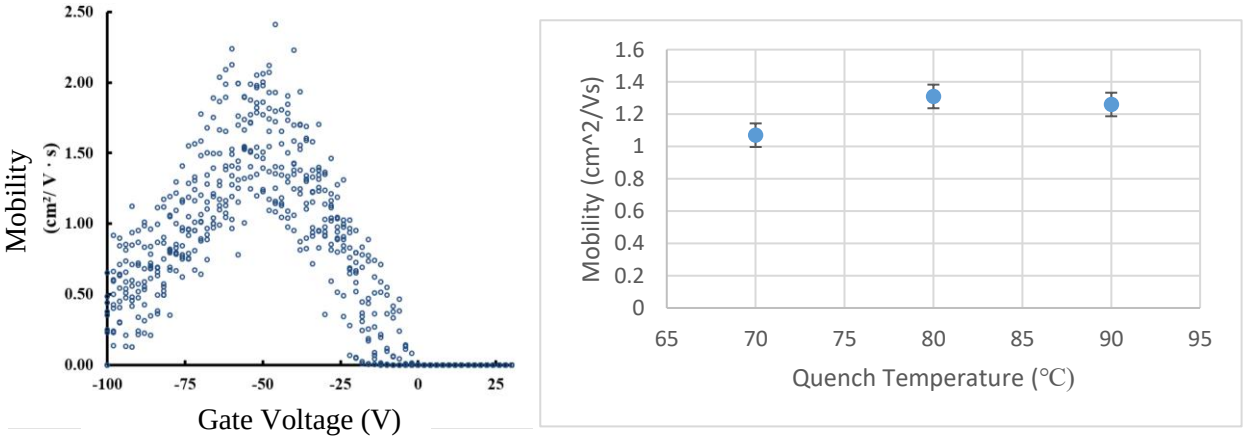


Figure 3: Charge mobilities of transistor using quench temperature of 80℃ and averages of each quench temperatures possible mobility with standard deviation bars.

In order to obtain averages of electrical characteristics, the mobility values between gate voltages of -25 to -75 V were averaged, which represents the area of peak mobility in the transistor. Initially, the mobilities increase as the gate voltage becomes more negative. However,

at some point near the peak, the mobilities reach saturation and thus begin to decrease. Thus, the active range would be between -25 to -75 V. This would be the optimal range to induce a gate voltage in industry. Based on these observations, it was determined that the most optimal quench temperature was 80°C. In the specified range, using a quench temperature of 80°C provided and average mobility of 1.31 cm^2/Vs. Quench temperatures of 70°C and 90°C only produced average mobilities of 1.07 cm^2/Vs and 1.26 cm^2/Vs respectively. As such, it would be recommended that 80°C be used as the quench temperature during transistor preparation. Furthermore, the transfer characteristics and output characteristics obtained from a transistor prepared in this manner are shown in Figure 4. This can help to show electrical characteristics and possible contact resistance issues.

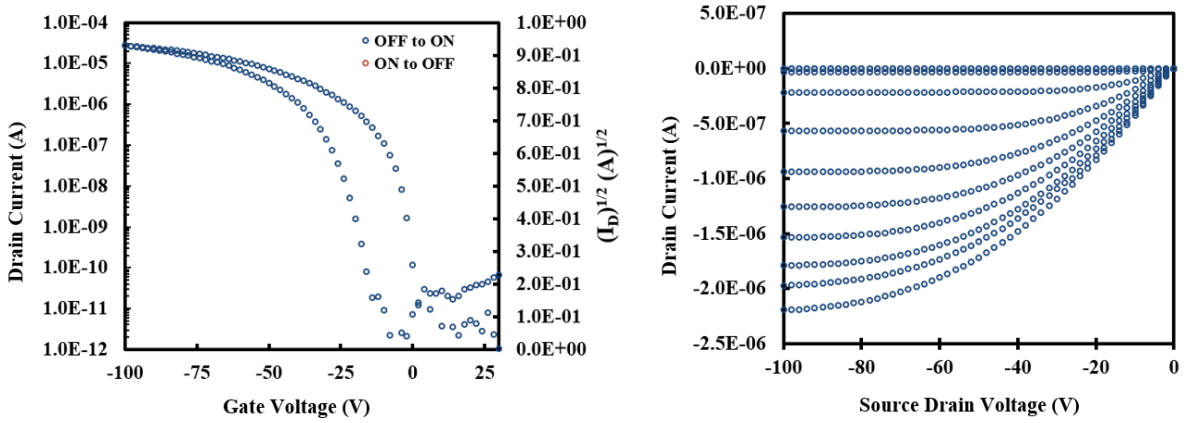


Figure 4: Transfer characteristics (left) and output characteristics (right) for a transistor prepared at optimal conditions

The next variable altered was the duration of the quench. The three times observed were 2, 3, and 4 minutes. All other variables were held constant. An HMDS surface treatment, melt temperature of 110°C, and quench temperature of 80°C were all used for this batch of transistors.

The most optimal duration as well as the averages of each quench duration are displayed in Figure 5.

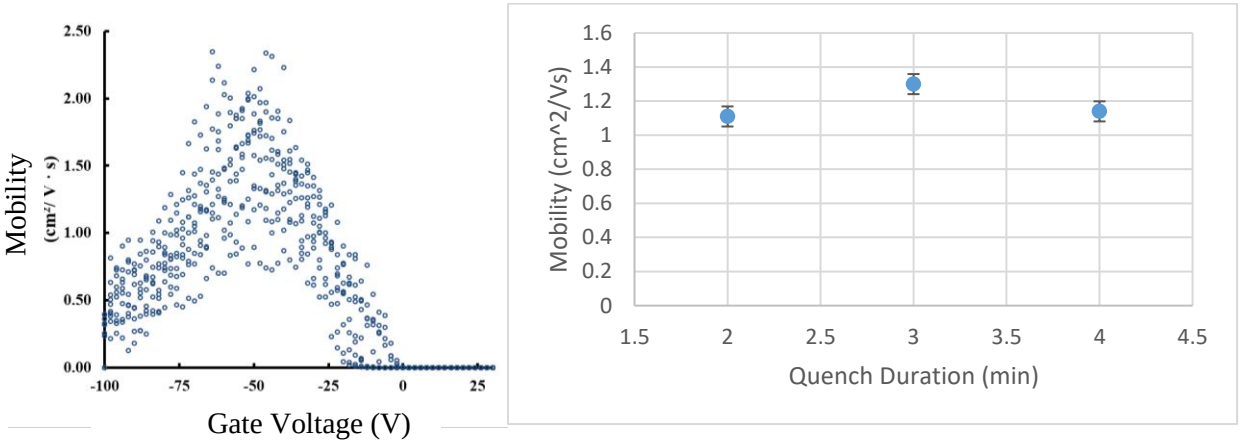


Figure 5: Charge mobilities of transistor using quench duration of 3 minutes and averages of each duration's mobility with standard deviation bars

From the above data it becomes clear that a quench duration of three minutes is most optimal. Again, averages were calculated across the -25 to -75 gate voltage range. The quench duration of three minutes represented a 1.30 cm^2/Vs mobility. The other duration of two minutes and four minutes only allowed for average mobilities of 1.11 cm^2/Vs and 1.14 cm^2/Vs. One interesting note here is that there is a large drop off in mobility in both the two- and four-minute durations. This indicates that two minutes would not be long enough to fully induce crystallization, whereas four minutes would overheat the molecule and cause potential partial degradation.

Another variable altered included the melt temperature. Since the C8-BTBT solution has a very specific melting point it is required that the temperature be at least 110℃ in order to fully melt the molecule. Therefore, the parameters tested were 110℃, 120℃, and 130℃. Every other variable was held constant. An HMDS surface treatment, 80℃ quench temperature, and three-

minute quench duration were used. The results of the mobility for the most optimal melt temperature and averages of each melt temperature mobility are displayed in Figure 6.

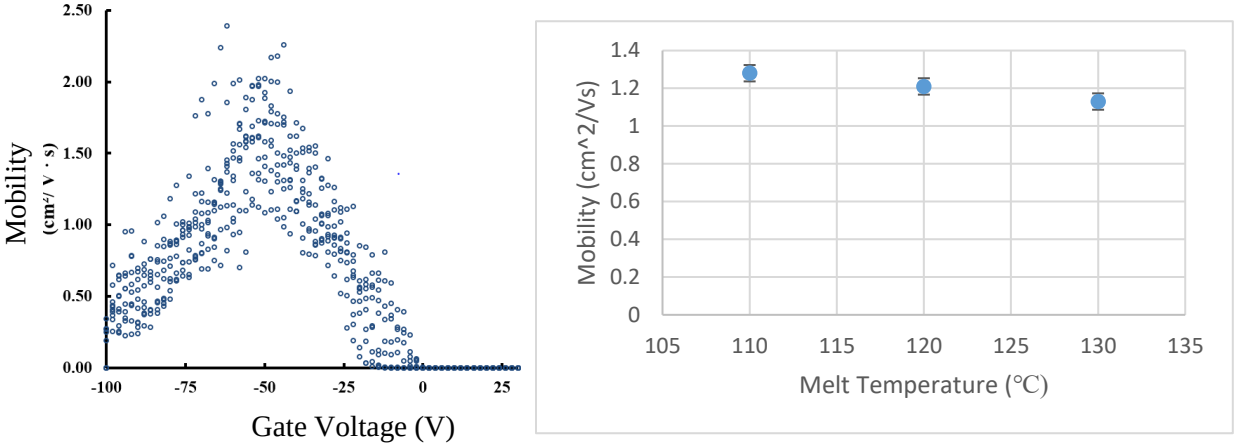


Figure 6: Charge mobilities of transistor using melt temperature of 110°C and averages of each temperature's mobility with standard deviations

These results show that a melt temperature of 110°C is most optimal. Like previously, these averages were calculated in the -25 to -75 gate voltage range. The average mobility at 110°C was 1.28 cm^2/Vs. The other two temperatures of 120°C and 130°C showed average mobilities of 1.21 cm^2/Vs and 1.13 cm^2/Vs respectively. From this data it can be concluded that temperatures above the specific melting point of the C8-BTBT solution harm mobility and do not promote crystallization. The temperatures may be too elevated and cause over melting and degradation of the molecule. As such, it is important to get very close to the melting point of the solution during the melt step.

Finally, the application of the HMDS surface treatment was tested for viability. In order to determine this, the optimal characteristics determined previously were used. However, only two transistors were tested. One with the HMDS surface and one without. In theory, the HMDS treatment should be beneficial because it allows the silicon dioxide layer to become hydrophobic. This allows for better contact angle, which leads to better crystallization and thus an overall

greater average charge mobility. The results of the mobility difference between a transistor with the surface treatment and without are shown in Figure 7.

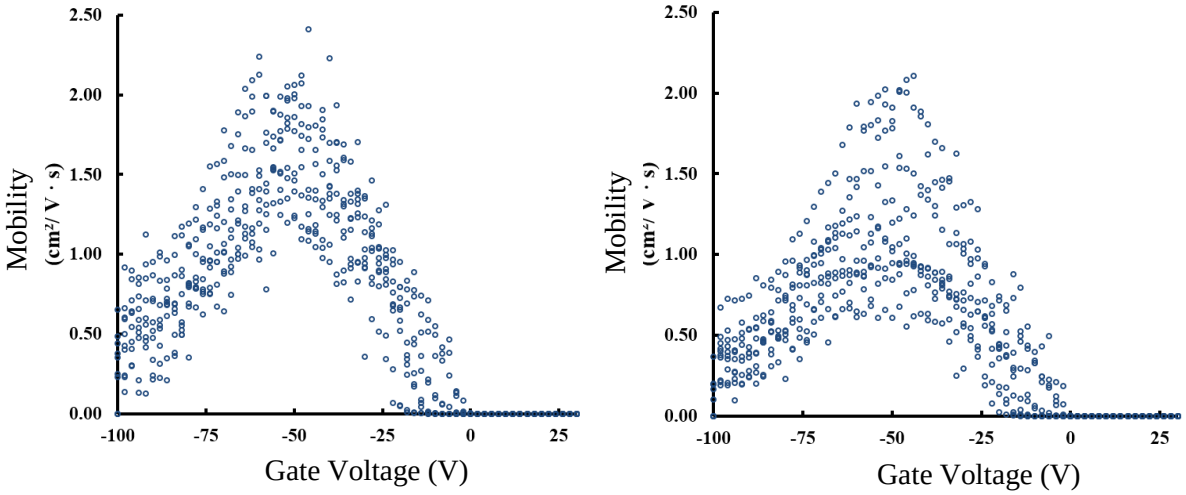


Figure 7: Charge mobilities of transistors with and without a HMDS surface treatment respectively

From the above data it can be seen that the application of the HMDS surface, represented by the graph on the left, is clearly beneficial. When using the average gate voltage range of -25 to -75 V, the average mobility of the transistor with the HMDS treatment is 1.31 cm^2/Vs. In comparison, the transistor without the treatment only has a mobility of 1.05 cm^2/Vs. One interesting note is that the mobility represented by that transistor without the HMDS surface also represents the lowest average mobility across all transistors tested. Since HMDS was applied to all other transistors, it can be concluded that the surface treatment clearly has an effect on contact angle and thus crystallization and mobility. The treatment is necessary in order to obtain optimal mobility output.

Finally, these mobility results can be analyzed against optical/absorbance results in order to determine correlations between the two. In theory, the crystallization of the C8-BTBT solution should cause electrons within the transistor to become more localized. This is what allows for

charge to be conducted easier within a crystallized transistor versus a non-crystallized one. This increased localization of electrons should permit an increased absorbance in the transistor as a whole. More charge is able to be passed through it. Therefore, the plate glass slides were prepared in order to test this absorbance and hopefully determine a correlation between mobility and absorbance.

For the purposes of experimentation, a zone annealing apparatus was also used during the plate glass substrate preparation. Zone annealing allows for more directional crystallization of a material versus typical hot plate annealing. As such, it could potentially allow for greater localization of electrons, greater absorbance, and greater charge mobility when applied to a silicon dioxide wafer.

First, comparisons were made in absorbance among the hot plate annealed slides. The two most promising techniques determined by electrical properties of transistors were applied in

the creation of the plate glass. Therefore, the plate glass tested from the hot plates are shown in Table 2.

Table 2: Plate glass prepared via hot plates to determine absorbance spectrums

Transistor #	Quench Temp. (°C)	Quench Duration (min)	Melt Temp. (°C)	HMDS treatment?
1	80	3	110	Yes
2	90	3	110	Yes
3	80	3	120	Yes
4	80	4	110	Yes

Based on these preparation methods, absorbance spectrums were determined for each substrate and compared against one another in Figure 8.

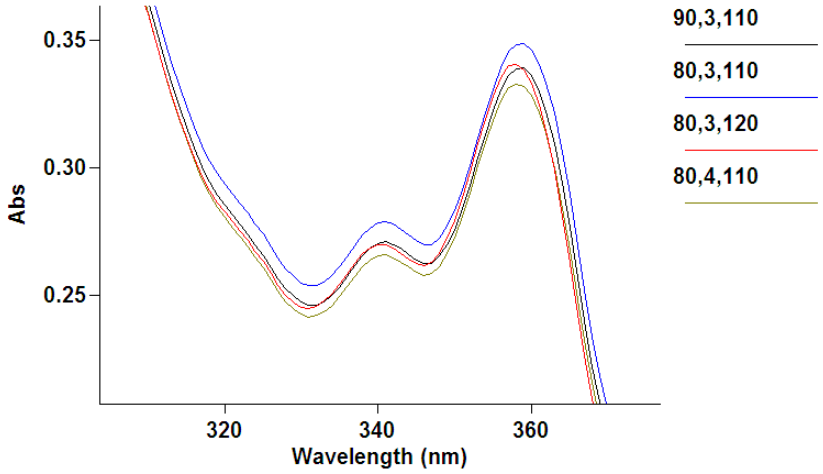


Figure 8: Absorbance spectrum of hot plate prepared substrates [quench temp., quench duration, melt temp.]

The range of interest is determined to be between wavelengths of 320-370 nm. This is where there are appreciable absorbance values and identifiable differences among the substrates prepared. After viewing these results a clear correlation is determined between electrical and

optical characteristics. The substrate that was prepared using a HMDS surface treatment, 80°C quench temperature, three-minute quench duration, and 110°C melt temperature, which represented by the royal blue line above, exhibits the highest absorbance when compared to others. Among the other properties altered it appears that a change in quench temperature would have the least negative effects on absorbance and thus mobility, followed by melt temperature, and finally quench duration.

A few select substrates were also prepared using the zone annealing system described previously. The goal of these tests being to determine whether using the zone annealer and achieving more directional crystallization is beneficial to absorbance. Therefore, properties altered in the zone annealer included temperature of the heated lines and speed of the substrate being pushed underneath the wires. The block spacing was held at 1/8 inch. The methods used to prepare the substrates of interest are detailed in Table 3.

Table 3: Plate glass prepared via zone annealing to determine absorbance spectrums

Substrate #	Wire Temperature (°C)	Duration of crystallization
1	110	1 hour
2	120	1 hour
3	110	30 min

Based on these preparation methods the absorbance spectrum was obtained for each substrate in comparison shown in Figure 9.

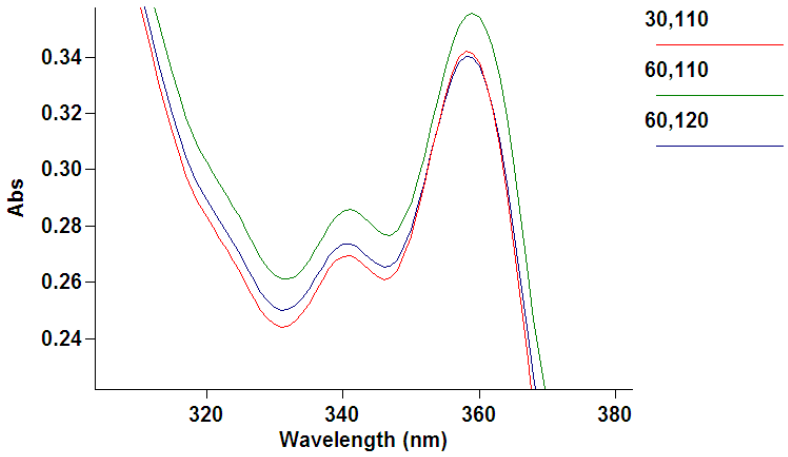


Figure 9: Absorbance spectrum of zone annealing prepared substrates [annealing duration, wire temp.]

Based on these results it can be seen that the ideal melt temperature of 110°C produces the best results when used as the wire temperature. Furthermore, an approximate time of one hour is also appropriate for this experimentation. Faster speeds and higher temperatures produced results with lower absorbance values. Faster speeds may not allow for every piece of the substrate to remain directly under the wire long enough in order to achieve melting of the C8-BTBT solution, which harms the crystallization process. Additionally, higher temperatures would have the same effect as they did during hot plate annealing. The increased temperature may cause the solution to over melt and could cause degradation of the molecule. This data aligns with data seen from the transistors tested previously. Increasing the melt temperature had a small adverse effect, whereas decreasing the rate of reaction produced the worst results. This is similar to how results were largely decreased when quench duration was changed.

When the zone annealed and hot plate annealed slides are plotted against one another even more trends can be seen. This overall graph is displayed in Figure 10. Data labeled with three numbers represents hot plate annealed substrates and their respective quench temperature,

quench duration, and melt temperature. Data labeled with two numbers represents zone annealed substrates and their respective annealing duration and wire temperature.

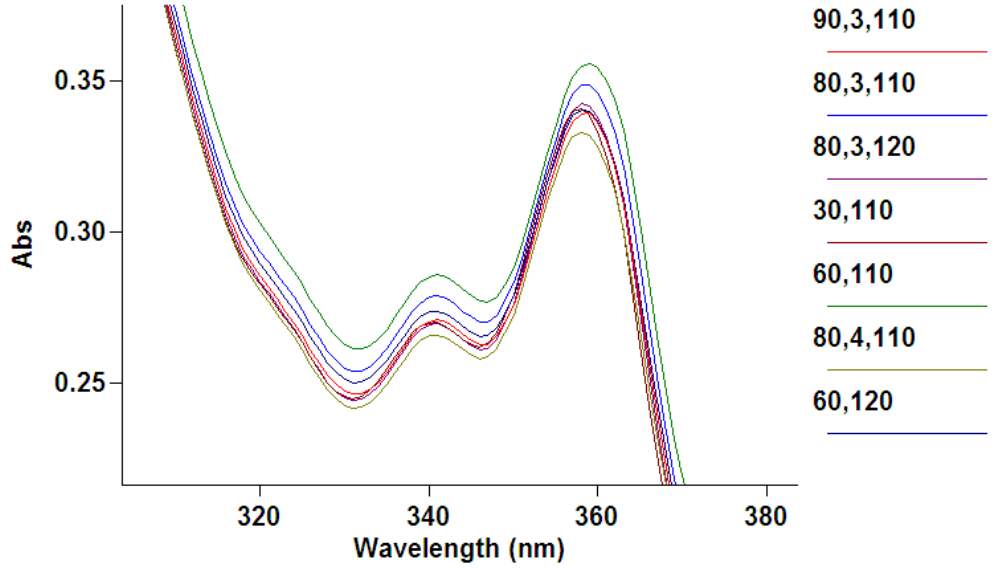


Figure 10: Absorbance spectrum including hot plate and zone annealed substrates

From Figure 10 it can be seen that the most optimal substrate optically was the zone annealed substrate annealed for one hour at a wire temperature of 110℃. This was also the most ideal among all the zone annealed substrates. Next comes the hot plate annealed substrate that was prepared using the best preparation methods determined previously. These methods include an HMDS treatment, 80℃ quench temperature, three-minute quench duration, and 110℃ melt temperature. Again, this was the most ideal substrate prepared using hot plate annealing techniques. Therefore, it can be concluded that using zone annealing to induce directional crystallization of substrates can result in greater absorbance and perhaps greater charge mobility as well. However, the use of correct temperatures and durations is still the foremost concern during transistor preparation. Furthermore, it can be seen that utilizing an incorrect duration causes the worst results. The worst results of both the zone annealed and hot plate annealed

slides included when the annealing duration was decreased and when the quench duration was increased, respectively. Several zone annealed substrates showed lower absorbance values compared to hot plate annealed substrates prepared using optimal conditions. Therefore, as a step for future research it could be beneficial to try to prepare transistors using the zone annealing process in order to determine charge mobility. As a side note, there was little workable time with the zone annealing system. As such, if more time were available some other parameters that could have been altered within the zone annealer could have been block spacing and cooling block temperature.

Chapter 4

Conclusion

In this research, the effects of different preparation methods on C8-BTBT transistor/substrate charge mobility and absorbance values were observed. The variables altered namely included quench temperature, melt temperature, quench duration, and the application of a HMDS surface treatment. These variables were altered during the crystallization process in order to induce more or less ordered molecular packing structure, which can lead to an increase or decrease in overall charge mobility. Quench temperatures were varied using 70℃, 80℃, and 90℃. Quench durations were varied using 2-, 3-, and 4-minute durations. Melt temperatures were varied using 110℃, 120℃, and 130℃. After testing differently prepared transistors using a sourcemeter, it was determined that the optimal conditions included the application of a HMDS treatment, 80℃ quench temperature, three-minute quench duration, and 110℃ melt temperature. The largest average mobility obtained between gate voltages of -25 to -75 V using the optimal parameters experimentally determined yielded a mobility value of 1.31 cm^2/Vs.

These results were then confirmed via the determination of UV-Vis absorbance spectrums for each substrate. During this process, select substrates were zone annealed in order to examine effects of directional crystallization. Annealing duration of 30 minutes and 1 hour were used. Wire temperatures of 110℃ and 120℃ were used. These results revealed that the usage of zone annealing using a wire temperature equivalent to the optimal melt temperature of 110℃ and an annealing duration of 1 hour produced the best absorbance values. This was

followed by the ideally prepared transistor using the hot plate technique. Along with the spectrums of the other substrates, a correlation was determined between absorbance and charge mobility. The substrates prepared using optimal techniques produced greater absorbance and mobility values. Further research could be done into testing the zone annealed transistors for charge mobility as well.

Appendix A

Additional Graphs Detailing Transistor Charge Mobility

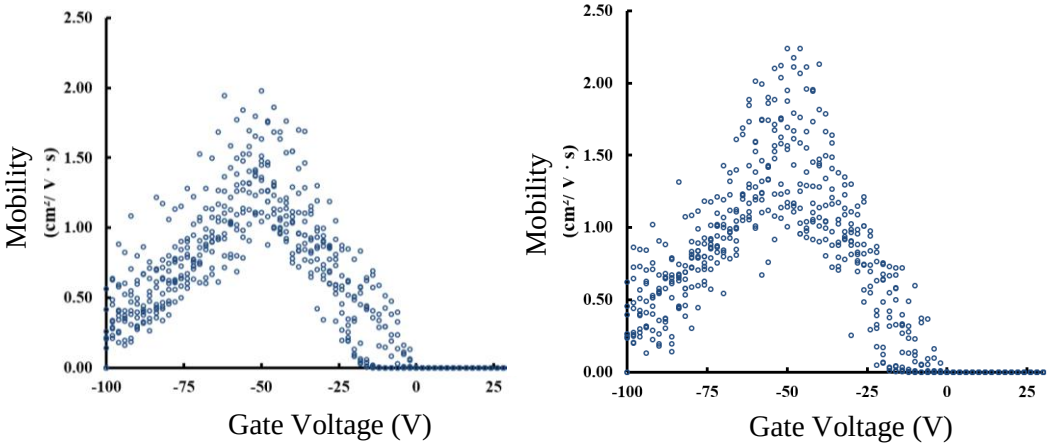


Figure 11: Charge mobilities of transistors using quench temperatures of 70°C and 90°C respectively

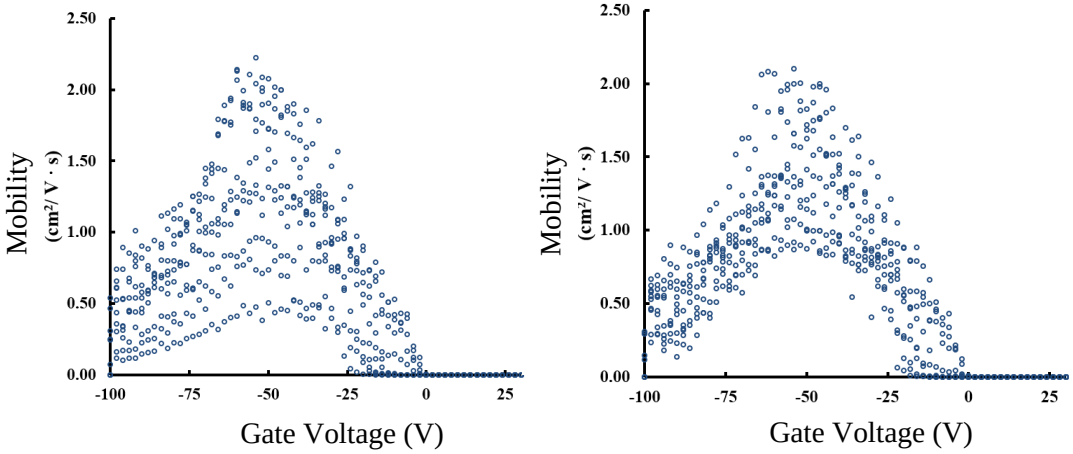


Figure 12: Charge mobilities of transistors using quench duration of 2 min and 4 min respectively

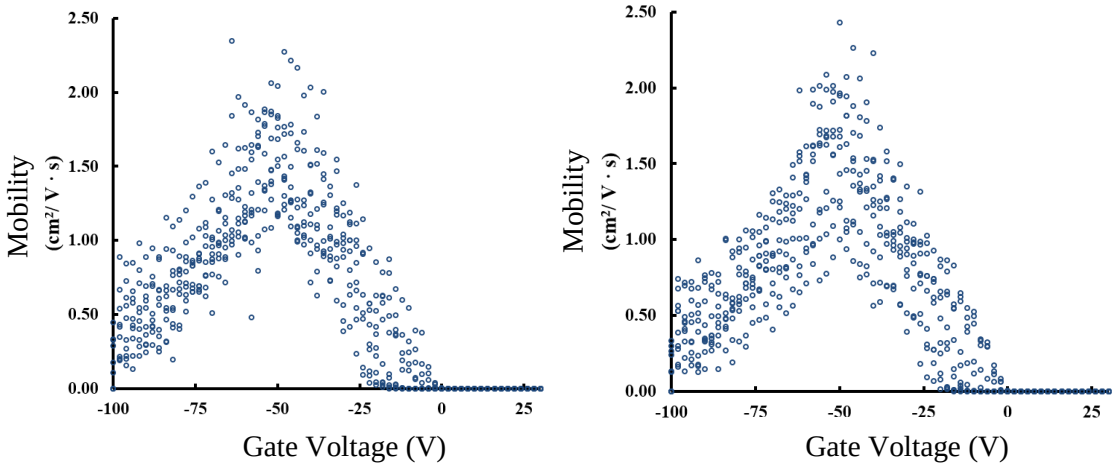


Figure 13: Charge mobilities of transistors using melt temperatures of 120℃ and 130℃ respectively

BIBLIOGRAPHY

1. Adhikari, J. M.; Vakhshouri, K.; Calitree, B. D.; Hexemer, A.; Hickner, M. A.; Gomez, E. D. *J. Mater. Chem. C*. **2015**, 3, 8799-8803.
2. Chai, Z.; Abbasi, S. A.; Busnaina, A. A. *ACS Appl. Mater. Interfaces*. **2018**, 10, 18123-18130.
3. Janneck, R.; Pilet, N.; Bommanaboyena, S. P.; Watts, B.; Heremans, P.; Genoe, J.; Rolin, C. *Adv. Mater*. **2017**, 29, 1703864.
4. Lim, S.C.; Kim, S.H.; Lee, J.H.; Kim, M.K.; Kim, D.J.; Zyung, T. Synthetic Metals. 2005, 148, 75-79.
5. The Basics of UV-Ozone Cleaning of Surfaces. https://www.samcointl.com/basics-uv-ozone-cleaning-surfaces (accessed January 10, 2019).
6. Yuan, Y.; Giri, G.; Ayzner, A. L.; Zoombelt, A.P.; Mannsfeld, S.C.B.; Chen, J.; Nordlund, D.; Toney, M. F.; Huang, J.; Bao, Z. *Nat. Commun*. **2014**.

ACADEMIC VITA

Hunter Miller
Hgm5032@psu.edu
(724) 651-7911

Education

Shenango Jr./Sr. High School, New Castle, Pennsylvania
Graduation Date: June 2015
Member of Peer Leadership, NHS, Student Council, Spanish Club, Football, Basketball, 12th grade class president, and academic games

The Pennsylvania State University (University Park)
Anticipated Graduation Date: Spring 2019
Anticipated Degree: B.S. in Chemical Engineering with minors in Spanish and Chemistry
Active member of Schreyer Honors College, Student Council, American Institute of Chemical Engineers, Phi Eta Sigma Honor Society, Intramural Athletics, and The National Society of Collegiate Scholars

Work Experience

Dallas W. Hartman P.C.
Law Clerk 2013-present

- Prepared Demand for settlement statements
- Prepared Mediation Statements and Presentations
- Drafted Interrogatories and Request for Document papers
- Drafted Complaints to instate cases

All-Star Seamless Gutter 2015-present

- Installed and delivered gutters and gutter supplies

Research

Dr. Enrique Gomez Undergraduate Research Team 2015-present

- Prepared Organic thin-film transistors (OTFTs) coated in C8-BTBT and P3HT molecules
- Identified effects of various properties such as temperature, annealing duration, application of a Hexymethyldisulfide (HMDS) surface treatment etc. on the charge mobility of OTFTs
- Analyzed the UV-Vis absorbance spectrum of various transistors and plate glass

Service/Volunteer experience

Easter baskets

- Made Easter baskets for those in nursing homes.

Tutoring

- Assisted in tutoring neighbor student and elementary age students.

Soup kitchen

- Worked with the soup kitchen of my local church to provide food for the hungry.

Make a Wish project

- Participated in special events and programs to raise money for the Make A Wish foundation.

Pro-life spaghetti dinner

- Helped work a dinner to raise many for pro-life campaigns.

Oktoberfest

- Worked an October festival at my local church to help raise money.

Rescue Mission

- Prepared and served a meal at the New Castle City rescue mission.

Honors/Awards

- Outstanding Citizenship award
- Undefeated in Equations at Tri-Bowl
- Top 5,000 scores on SAT or ACT in Pennsylvania
- High Honor Roll consecutively throughout high school career
- Valedictorian
- Lawrence County Bar Association Scholarship
- PA American water Stream of Learning Scholarship
- Range Resources scholarship
- AP calculus award
- Spanish Award
- AP Biology and Chemistry award
- Tri County Athletic Excellence award
- Wolves Club Scholarship
- Schreyer Honors College Scholar
- Dean's List for 5 semesters
- Induction into the National Society of Collegiate Scholars