A Study of Charge Mobilities in Annealed Poly(3-hexylthiophene-2 5-diyl) Thin Film Transistors and Optimization of Zone Annealing

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Abstract

Polythiophene thin film devices are promising sources of next generation organic electronics that may one day be implemented into industry as well as common household items. We have analyzed the charge mobility of poly(3-hexylthiophene-2,5-diyl) (P3HT) thin-film transistors (TFTs) under conditions of altered recrystallization kinetics. Charge mobility increases in regions of higher order in polythiophenes as a consequence of greater density of tie molecules. Our results suggest that controlling recrystallization kinetics and ultimately the number of higher ordered regions in P3HT, namely by increasing both quenching temperature and time, might result in increased charge mobility in polythiophene thin films. Our results also suggest that as TFTs degrade due to prolonged exposure to non-inert and non-vacuum environments charge mobility also decreases, characterizing the delicate nature of polythiophene thin films.

We have also analyzed the ability of zone annealing to enhance the UV absorbance and ultimately the density of ordered regions in P3HT thin films. Zone annealing allows for control of recrystallization kinetics over the thin film to a much higher degree than traditional hot plate annealing. We have found the optimal speed and cooling block spacing settings for the custom fabricated linear zone annealing apparatus to vary with temperature gradient based on heat source temperature. Future work with the zone annealing apparatus may utilize these results to alter the crystallization of thin films for transistor applications.
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I would like to thank my parents, sister, and friends for their love and support throughout both my research and college experience.
Chapter 1

Introduction

1.1 Thin Film Transistors

Various forms of organic electronic applications such as organic field effect transistors (OFETs), organic light emitting diodes (OLEDs), and organic photovoltaics (OPVs) rely on the usefulness of conjugated polymers. Chemical versatility, flexibility, and range of application of conjugated polymer devices have great potential to revolutionize the electronics industry as a whole.\(^1\) Another one of their big advantages is that they are solution processable. Flexibility and solution processability are characteristics of conjugated polymers that are inherently better for producing OFETs that may be used in new forms of wearable electronics and therefore make studying OFET technology of great importance to the electronic industry. Recently, conjugated polymers have been proven to have electroluminescent characteristics, that is, emitting light when excited by a small amount of electric current.\(^2\) With the rising number of applications of organic electronics, studying conjugated polymers is without doubt of vast importance for innovating the field. Within conjugated polymers, charge transport is determined by the effects of hopping events between localized states. By contrast, metals and traditional semi-conductors experience delocalized charge transport.\(^3\) When used as the active layer of thin-film transistors (TFTs) as seen in Figure 1-1, conjugated polymers can exhibit rather modest charge carrier mobilities but remain dependent on aspects of the thin film such as structure, ordered region connectivity, crystallinity, and crystal orientation.\(^1\)
Since these conjugated polymers are readily incorporated into TFTs, it is intuitive to attempt to increase the charge mobility characteristic to induce optimal TFT performance. Many conjugated polymers have charge mobilities near $10^{-7}$-$10^{-5}$ cm$^2$ V$^{-1}$s$^{-1}$, which is orders of magnitude lower than inorganic materials and are not yet viable for industrial applications.\textsuperscript{1} Despite a low average, certain polymers experience greater charge mobilities depending on often structure specific aspects of the polymer. For instance, poly (3-hexylthiophene), or P3HT, has had charge mobilities referenced at nearly $10^{-1}$ cm$^2$ V$^{-1}$s$^{-1}$.\textsuperscript{1} Figure 1-2a-b exhibits typical transfer and output curves for an “ideal” P3HT TFT. Thin film transistor performance is typically characterized by measuring the current, I, and drain voltages, V which are plotted in transfer curves. V is plotted logarithmically and a saturation regime from the plot shows a transition from a linear to saturation regime indicating device performance levels. Charge mobility is then calculated from the saturation region of the transfer curves which characterizes the electronic capabilities of OFETs.

Once a saturation regime value is determined, a plot is calibrated to reflect the current versus the gate voltage, $V_G$, where we locate a threshold voltage used in calculating the charge mobility of the thin film transistor. Substantial charge mobilities and general physical properties of semiconducting polymer TFTs are indicative of their usefulness in many areas and deem them worthy for further study.

**Figure 1-1.** A simple representation of a common thin film bottom gate field effect transistor.
Semiconducting polymers, especially polythiophenes, have gained significant notice recently due to their potential practicality in small devices ranging from flexible light emitting diodes to photovoltaics. Controlling recrystallization of these polymers is necessary to produce high value charge mobilities and optimize the transistors’ performances. Polymer crystallization occurs at nucleation points which polymer chains diffuse towards to start forming larger, more ordered crystal networks. Between the glass transition temperature and melting temperature ($T_m$) of the polymer, as temperature increases, so too does the ability of polymer chains to diffuse toward the nucleation sites and begin forming crystals. This temperature range is referred to as the “diffusion controlled regime” characterizing the dependence of the rate of crystallization on the diffusion of polymer chains. After this regime, nucleation dominates recrystallization. Once the $T_m$ is
exceeded it is even more difficult for nucleation to occur as the polymer is attempting to melt rather than form nucleation sites for crystal formation. In this temperature regime, it is likely that nucleation sites will not survive. The “nucleation-limited regime” reverses the trend created by diffusion controlled rates and a decrease in crystallization rate as temperature increases past the Tm is seen. Figure 1-2c portrays a representation of the diffusion and nucleation controlled regimes in polythiophene annealing.

Polythiophenes, especially thin films of polythiophenes, are susceptible to degradation over time in certain non-vacuum environments. N.C. Billingham et al. has shown that conductivity, which is a function of charge mobility, decreases in polythiophenes stored in environments containing air.⁵ Although glove boxes typically contain trace amounts of oxygen (10ppm O₂ or lower) the polythiophenes held under non-vacuum conditions may be exposed to enough O₂, through the glove box itself or from miniscule amounts transferred when the glovebox is opened by lab citizens in time frames exceeding 1 hour, to impair conductivity and ultimately charge mobility of the annealed substrates. Figure 1-3 illustrates the degradation of polythiophene thin films during exposure to air environment from Billingham et al. From the figure, it is seen that storing polymer thin films in P₂O₅ solution under vacuum hinders decay of the conductivity of a polythiophene. It is suggested then that to produce thin films with best performance, they must be stored properly under vacuum and in P₂O₅ solution for best results. These thin films may also be held strictly under vacuum if time between experimental processes is minimized.
Figure 1-3. From Billingham et al., Conductivity decay in polythiophene thin films at 70°C. Maintained in vacuum. Maintained in vacuum and P$_2$O$_5$. Arrows indicate where vacuum was broken.

By studying these aspects of polythiophene, especially P3HT, thin films in devices such as transistors we hope to determine favorable conditions to create high performance organic electronics and/or photovoltaics for industrial and commercial purposes.
1.2 Zone Annealing

In order to control thin film crystallization kinetics to a great degree, a strategy known as zone annealing may be employed. Zone annealing involves placing a polymer thin film under precise temperature gradients as seen in Figure 1-4. The goal of zone annealing relies on the melting of the polymer thin film at a localized region and then allowing the region to cool in a single direction, theoretically causing crystallization in a single, uniform direction. Utilizing this strategy would allow the polymer crystal to be uniform throughout the thin film and increasing its order or regions of order allows better charge transport through ties regions of higher density. 

Figure 1-4. Schematic of basic zone annealing of a TFT.

Berry et al. have shown that zone annealing spurs crystallization resulting in ordered tie region density that is suitable for rapid processing of polymers for nanomanufacturing, such as in transistors, based on self-assembly methods preferred by most copolymers. Zone annealing, therefore is a practical method for altering crystallization kinetics in polymer TFTs capable of respectable charge mobilities.
Here we utilized a custom, in-house, zone annealing apparatus designed and built for Gomez Lab crystallization studies to alter the crystallization kinetics of P3HT organic field effect transistors (FET). **Figure 1-5** shows the in house schematic alongside real images of the equipment.

![Figure 1-5. a) Schematic of the in-house zone annealing apparatus. b) Angled front view. c) Top view. d) Left side view. The zone annealing apparatus arm moves in a right-to-left direction.](image)

The in-house zone annealing apparatus contains a motor capable of velocities of as slow as 5 μm/s and up to a tested 40 μm/s. P3HT has a melt temperature of 238°C and thus the operation temperature of the nichrome wire heat source was chosen to be 250°C while copper cooling blocks were set at a water bath temperature of 20°C to simulate room temperature cooling.11
Chapter 2

Experimental Procedures

2.1 Materials and Equipment

2.1.1 Materials

- Poly(3-hexylthiophene-2,5-diyl) (P3HT)
- 1,2,4 trichlorobenzene (TCB)
- Tetrahydrofuran (THF)
- Acetone
- Methanol
- Isopropyl Alcohol (IPA)
- Bottom contact field effect transistors (FET)
- Glass substrates
- Hexadecane
- Tetramethyl orthosilicate (TMOS)

2.1.2 Equipment

- 10 mL beaker
- 500 mL beaker
- 2 mL amber vials
- 10 mL graduated cylinder
- Micro magnetic stir bar
- Wafer tweezers
- Diamond scribe
- Ultra sonicator
- UV Ozone cleaner
- Spin coater
- Glove box
- N2 cleaning gun
- Drying oven
- Aluminum foil
- Hot plate
- Device testing probe station
- Balance (±0.0001 g)
- UV Vis Spectrometer
- In-house zone annealing apparatus (see Figure 1-5)
- Dinocam microscope
2.2 Methods

2.2.1 Solution Preparation

Regioregular P3HT (>90% RR) solutions of 10 mg mL$^{-1}$ were made with 1,2,4-trichlorobenzene (Sigma-Aldrich) in an inert N$_2$ environment. The solutions were mixed on a hot plate with stir function at 25ºC and 800 rpm for 12-14 hours (overnight).

2.2.2 Substrate Preparation

Bottom contact FET plates were cut into 1cm by 1cm squares using a diamond scriber. The FETs were rinsed with IPA and subject to a UV ozone cleaner for 20 minutes. Substrates were then rinsed with water, dried with an N$_2$ gun and again subject to a UV ozone cleaner for 20 minutes. After the second UV ozone cleaning, FETs were added to approximately 8mL of hexadecane per substrate and coated with 40μL of TMOS. The FETs were allowed to sit for approximately 12-14 hours at room temperature. Following TMOS treatment, the FETs were rinsed with IPA and dried with an N$_2$ gun and moved to an inert N$_2$ glove box for spin coating.

The P3HT/TCB solutions were premixed at 600 rpm and heated to 90ºC for 2 minutes. 250μL of solution were pipetted onto the substrate and allowed to stand for 40 seconds. Films were cast at 1000 rpm for 4 minutes to yield a thickness of ~40 nm per substrate. P3HT solution was cast over bottom-contact, bottom-gate FETs as seen in Figure 2-1. Transistors were comprised of heavily p-type silicon doped gate electrodes with a 300 nm think thermally grown SiO$_2$ layer as
the gate dielectric (C=10.6 nF/Cm², Process Specialties) with 100 nm thick gold source and drain electrodes fabricated with 220 µm wide by 20 µm channels.7

Figure 2-1. A P3HT thin-film transistor and devices (made up of small gold electrodes) under the polymer layer.

2.2.3 Hot Plate Annealing and Testing

To optimize quenching temperature, transistors were placed on a calibrated hot-plate set to 240°C for an annealing time of 1 minute to melt the P3HT films. We chose 240°C on the basis that it exceeds the highest recorded melting temperature for P3HT at 238°C. Immediately post annealing, substrates were quenched on an adjacent hot plate at temperatures ranging from 140-220°C (quench temperatures) in 20°C increments. Charge mobilities were calculated and the optimal temperature was used in a subsequent test with varying quenching times of 10, 30, 90, 150, and 270 seconds respectively. As a control, a substrate was annealed at 150°C for 3 hours and quenched at room temperature. All procedures were performed in an inert N₂ glovebox.

The annealed TFTs were moved to another inert N₂ glove box containing the device testing probe station. A Dinocam™ microscope was used to set testing probes onto the transistor source and drain gates. Forward and reverse sweep settings were set according to Table 2-1 and output settings according to Table 2-2.
Table 2-1. Forward/ reverse transfer testing settings.

<p>| | |</p>
<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>Gate Start Voltage (V)</td>
<td>100</td>
</tr>
<tr>
<td>Gate Stop Voltage (V)</td>
<td>-100</td>
</tr>
<tr>
<td>Gate Step Voltage (V)</td>
<td>-2</td>
</tr>
<tr>
<td>Source-Drain Start Voltage (V)</td>
<td>-100</td>
</tr>
<tr>
<td>Source-Drain Stop Voltage (V)</td>
<td>-100</td>
</tr>
<tr>
<td>Length (µm)</td>
<td></td>
</tr>
<tr>
<td>Width (µm)</td>
<td>220</td>
</tr>
<tr>
<td>End Voltage (V)</td>
<td>-80</td>
</tr>
<tr>
<td>Capacitance (F/cm²)</td>
<td>1.06x10⁻⁸</td>
</tr>
</tbody>
</table>

Table 2-2. Output testing settings.

<p>| | |</p>
<table>
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<tr>
<th></th>
<th></th>
</tr>
</thead>
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<tr>
<td>Stop Voltage (V)</td>
<td>-100</td>
</tr>
<tr>
<td>Step Voltage (V)</td>
<td>-2</td>
</tr>
<tr>
<td>Gate Stop Voltage (V)</td>
<td>-100</td>
</tr>
<tr>
<td>Gate Step Voltage (V)</td>
<td>-20</td>
</tr>
</tbody>
</table>

The testing program (Appendix A) tested both forward and reverse source/drain voltages and output current. Charge mobilities were calculated in Microsoft Excel using the equation for charge mobility in Equation 2-1. Charge mobilities of TFTs were tested in the Steidle Building at The Pennsylvania State University.
\[ \mu_{\text{sat}}(V_G) = \left( \frac{\partial \sqrt{I_{D,\text{sat}}}}{\partial V_G} \right)^2 \times \frac{2L}{WC} \quad \text{Equation 2-1} \]

\( V_G \) = gate voltage, voltage between the silicon layer and the source layer.
\( I_{D,\text{sat}} \) = saturation current based on the transfer plot, measured between source and drain.
\( L \) = length between source and drain
\( WC \) = electrode width times capacitance

We calculated the charge mobilities from the device saturation region which is preferred due to its independence of source-drain voltages and less sensitivity to contact issues. Substrates were not held under vacuum between annealing and device testing. Annealing and testing were also completed 12~14 hours apart from one another. We hypothesized that degradation had occurred during this period between annealing and testing from the glovebox environment resulting in proportionally low charge mobilities. To confirm or hypothesis, a second batch of P3HT transistors were made following the prior experiment and held under vacuum between annealing and testing. Annealing and testing occurred within 4 hours of one another to reduce the time degradation could occur. We again tested devices on these TFTs using the same device testing procedure as previously described to compare to the substrate batch tested without vacuum storage.

2.2.4 Zone Annealing and Testing

The in-house zone annealing apparatus was controlled by a custom LabView program (Appendix B) to control the motor velocity and collect thermocouple data. Two 1 inch by 1 inch glass substrates were prepared based on the substrate preparation methods alongside preparation of the 10 mg mL\(^{-1}\) P3HT/TCB solution to make P3HT thin films. The nichrome wire heat source was powered by an outside voltage and current adjustable power source until a sweeping thermocouple reached 250\(^{\circ}\)C directly under the wire. Substrates were zone annealed at 20 \( \mu \text{m/s} \) with a 1/8 inch cooling block spacing. The LabView program was executed to move the
substrate approximately 4 inches (ensuring complete clearing of the nichrome heat source) and were allowed to completely cool on the left most cooling block. Two control substrates were prepared; one subject to hot plate annealing at 150ºC for 3 hours and the other remained unannealed.

The substrates were tested by UV-vis spectroscopy with a spectrum range of 300nm to 800 nm. Absorbances were compared for substrates based on both velocity and cooling block spacing and again compared to control substrates used as reference spectra in order to select optimal annealing settings for P3HT thin films.
Chapter 3

Results and Discussion

3.1 Hot Plate Annealing and Degradation

Films of conjugated P3HT typically utilize amorphous regions within the polymer to carry charge thus favoring dependence on these amorphous regions. With heat above a transitional temperature (236°C), P3HT is able to reorient amorphous regions into longer ordered chains. Charge mobility dependence therefore decreases in amorphous regions and increases in the new highly ordered domains. First, we examined quenching temperatures under the 240°C annealing temperature and above the 150°C control in 20 degree increments at a standard 90 second quench time interval. Figure 3-1a displays the charge mobilities measured with respect to temperature controlled recrystallization kinetics. Despite low charge mobilities compared to a typical P3HT TFT, seen in Figure 1-3, Figure 3-1a suggests that quench temperatures closer in magnitude to the initial annealing and melting temperature produce higher charge mobilities. The suggested trend agrees with the argument that as temperature reaches the T_m of P3HT, the limit of the diffusion-controlled regime is reached with rate increasing as the temperature increases. Using this notion, we examined recrystallization kinetics as a function of time using a quenching temperature of 220°C. Lengthening the time under quench was hypothesized to increase the charge mobility due to the longer period under conditions optimal for formation of longer chain molecules with intermolecular ties beneficial for charge carrying character. Without exceeding the Tm of P3HT, the crystallization rate of the polymer chains is maximized which correlates to higher charge mobilities seen in the P3HT TFT devices.

After determining the best temperature for increasing charge mobility was 220°C, we then controlled recrystallization by varying
the amount of time under quench post annealing. We hypothesized that longer time lengths under quench should correlate to more order and ultimately better charge mobility in the devices. Answering this question would provide insight as to how the polymer chains respond to quenching over time and would determine an optimal time for which to quench the TFTs to see highest charge mobilities. We tested 5 quench time ranges of 10, 30, 90, 150, and 270 seconds after a 60 second annealing period at 240°C. Figure 3-1b shows the charge mobilities calculated after varying the quenching times. Charge mobilities generally increased as time under quench increased, reaching close to ideal charge mobility of 0.04 cm²/Vs, at the time length of 270 seconds. As we allowed longer quench times, diffusion-controlled recrystallization was maximized for longer periods of time as polymer chains moved to the nucleation sites and crystallized resulting in heightened charge mobilities as displayed in Figure 3-1b. Ultimately, it was determined that by controlling recrystallization kinetics we can optimize charge mobility in P3HT devices, namely these TFTs.

a)
b) Figure 3-1. a) charge mobilities at varied quench temperatures show higher magnitudes at temperatures closer to the $T_m$. b) charge mobilities at 220°C annealing temperature and 25°C quench temperature with varied quench time intervals exhibit higher magnitudes at longer quench periods.

Figure 3-1 also shows uncharacteristically low charge mobilities of the P3HT TFTs post annealing. Typical charge mobilities of our P3HT TFTs range from 0.05-0.08 cm²/Vs, much higher than the $\sim 10^{-3}$ and lower values seen in the P3HT TFTs annealed under test conditions. After initial experiments of the time and temperature varying annealing processes, we hypothesized that the time and storage of the TFTs between annealing and device testing may have contributed to decay of the charge mobilities compared to typical P3HT TFTs. Figure 3-2 is the charge mobilities of a batch of P3HT TFTs casted, annealed, and tested within in a four-hour time frame (b) while also being held under vacuum between each experimental step compared to (a) a typical P3HT TFT charge mobility range of our transistors not stored under vacuum between experimental steps.
As seen in Figure 3-2, charge mobilities were more ideal in the TFTs when they were stored under vacuum and tested in a much shorter time frame than the previous batch. Therefore we can conclude that as time increases and if the environment is non-vacuum, during storage of a polythiophene polymer, the charge mobility decreases.⁵
3.2 Optimized Zone Annealing Settings

An optimization study was performed to define optimal zone annealing conditions of motor speed and cooling block spacing for optimal absorbance of P3HT in UV-Vis. Glass was utilized as the substrate and baseline corrected absorbances were found for a light spectrum range of 300 to 800 nm. Optimal conditions would show higher absorbances in the P3HT after baseline correction as the greater order and density of tie regions of P3HT would allow higher amounts of electron absorbance from photons. Initially, the velocity was studied with speeds of 5μm/s, 10μm/s, and 20μm/s with block spacings of 1/16 inch, 1/8 inch and 1/4 inch individually. Figure 3-3 shows the absorbance spectra of P3HT thin films cast on glass substrates for different motor speeds at constant cooling block spacings.

![Absorbance Spectra](image)

**Figure 3-3.** a) Absorbance spectra for various speeds at 1/4 inch block spacing. b) 1/8 inch cooling block spacing. c) 1/16 inch cooling block spacing.
Figure 3-3 evidences that for each cooling block spacing, a different motor speed is optimal for producing the highest absorbance spectra in the thin films. The results are tabularized in Table 3-1.

Table 3-1. Motor speeds necessary to produce the highest absorbance for each block spacing.

<table>
<thead>
<tr>
<th>Cooling Block Spacing (inches)</th>
<th>Motor Speed (μm/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/4</td>
<td>20</td>
</tr>
<tr>
<td>1/8</td>
<td>5</td>
</tr>
<tr>
<td>1/16</td>
<td>10</td>
</tr>
</tbody>
</table>

No trend exists for deciding the optimal motor speed for each cooling block spacing. However, each block spacing is necessarily defined by a successful motor speed that optimizes the absorbance spectra for P3HT thin films. Likely the reasoning for the disparity and lack of trend produced is due to the temperature gradient which is a function of cooling block spacing and not the motor speed. Temperature gradient is calculated using Equation 3-1 below.

\[

\nabla T \left( \frac{^\circ C}{mm} \right) = \frac{\text{Wire temperature} - \text{Cooling block temperature}}{\text{Cooling block spacing}}

\text{Equation 3-1}

\]

The temperature gradient for a zone annealing experiment the will thus determine the optimal speed based on the results from Table 3-1. Therefore, the block spacing is the most important aspect of accessing higher absorbances and ultimately higher density of ordered regions within thin films. It may be assumed that reaching temperatures above the melting temperature for a given polymer thin film will result in a localized melt but the temperature gradient results in better control of recrystallization utilizing the optimized speeds for the custom zone annealing apparatus.
Chapter 4

Conclusion

We have examined the charge mobilities of P3HT thin films with respect to crystallization kinetics. Our results show that charge mobilities increase with higher rates of crystallization in P3HT and that storage of polythiophenes in non-vacuum environments over time leads to decayed charge mobilities. Also, it is a necessity to store polymer thin films under vacuum conditions for condensed amount of times between casting, annealing, and device testing to preserve ideal charge mobilities in the transistors. By controlling the rate of crystallization with temperature, we can conclude that crystallization control may be vital in determining electrical properties of polythiophene electronic devices. We expected this effect would be enhanced if we linearized the recrystallization of the polymer chains through a zone annealing process creating higher ordered regions of crystals at higher rates. It was determined that for the custom zone annealing apparatus that block spacing determines the temperature gradient and therefore, speed settings must be set according to a particular temperature gradient. The temperature gradient is, therefore, the most necessary to optimize to produce high absorbances which translates to higher order within P3HT thin films. It is suggested that a variety of temperature gradients be studied for P3HT thin films. We also expect sustained stability of thin film devices by use of optimal storage techniques thus enhancing and improving charge mobility and device functionality as it applies to organic electronics.

Future work may look to utilize the zone annealing apparatus for annealing TFTs of P3HT and other higher conductivity polymers for heightened charge mobilities based on optimal temperature gradients, which was outside the scope of this study. Transistors may also be placed in the zone annealing apparatus with both perpendicular and parallel alignment with respect to the transistor
direction in order to study charge mobilities both inter- and intramolecularly. Zone annealing of TFTs would prove useful for fabricating transistors with higher charge mobilities possibly comparable to current industrially utilized materials and may be the future of semiconductors in electronic devices.
Bibliography


Appendix A

Input screen for the transfer sweep and output curve settings defined in Table 2-1 and Table 2-2.

(Default values are shown in the image above).
Appendix B

The LabView program user interface utilized in zone annealing. Motor speed is controlled using the Velocity, No. of Steps, and Step Size inputs. TC0 shows the temperature reading of the thermocouple for substrate temperature. TC1 shows the cooling block temperature at all times during annealing. TC2 and TC3 are unused by the program but these thermocouples remain ready to be used. The distance vs. temperature graph depicts the real time temperature profile and ultimately the temperature gradient of TC0 for the temperature of the substrate being annealed.
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SUMMARY
Penn State senior pursuing a Bachelor of Science in Chemical Engineering. Seeking to utilize chemical engineering internship experience and acquired skills in business processes and operations. Experience in qualitative and quantitative research, data analytics, and startup operations. Interested in technical solutions, consulting, and sales.

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Graduation: May 2019

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Air Liquide Industrial Gases – Process Controls Intern
Air Liquide Large Industries, Houston, TX
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- Compiled over 300 alarm tags in master engineering spreadsheet
- Conducted evaluative meeting with plant operators and on-site management teams
- Co-developed a calculation program designed to easily determine the cost of new business using several variables and standard company cost analyses
- Presented final project for alarm improvement for 2 pilot plants

Hillis Carnes Engineering Associates Intern
Hillis Carnes Engineering Associates, Frederick, MD
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- Certified APNGA Nuclear Density Gauge Operator

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- Analyze thin film transistors for electronic capacities
- Collaborate with graduate researcher for electron microscope analysis

National Cancer Institute Biomedical Research Assistant
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- Engineered RNA templates for HIV-1 detecting proteins
- Exposed proteins to HIV-1 virus and analyzed by microscopy the localization of detection proteins
- Presented findings at NIH Spring Research Festival among ~500 student/ fellow projects

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Member, American Institute of Chemical Engineers 2016 - 2018