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Moore's Law is Ending: What Comes Next?

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ABSTRACT

Moore's Law has been the driving force behind the exponential growth in computing power over the past few decades. However, the end of this law has raised concerns about the future of the semiconductor industry and technical progress as we know it. This thesis paper explores potential solutions for continuing technical progress beyond the limits of Moore's Law. The paper examines several emerging technologies such as Graphene and carbon nanotubes, quantum computing, spintronics, and optical computing. Some of these solutions are materials based meaning computers will still function based on the same principles, while some would mean completely new ways of computing such as replacing electrons with photons. These technologies offer promising possibilities for enhancing computing performance and improving energy efficiency beyond the limitations of traditional silicon-based devices. In this paper, we analyze the advantages and disadvantages of each technology and their potential impact on the future of computing.

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Chapter 1

Introduction

Moore's law, observed by Gordon Moore in 1965, states that the performance of computers, in terms of speed and capability, can be expected to double every year due to the increase of transistors able to fit in an integrated circuit. Although this is not a scientifically proven theory, it has held true up until recently. As devices are approaching the nanometer scale, it is becoming increasingly difficult to continue this trend, and progress is ending at different rates for different technologies due to the various limiting factors. The two main limiting factors, which will be discussed in the following two sections, are physical device limitations and manufacturing difficulties with economic constraints only making these limiting factors worse.

Lithography

Lithography is the manufacturing process of forming the desired structures on a silicon wafer. The most recent widely used method of lithography is optical lithography. Although progress with optical lithography is beginning to slow, improvement has been able to continue through methods such as higher resolution lenses and phase shifting. Phase shifting uses the topography of the mask to alter the phase of the radiation. This creates interference that results in a sharper image on the wafer. Despite methods such as these, researchers do not expect progress of optical lithography resolution to continue past about 100 nm [1].

To go below this 100 nm threshold techniques such as x-ray lithography and electron beam lithography are being pursued. However, they both have significant challenges. X-ray lithography has been able to produce components on a wafer as small as 30 nm, but it is worth noting that this result was only experimental. 30 nm is a very favorable result though since transistors much smaller than this run into their own physical limitations (these limitations will be discussed later). Before x-ray lithography can be used at a large scale there are two challenges that must be overcome. Firstly, it is very difficult and expensive to produce masks for this method. Secondly, x-ray lithography is much more sensitive to imperfections than optical lithography [1].

Electron beam lithography has even more impressive resolution than x-ray, being able to produce features as small as about 10 nm. Electron beam lithography has already been able to overcome obstacles such as electron scattering. However, it is limited by its speed. Electron beam lithography is very slow compared to other methods making it currently unsuitable for mass production [1].

Physical Limitations

In order to add more transistors to microchips, the active power of each transistor must scale down with their size in order to follow Dennard Scaling. Dennard Scaling is the principle that as transistors get smaller, their power density should remain the same, and this principle is a major contributor to Moore's Law holding true over the last few decades. Active power of a transistor is defined by the following equation.

Equation 1 [1]

$$P_{ac} = \left(\frac{C_{sw}V_{dd}^2}{2}\right) f$$

Operating frequency and switching capacitance have been increasing with technological progress to allow for faster computing. As is evident by equation 1, an increase in frequency and switching capacitance will drive an increase in active power. This leaves only supply voltage left to be scaled down in order to maintain Dennard Scaling. However, scaling down supply voltage is not trivial because of minimum threshold voltage requirements. As can be seen from equation 2 below, decreasing the worst-case threshold voltage, which is typically about 200 mV below room temperature Vt, increases standby power [1].

Equation 2 [1]

$$P_{off} = W_{tot}V_{dd}I_0 \exp\left(-\frac{qV_{t,WC}}{mkT}\right)$$

Due to this, the current minimum threshold voltage is around 0.3 V. A problem arises because the ratio of Vdd/Vt must be high enough to achieve gate overdrive, a key operating mode for transistors. Therefore, due to the limit of Vt at 0.3 V, Vdd cannot be scaled down past about 1 V [1].

Short channel effect also inhibits decreasing threshold voltage because it is a key factor in determining the worst-case threshold voltage. The short channel effect decreases threshold voltage because short-channel devices experience electrostatic charge sharing at the gate and source/drain regions. Short-channel effect can be minimized by decreasing the thickness of the gate oxide. However, the gate oxide can only be thinned to a certain point before quantum effects start to affect the transistor's performance. If the gate oxide is too thin, quantum

tunneling can occur, causing gate leakage which is detrimental to the transistor's functionality [1].

Flash Memory

Flash memory has been leading technological advancement in terms of smallest feature size, device density, and cost. However, its rapid progress means that it will likely be one of the first technologies to break from the trend of Moore's Law. In order to store more data, flash memory has shifted from single layer cell (SLC) memory to multilayer cell memory (MLC) and enterprise MLC (eMLC). Although these changes did achieve the added storage, they came with significant tradeoffs. For example, MLC and eMLC memory has a larger error correction requirement, lower endurance, and longer program and read time. The switch also comes with the introduction of read disturb errors which when reading data from a cell causes other cells in the block to change value [2].

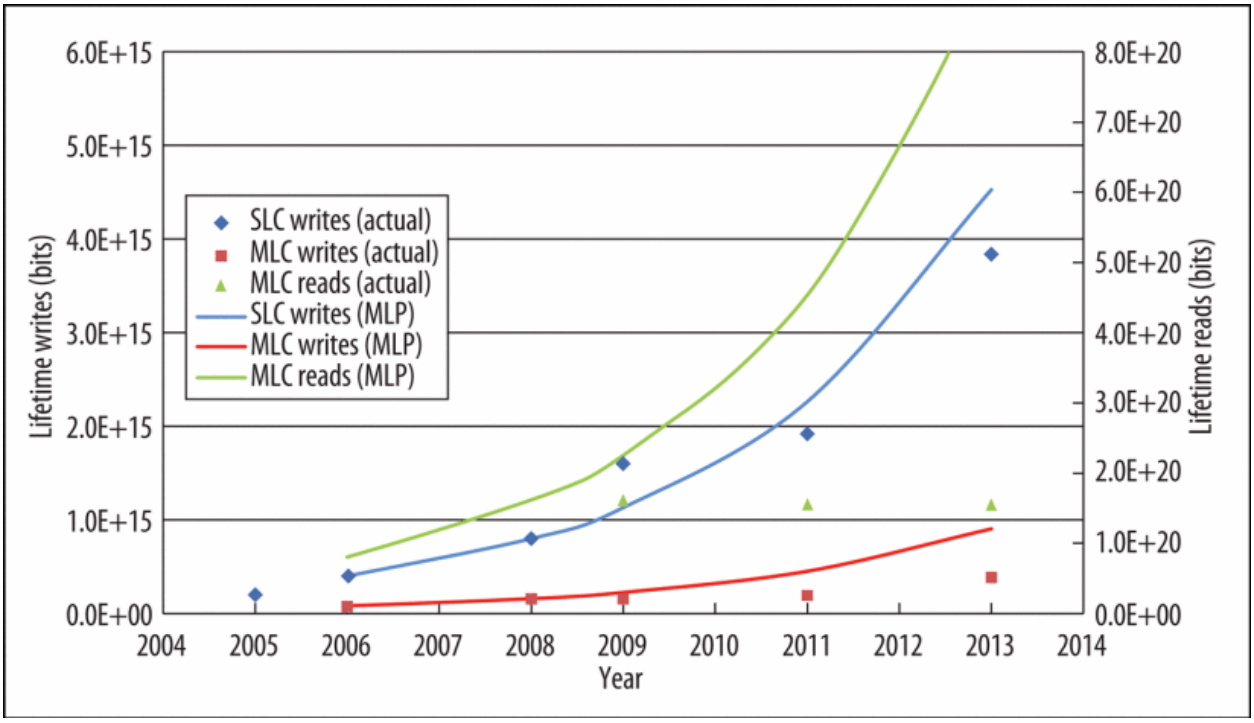

Figure 1. Graph showing the decline in usable read/write progress (MLP is Moore's Law Projection) [2]

These tradeoffs exemplify the general problem facing nanoelectronics; increased performance in one respect comes at the expense of decreased performance in another respect. At submicron levels, reading and writing to memory is a very sensitive endeavor, and these sensitivities are causing usable improvement in flash memory to nearly come to a halt. There are some potential technologies being researched that could continue some progress in flash memory such as phase change memory, resistive random access memory, and components that put more strain on well behaved read/write regions [2]. However, these options are unique to flash memory, and since they still follow the same general principles as their predecessors, they will eventually run into similar problems. To continue significant progress in computing long-term, the world will most likely need to turn to entirely new technologies such

as graphene and carbon nanotubes, quantum computing, spintronics, and optical computing, which will all be discussed in the following chapters.

Chapter 2

Graphene and Carbon Nanotubes

Graphene is a single layered sheet of carbon where the atoms are arranged in a hexagonal lattice. Each carbon atom has four valence electrons. For graphene, three of these electrons form sigma bonds with the neighboring atoms, leaving the fourth electron free to roam. Carbon nanotubes (CNTs) are essentially a sheet of graphene rolled into a tube. Carbon nanotubes can be single walled (SWNTs) or multi-walled (MWNTs). As you might be able to guess, SWNTs are a single layer of graphene rolled into a tube while MWNTs consist of multiple layers of graphene rolled into a tube. The behavior of SWNTs is dependent on how the hexagons in the graphene are aligned. The alignment of the hexagons is defined by the tube's two-dimensional (dimensions n and m) roll up vector which is defined as the tube's circumference in terms of 2 unit vectors which is demonstrated in the figure below [3].

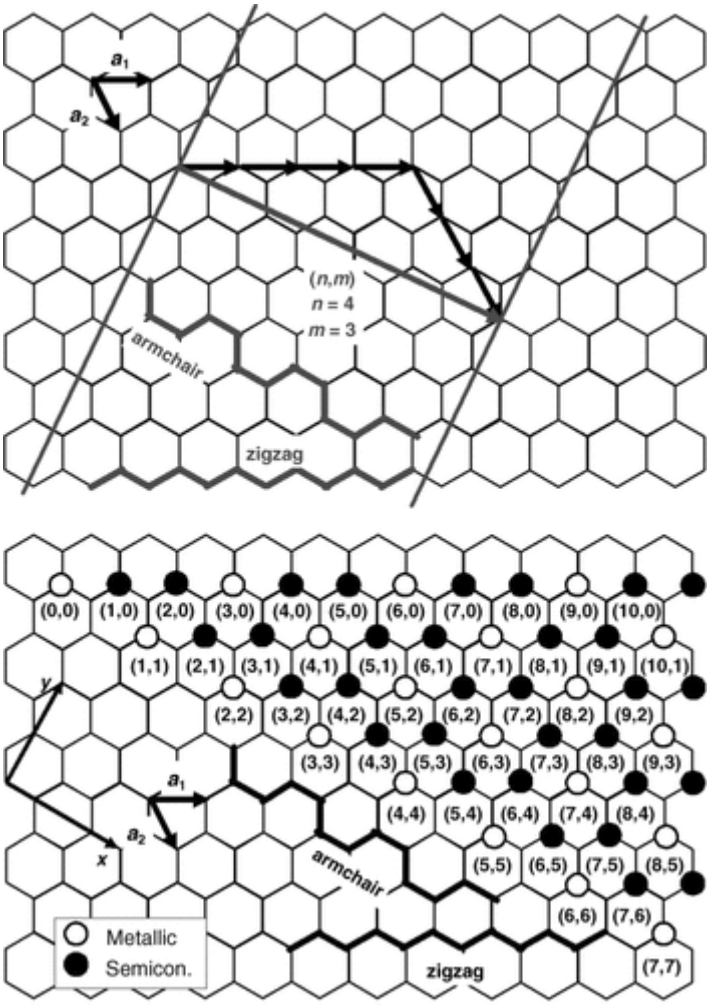

Figure 2. Rollout vector to classify CNTs [3]

If n = m, the hexagon alignment is known as "armchair," and the tube is metallic. If n or m = 0, the hexagon alignment is called "zig-zag," and the tube is semiconducting. Zig-zag tubes at fermi level E=0 have a density of states equal to zero meaning they are metallic while armchair tubes at fermi level E=0 have a density of states always above zero meaning they are semiconducting [3].

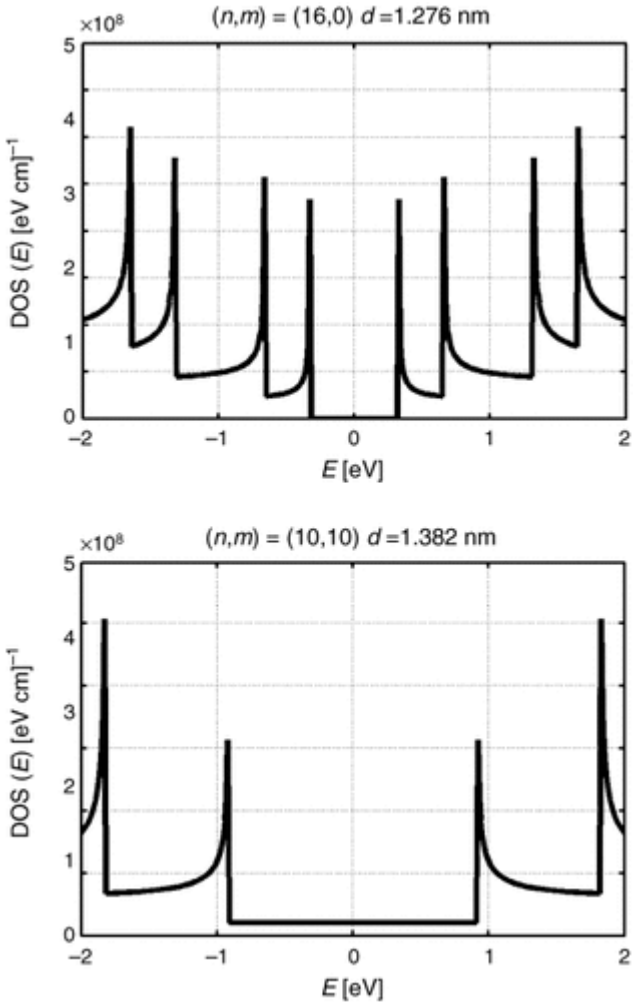

Figure 3. Density of states for zig-zag (top) and armchair (bottom) at different fermi levels [3]

More generally, the tube is metallic if (n-m)/3 is a whole number, and semiconducting otherwise. MWNTs are always metallic [3]. Important properties of CNTs for use in microelectronics are shown in the table below.

Table 1. Important Properties of CNTs [4]

Electrical Conductivity	Metallic or semiconducting
Electrical Transport	Ballistic, no scattering

Energy gap (semicond.)	E_g [eV]≈1/d [nm]
Maximum current density	~10$_{10}$ A/cm$_2$
Maximum strain	0.11% at 1 V
Thermal conductivity	6000 W/Km
Diameter	1–100 nm
Length	Up to millimeters
Gravimetric surface	>1500 m$_2$/g
E-modulus	1000 GPa

Applications of Graphene and Carbon Nanotubes

One potential way to capitalize on the unique properties of graphene and CNTs is to use them to replace the standard copper interconnects used in electronics today. Graphene and CNTs are well suited for interconnects because of their high current densities and thermal conductivities as shown in the table above. Comparing the values of CNT properties to standard copper interconnects, CNTs have a maximum current density nearly 1000 times higher and 10 times higher thermal conductivity [5].

Table 2. Comparing properties of Graphene and CNT to copper interconnects [5]

	Graphene	CNTs	Cu
Elec. conductivity (S cm^{-1})	$\sim 10^5$	$\sim 10^6$	$\sim 10^5$
Ther. conductivity (W m^{-1}K^{-1})	5300	> 6000	385
Max. current dens. (A cm^{-2})	10^8	10^9	$< 10^7$
Young's modulus (TPa)	1	1	0.13

One of the physical limitations of Moore's law is keeping heat dissipation up with the increasing density of devices and their now increasing power density. Therefore, CNTs and their higher thermal conductivity could potentially be a very useful tool in addressing the coming end of Moore's law. Also, with device miniaturization, classical copper interconnects have had to decrease in diameter, increasing their resistance and in turn limiting the amount of current they can transport. Again, using CNTs as interconnects can address the physical limitations of Moore's law because, due to their high current density, CNTs can be extremely thin and still carry enough current [5].

Another possible use for CNTs in microelectronics is in transistors. Initially, transistors known as CNTFETs were developed, consisting of one or multiple CNTs lying across the gate between the source and the drain, replacing the part of the silicon substrate that acts as the channel in MOSFET operation [4].

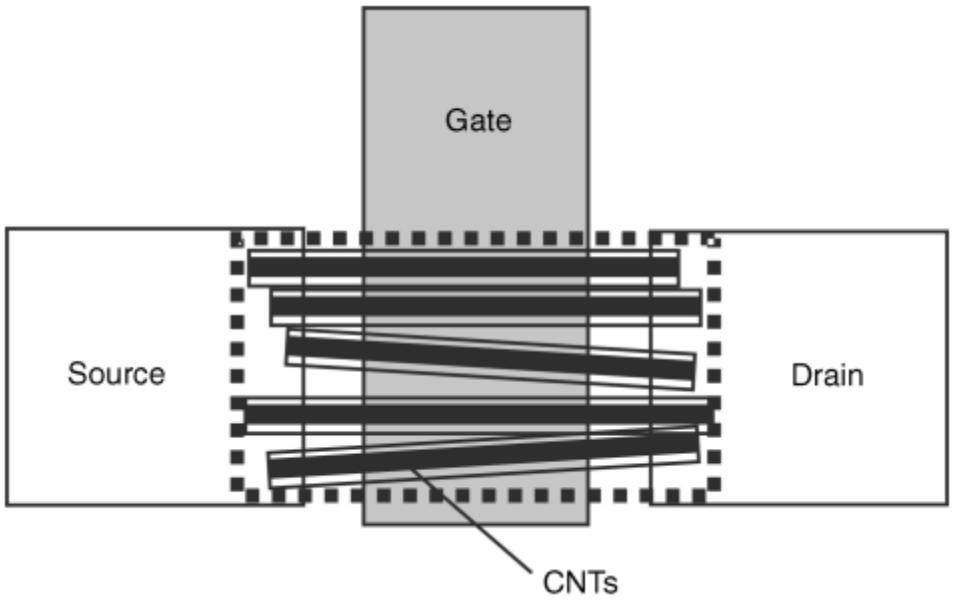

Figure 4. Implementation of a CNTFET [3]

Experimentally, these CNTFETs greatly outperform MOSFET transistors in key characteristics, as outlined in the table below.

Table 3. Properties of CNTFETs compared to MOSFETs and FinFETs [4]

	p-CNT FET 1.4 µm (1 V)	p-CNT FET 3 µm (1.2 V)	MOSFET 0.1 µm (1.5 V)	FinFET 10 nm (1.2 V)	MOSFET 14 nm (0.9 V)
Drive current Ids (mA/µm)	2.99	3.5	1.04 nFET 0.46 pFET	0.450 nFET 0.360 pFET	0.215 pFET
Transconductance (µS/µm)	6666	6000	1000 nFET 460 pFET	500 nFET 450 pFET	360 pFET
S (mV/dec)	80	70	90	125 101	71
On-resistance (Ω/µm)	360	342	1442 nFET 3260 pFET	2653 nFET 3333 pFET	4186 pFET
Gate-length (nm)	1400	2000	130	10	14
Normalized gate-oxide (1/nm)	80/1=80	25/8=3.12	4/2=2	4/1.7=2.35	4/1.2=3.33
Mobility ($cm_2/(Vs)$)	1500	3000	–	–	–
Ioff (nA/µm)	–	1	3	10	100

Notice the measurements are per gate length because CNTFETs are currently much longer than MOSFETs or FinFETs. Research is being conducted to find ways to shorten the tubes as this will not only help with improving these parameters but also potentially allow CNTFETs to surpass silicon devices in terms of operating frequency.

Researchers are looking into a conceptual CNT based transistor which would feature a construction in which the CNT is vertical between the source and the drain, and the gate and dielectric are coaxial can be seen below. This transistor design is known as the vertical CNTFET

or VCNTFET. This arrangement breaks the separation of the gate and electrodes free from the limits of lithography. It also allows for minimum transistor footprint and three-dimensional structures of transistors, helping improve device density [3].

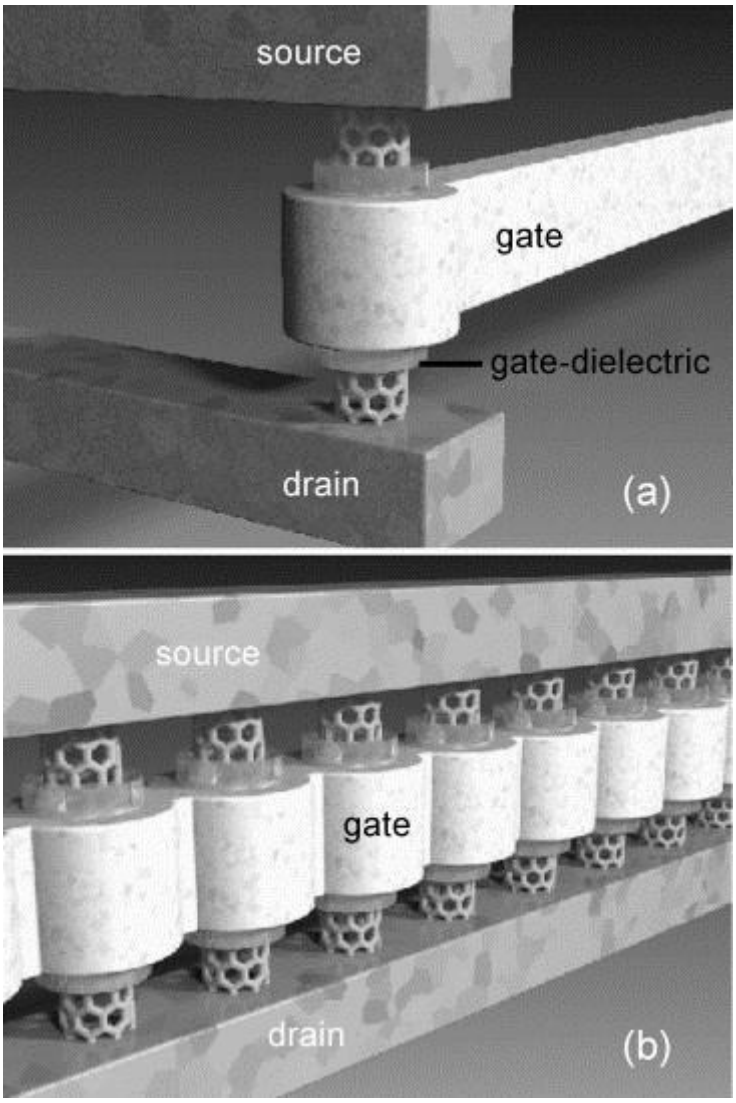

Figure 5. Vertical CNTFET configuration [4]

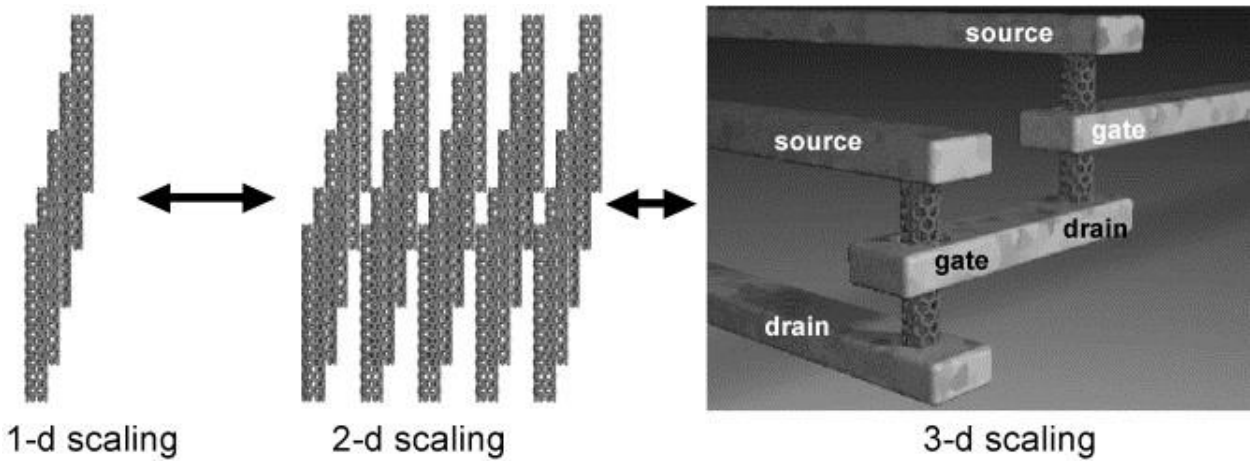

Figure 6. Multi-dimensional arrangements of VCNTFET [4]

Producing Graphene and Carbon Nanotubes

Originally, graphene was produced by exfoliating single layers from graphite, but this process has a limited yield and produces unfavorable shapes and orientations of the lattice. The most common method for commercially producing graphene is chemical vapor deposition (CVD). In this process, a metal substrate is exposed to a gas that is a precursor for graphene, such as methane, at high temperatures. The deposited graphene is then transferred to an insulating substrate to be used for microelectronic applications. However, during this transfer process, the graphene is susceptible to imperfections which affect its performance. To avoid this transfer process, graphene can be grown directly on a SiC substrate by heating the system (the substrate and precursor gas) to a high temperature in a vacuum then allowing the system to slowly cool while the graphene deposits. Although effective, this method is very expensive. CNTs can also be produced using CVD along with other methods such as electric arc discharge and laser ablation, but these methods are all too expensive for mass production. It is

worth noting that the production of MWNTs is more favorable than SWNTs because they are always metallic, and their growth is easier to control [5].

Limitations to Large Scale Implementation

In addition to the manufacturing difficulties mentioned in the section above, practical implementation of graphene is limited. The main limitation to unlocking the full potential of graphene and CNTs is the material surrounding them. For example, support material in CNT structures limits their carrier mobility by a factor of 5. Similarly, CNTs' conductivity is limited by the resistance of the materials that make up contact points [5].

Chapter 3

Quantum Computing

Quantum computing is probably one of, if not, the most talked about alternatives to classical computing, and its potential is certainly exciting. Classical computers work based on bits which can be switched between one of two states by a transistor: high (1) or low (0). Quantum computers use qubits made of fundamental particles that behave with quantum properties such as superposition. Due to superposition, these qubits can be in a state of limbo between a high state and a low state where these states are usually defined as the orientation of their spin with respect to a surrounding magnetic field. Superposition essentially states that there is a probability of the qubit being in the high state and a probability of it being in a low state, and this probability sums up to 1. When there are multiple qubits, their combined state is defined by 2^n factors. For example, with 2 qubits, there are 4 possibilities of spin

orientation defined by 4 probability coefficients, If there are 3 qubits, there are 8 possibilities with 8 coefficients, and so on. Comparing this to a classical bit, 2 bits are defined by 2 factors: the value of the bits themselves. This means that the number of factors required to describe a number of classical bits grows linearly while the number of factors required to describe a number of qubits grows exponentially [6], [7], [8].

Pros and Cons of Quantum Computing

Due to this larger number of factors, quantum computers are particularly useful for applications with large amounts of data and possibilities. For example, using complex algorithms based on the system of qubits' state probability constants, quantum computers can quickly solve problems in areas such as cryptography, optimization, data search, and simulating quantum systems that classical computers couldn't even solve [9]. A common method for solving these problems with large possible outcomes is a process called quantum annealing. Quantum annealing frames these problems as an energy optimization problem and finds the lowest possible energy state of the qubit system [10].

The large number of factors could also make quantum computers extremely useful for storing data. However, it is difficult to actually go back and read this data because to do so, the states of the qubits need to be defined and not probabilistic. This means that they lose their superposition and effectively function the same as classical bits [6], [9] .

This idea of qubits losing their superposition is called decoherence, and it is the main drawback of quantum computing. Other than specific applications such as the ones mentioned above (cryptography, optimization, etc.), quantum computing is not very useful because most applications of computers require the bits to end up in a determined state. Without the added

factors due to superposition, quantum computers perform equally or worse than classical computers. This greatly limits their potential applications. Additionally, to avoid decoherence, even in these specific applications, quantum computers need highly controlled environments making it nearly impossible to imagine them being used for desktop computing [9].

Chapter 4

Spintronics

Spintronics is the redesign of the classical computer using the spin of electrons rather than their charge. Spintronics has already had a significant impact in magnetic hard disk drives through giant magnetoresistive (GMR) spin valves. A spin valve consists of a thin non-ferromagnetic layer lying between 2 ferromagnetic layers. When the magnetic fields of the ferromagnetic layers lie in parallel, the valve is open with low resistance. If the fields are antiparallel the valve is closed with high resistance. Spintronics contribute by placing an electron atop the valve as a sensor of whether it is open or closed. These GMR spin valves have already been replaced by spin dependent tunneling devices, but this technology relies on electron spin as well [11].

Racetrack Memory

Another potential spintronics technology is racetrack memory. Racetrack memory utilizes sending spin current through a small magnetic passageway to switch the magnetization of an element. Racetrack memory is a non-volatile memory structure that stores data through the magnetic polarization of sections along a track. This memory system could eliminate the need for motors in disk drives and therefore eliminate crashes. As you can see in the figure, racetrack memory also could allow for 3-dimensional memory structures. Also, since each track has its own read/write device, racetrack read/write times can easily match up with current memory systems. There is even speculation that this technology could be used for logic

gates. Ultimately, spintronics seem very promising, but they are still in the very early phases of research and development, so only time will tell [11].

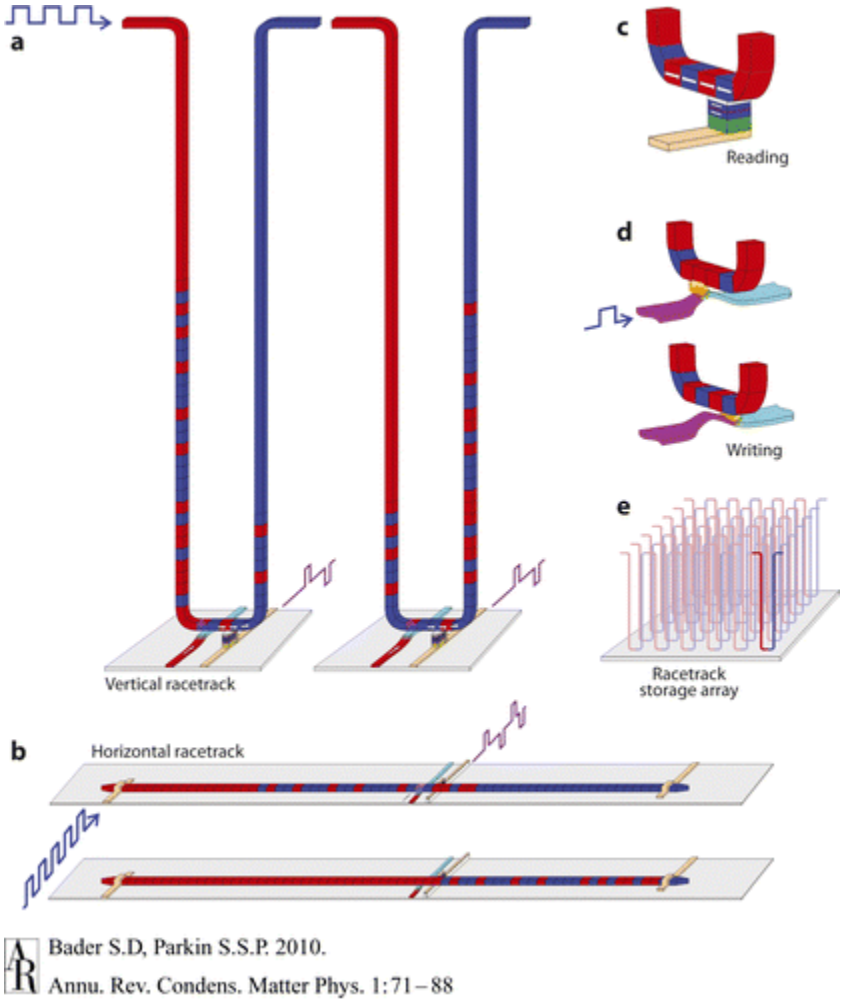

Figure 7. a and b show possible racetrack orientations, c and d show how the track reads and writes, and e shows how the tracks can be placed in arrays [11]

Chapter 5

Optical Computing

Optical computing functions based on light instead of electrons, and there are several different methods of optical and electro-optical computing. Some of these include optical pattern recognition, analog optical computation, digital optical computing, and multi-operand electro-optical computing. Digital optical computing and multi-operand electro-optical computing will be discussed in the following sections. Optical computing is promising because light travels much faster than electrons, meaning data can be transmitted much faster with optical computing. Additionally, optical computing has a much higher bandwidth and density, partially due to the fact that photons do not interact with each other the same way electrons do which allows for beams to pass across each other without losing their information. The two main limiting factors of optical computing are the complex computation process due to the many signals and the large size of experimental optical computing devices [12].

Digital Optical Computing

Digital optical computing is achieved by optically superimposing multiple input optical signals whose value is determined by their intensity. A binary 0 is defined by a low intensity and a binary 1 is defined as a high intensity. The combined signal goes to a nonlinear function which produces the binary output for the intended logic operation. This process can be seen in the figure below [13].

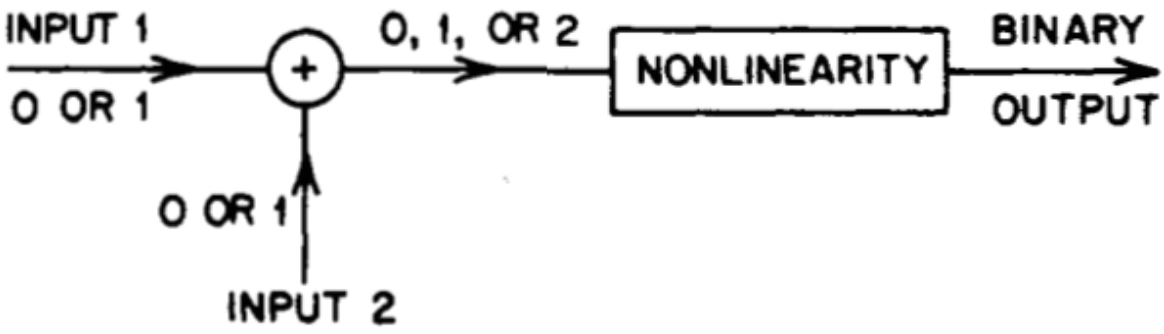

Figure 8. Block diagram showing how optical computing signals are processed [13]

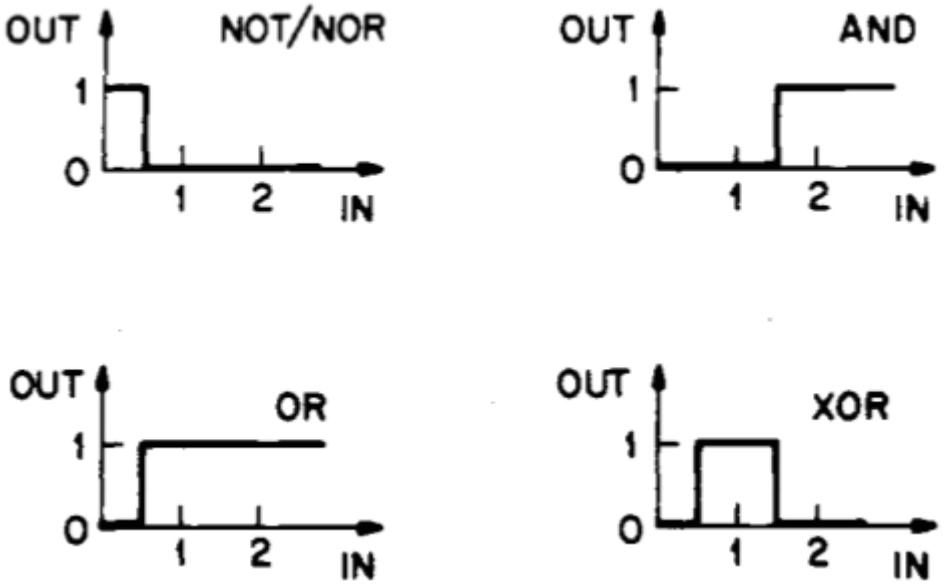

Figure 9. Ideal switching characteristics of above diagram [13]

However, the switching characteristics shown in the figure above are not realistic. The actual switching characteristics can be seen in the following figure. Region C is the preferred area of operation for digital optical computing because the output is only slightly dependent on the input. This means that the operation is not as heavily influenced by the operating environment [13].

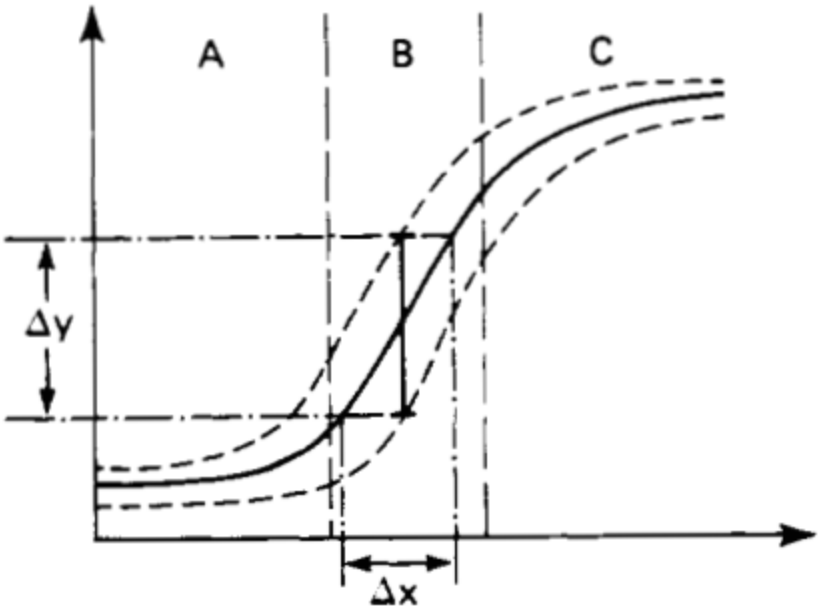

Figure 10. Actual switching characteristics of optical gate [13]

Digital optical computing is very promising, but it is limited by several challenges. One of the challenges is avoiding changes of state such as having to switch from electrons to photons and back to express signals. Another challenge is interconnection both between devices on a chip and from the chip to external systems [13].

Multi-Operand Electro-Optical Computing

Multi-operand electro-optical computing uses electrical signals to control an optical input and output using multi-operand logic gates (MOLGs). MOLGs consist of a micro-resonator controlled by multiple signals with different weights. The micro-resonators have a base operating wavelength, but as the input signals change, this wavelength changes. Each additional high input signal contributes to a redshift in the transmitted wavelength. The different weights are typically determined by the width of the active region of the section on the micro-

resonator. By adding weights, the number of possible functions greatly increases, similar to quantum computing [14].

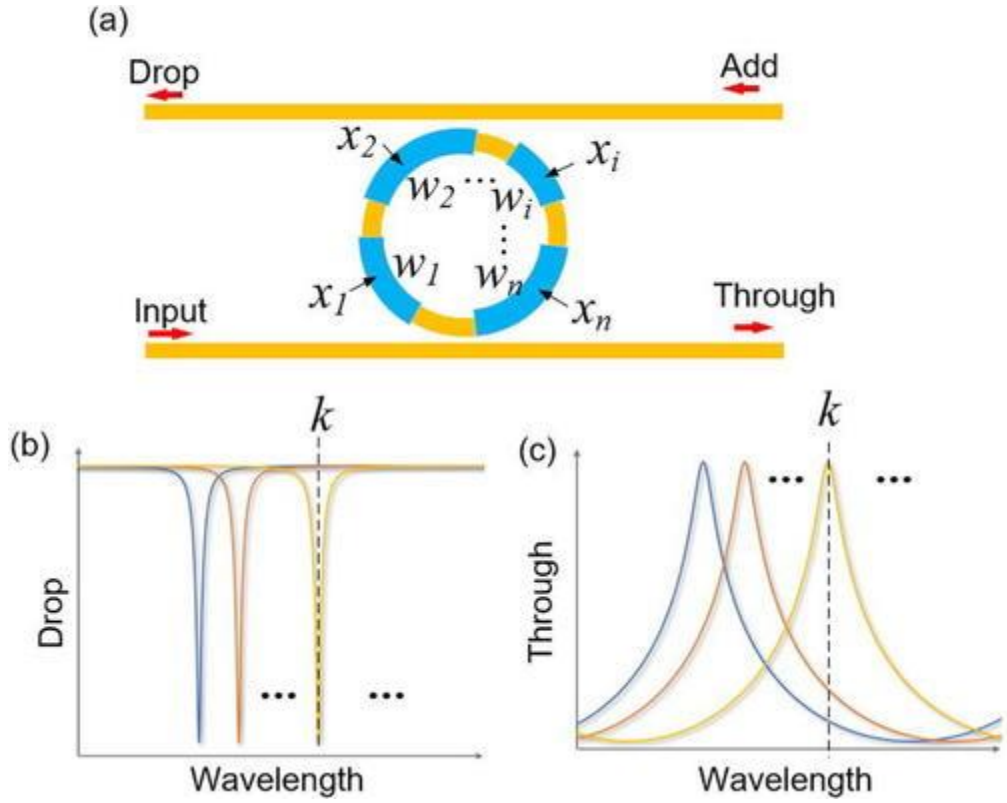

Figure 11. MOLG and its wavelength graphs [14]

The output is determined by a target wavelength k, which can only be achieved through a specific input. When wavelength k is met, the MOLG outputs 0. With n input variables, there are 2^n possible input combinations. When combined with the input weights, there are 2^2^n possible wavelengths [14]. The truth table for a MOLG can be seen below.

Table 4. Truth table for MOLG with n inputs [14]

	Input						Output
No.	x_1	x_2	...	x_i	...	x_n	y
1	x_{11}	x_{12}	...	x_{1i}	...	x_{1n}	y_1
2	x_{21}	x_{22}	...	x_{2i}	...	x_{2n}	y_2
...			...		...		...
j	x_{j1}	x_{j2}	...	x_{ji}	...	x_{jn}	y_j
...			...		...		...
2^n	$x_{2^n 1}$	$x_{2^n 2}$	...	$x_{2^n i}$	...	$x_{2^n n}$	y_{2^n}

The large number of possible functions leads to electro-optical computing being able to compute extremely quickly and efficiently compared to a classical computer. Logic functions can be solved using a fraction of the number of gates required by classical computing which saves time and area. For example, by using four-operand MOLGs $y = (a \oplus b) \cdot (c \oplus d)$ can be computed with only 16.6% of the gates required by classical computing. This leads to a 67% decrease in propagation latency and an 81% decrease in required area [14].

Chapter 6

Analysis

Clearly there are many options for continuing technological progress as Moore's Law begins to fail. Each of these options have their own benefits and drawbacks. Material solutions such as graphene and CNTs would allow for a pretty seamless transition but are currently limited in terms of mass production. Quantum computing and spintronics seem extremely promising for specific applications, but may not be of much help for more general use. Optical computing is very exciting because of its high speed and density, but it is still in the early stages of development.

Ultimately, I think a material solution is ideal for the short term because it would require very little overall redesign of technological systems since they would still function based off of the same principles, just with different materials. The potential improvements from a material based solution such as graphene and CNTs would be able to affect the microelectronics industry as a whole instead of specific devices and applications. On the other hand, since these solutions would still be using the same general principles, they will eventually run into the same problems currently being experienced. In the long term, I think optical computing has the most potential. This is because it has the potential to improve many different computing applications and avoids the problems associated with using electrons by using light instead.

Chapter 7

Conclusion

In this paper, we covered the constraints contributing to the slowing and eventual end of Moore's Law as well as several potential emerging technologies that could aid in overcoming these constraints. These solutions included the use of graphene and CNTs, quantum computing, spintronics, and optical computing. Comparing the pros and cons of each of these technologies, I believe that optical computing has the most potential long term, and CNTs will be useful in maintaining progress until optical computing is ready to be used at a large scale. The other solutions (quantum computing and spintronics) are still worthwhile due their excellence in specific applications. Although it may be scary facing the end of an era of unbelievable technological progress, we should be excited to see what the future holds for microelectronics.

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ACADEMIC VITA

John B. O'Toole, Jr.

EDUCATION

PENN STATE UNIVERSITY, Schreyer Honors College, *State College, PA*

Studying for Bachelor of Science in Electrical Engineering, anticipated graduation May 2023

- Achieved Dean's List in 7 semesters: Fall 2019 through Fall 2022
- Earned President's Freshman Award, Fall 2019

WORK EXPERIENCE

Potomac Electric Power Company (PEPCO), Washington, DC

Maryland Capacity Planning Intern (June 2022 - August 2022)

Completed weekly outages and overload reports, and performed technical analysis for solar installation projects

College Hunks Hauling Junk and Moving, *Annapolis, MD*

TRUCK CAPTAIN (June 2020-August 2020)

Promoted to Truck Captain within two weeks of employment; calculated the estimated cost for customer, managed the team assigned to job, and ensured customer satisfaction

EXTRACURRICULAR ACTIVITIES

PENN STATE THON, (Fall 2019 - Present)

Family Relations Chair (2021-2022) - Created fun memories and lasting relationships by coordinating events and provided assistance to organization's adopted family who has been personally affected by childhood cancer

Head Chair (2022 - Present) - Lead organization by coordinating fundraising events and promoting active membership

PENN STATE MEN'S RUGBY TEAM (Fall 2019 - Present)

Learning teamwork, leadership, and communication skills while competing in sport I love

- Selected to tour with the U18 junior national team in Canada and train with the U20 and U23 junior national teams in 2019, 2021, and 2022 respectively
- Named 2019 D1A All-Freshman 1st team, 2019 Rugby East All-Conference 2019, and 2021 National Collegiate Rugby All-American