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A Novel mmWave Down-Conversion Mixer Design for 5G FR2 Communication

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ABSTRACT

The Gilbert cell mixer is one of the most popular circuit topologies for frequency down-conversion in modern wireless networks. The topology is not well suited to the performance demands of some wireless networks in the mmWave spectrum, however, as it exhibits an inherent trade-off between linearity and DC power consumption. This work proposes an alternative mixer topology for mmWave down-conversion that overcomes this trade-off, enabling highly linear operation in nearly every 5G FR2 band. Over its RF bandwidth, the mixer proposed in this work exhibits a conversion gain above 0 dB, an IP1dB above 0 dBm, and an OP1dB above 0 dBm while limiting DC power consumption to 42 mW.

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Chapter 1

Introduction

1.1 5G NR Background

5G New Radio (NR) is a set of global standards concerning the air interface of fifth-generation (5G) wireless communication networks. Developed by the 3rd Generation Partnership Project (3GPP), the 5G NR standards employ software and algorithmic innovations that enable more efficient data transfer between devices and the use of a greater diversity of frequency bands than previous generations of cellular communication technology [1]. These innovations promise increased data rates, decreased network latency, and improved performance in high-traffic areas for users of 5G wireless networks [1].

The frequency bands supported by 5G NR fall into two main subdivisions: Frequency Range 1 (FR1) and Frequency Range 2 (FR2). FR1 consists of frequency bands ranging from 415 MHz to 7.125 GHz. FR1 contains many of the bands supported by previous cellular communication standards while also supporting new regions of the radio spectrum to handle increased network traffic [2]. FR2 consists of much higher frequencies than FR1, containing bands ranging from 24.25 GHz to 71 GHz. Electromagnetic (EM) waves at FR2 frequencies are characterized as millimeter-wave (mmWave) signals, as their free-space wavelengths are on the order of several millimeters.

The frequency bands in FR2 are much more sparsely allocated and have much higher bandwidths than those in FR1. Additionally, FR2 frequencies are utilized for cellular communication quite sparingly compared to FR1 frequencies [2]. FR2 thus contains abundant

and largely untapped available bandwidth, which can be used to enable higher network speeds and improved traffic handling capabilities. The immense available bandwidth of FR2 makes it an attractive candidate for the operating frequency of many novel wireless communication technologies.

1.2 mmWave Design Challenges

Despite its large available bandwidth, the mmWave spectrum presents many circuit-level and system-level design challenges, which is why this frequency range is not yet heavily utilized for wireless cellular communications [3]. At a circuit level, impedance matching and circuit layout geometry considerations are critically important for successful mmWave design, as parasitic effects and unwanted reflections can significantly degrade circuit performance [4]. Additionally, the transistors that make up active devices can see significant performance reduction at high frequencies, which must be accounted for [5].

At a system level, mmWave signals exhibit high path loss, as mmWave EM waves attenuate more quickly in Earth's atmosphere than many lower-frequency EM waves [3], [6]. This trend is depicted in Figure 1. Additionally, due to their short wavelengths, mmWave signals do not diffract around large obstacles, meaning they can be easily obstructed [3], [6]. As a result, mmWave transmitters and receivers must remain in an unobstructed, line-of-sight configuration to maintain a connection [3]. These constraints limit the mmWave spectrum to short-range applications, such as densely populated urban areas or backhaul links between cell towers [3], [7].

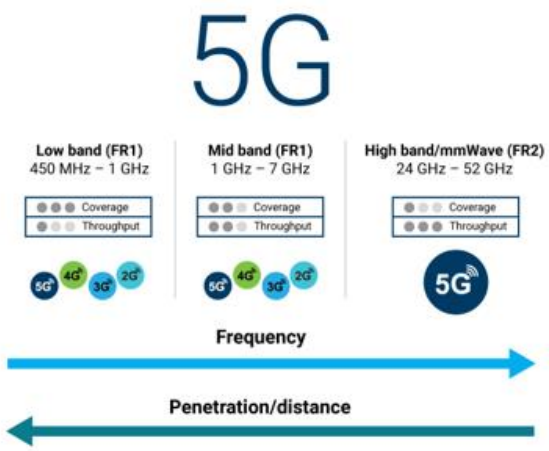

Figure 1. Trade-off between carrier frequency and coverage range for 5G NR bands [6]

1.3 Project Motivation

As the mmWave spectrum becomes more accessible and better characterized, it may be useful to have access to an integrated transceiver system that can operate in all or nearly all 5G FR2 bands [8]. Such a system would be characterized as multiband, as it would support many different bands, or standards, within FR2 [8]. Ideally, this system would also be easy to use and minimize the need for off-chip components, enabling easy access to vast swaths of the mmWave spectrum. The goal of this project is to design an integrated circuit (IC) that will serve as the frequency down-conversion block of the receiver (Rx) path for a multiband mmWave transceiver. This frequency down-conversion circuit is designed to have an operating bandwidth of 24 GHz to 50 GHz, covering nearly all the allocated 5G FR2 bands. Additionally, the circuit is optimized to exhibit highly linear operation. This is desirable because, in some modern mmWave transceiver systems, the use of phased arrays and the presence of interferers can expose mixers to large input power levels up to 15 dBm [9].

The circuit is designed using the GlobalFoundries 8XP 130 nm BiCMOS Process Design Kit (PDK). This process was chosen for two reasons. First, it provides access to both bipolar transistors and CMOS transistors, enabling a wider variety of circuits that can be designed [10]. The CMOS transistors are useful for switches and digital logic circuits, while the bipolar transistors exhibit high gain and are useful for analog applications [10]. Second, the bipolar transistors provided by the process are SiGe heterojunction bipolar transistors (HBTs), which exhibit strong high-frequency performance, making them suitable for mmWave applications [10].

Chapter 2

Technical Background

2.1 Basic Mixer Operation

A mixer is a device that mediates frequency conversion in a radio-frequency (RF) transmitter or receiver. The device contains three ports: a high-frequency RF port, a low-frequency intermediate-frequency (IF) port, and a local oscillator (LO) port. Each of these ports is associated with an electrical signal that oscillates at a specific frequency or range of frequencies. In a down-conversion mixer, the RF and LO signals are taken as inputs. The mixer then produces a signal with two frequency components at the third port: one frequency component is the sum of the RF and LO frequencies, and the other is the difference between the RF and LO frequencies. In down-conversion, the high-frequency component at the output is suppressed via a low pass filter (LPF), and the low-frequency component is taken to be the IF output. This scheme is depicted in Figure 2.

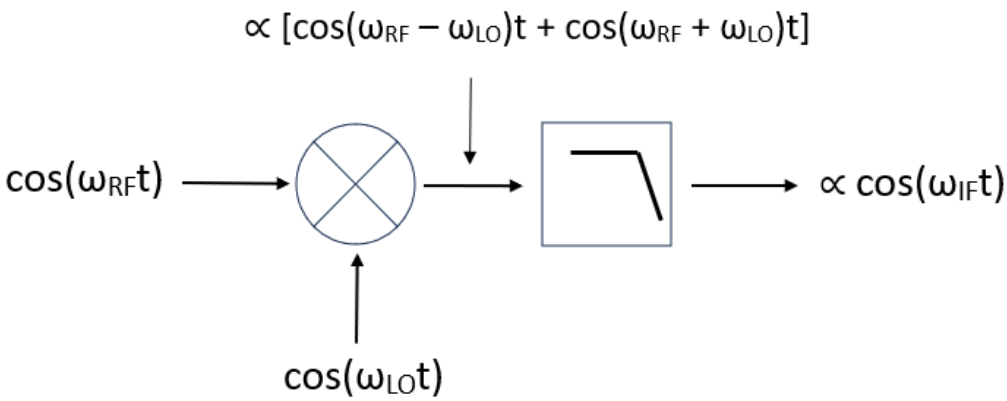

Figure 2. Principle of operation for down-conversion mixer

An up-conversion mixer admits the IF and LO signals and inputs. Similarly to the down-conversion mixer, it produces two frequency components at the output: the sum of the LO and IF frequencies and the difference between the LO and IF frequencies. The low-frequency component is suppressed at the output via a band pass filter (BPF), and the high-frequency component is taken to be the up-converted RF output. This scheme is depicted in Figure 3. In both mixer types, the IF frequency is the difference between the RF frequency and the LO frequency.

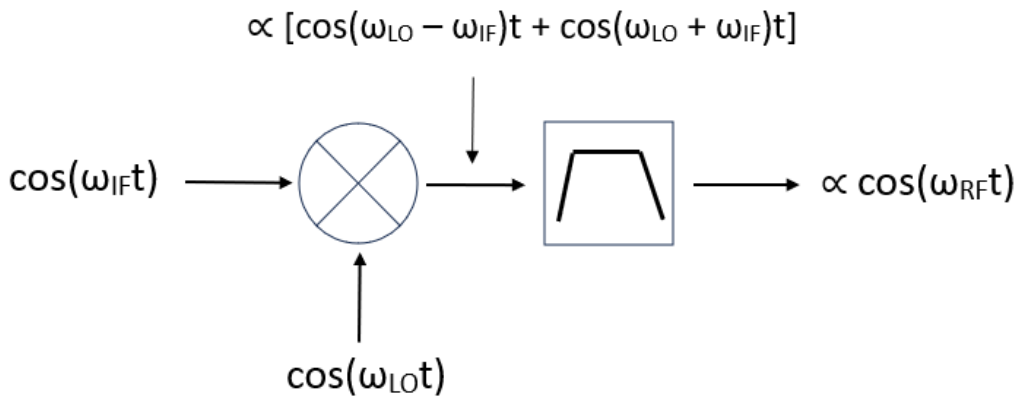

Figure 3. Principle of operation for up-conversion mixer

2.2 Mixer Characterization

In this thesis, the performance of different mixer designs is compared using the following metrics: conversion gain, bandwidth, linearity, noise figure, and DC power consumption. Conversion gain is the ratio of the output power at the desired output frequency to the input power at the corresponding input frequency, measured in dB. In down-conversion, for an input RF power of P_{RF} and a corresponding output IF power of P_{IF}, the conversion gain (CG) is given by Equation (2.1).

$$CG = 10\log\left(\frac{P_{IF}}{P_{RF}}\right) \qquad (2.1)$$

Voltage conversion gain (VCG) is the ratio of the output voltage amplitude at the desired output frequency to the input voltage amplitude at the corresponding input frequency, measured in dB. In down-conversion, for an input RF voltage amplitude of V_{RF} and a corresponding output IF voltage amplitude of V_{IF}, the conversion gain (CG) is given by Equation (2.2).

$$VCG = 20\log\left(\frac{V_{IF}}{V_{RF}}\right) \qquad (2.2)$$

Linearity characterizes the maximum input and output power levels a mixer can tolerate before its conversion gain begins to degrade. Figure 4 depicts the general shape of a plot of output power vs. input power applicable to both mixers and amplifiers. At low input powers, device output power increases linearly with input power. At high input powers, the curve flattens, and the output power ceases to change with input power. This corresponds to the active components within the device saturating and being unable to produce any additional power at the output. The input power level at which the power gain drops to 1 dB below the small-signal gain is termed IP1dB; the output power level at which this happens is termed OP1dB.

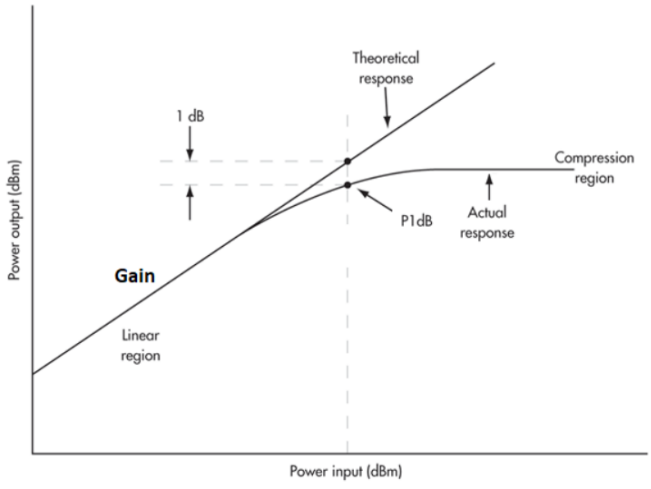

Figure 4. Output power vs. input power for a generic amplifier or mixer [11]

The mixer noise figure measures the amount of noise present at the mixer output port that was not present at the input port. In other words, it characterizes the amount of noise added to the signal of interest by the circuitry within the mixer. A mixer's noise factor (F) is the ratio of the signal-to-noise ratio present at its output (SNR_{out}) to the signal-to-noise ratio present at its input (SNR_{in}). This is expressed in Equation (2.3). The mixer's noise figure (NF) is simply the noise factor expressed in dB, as expressed in Equation (2.4). A noise figure of 0 dB is perfect, as this corresponds to zero noise contribution from a device's internal circuitry. This is impossible to achieve in practice, but mixer noise should be as low as possible to ensure reliable performance. DC power consumption simply refers to the product of the supply voltage applied to a mixer and the amount of current it draws. This value should be minimized.

$$F = \frac{SNR_{out}}{SNR_{in}} \qquad (2.3)$$

$$NF = 10\log(F) \qquad (2.4)$$

2.3 Gilbert Cell Background and Limitations

A common circuit implementation of a mixer is the Gilbert cell. A simplified schematic of a Gilbert cell mixer is depicted in Figure 5. The circuit consists of three main parts: a transconductance stage, a mixing quad, and a load impedance [12]. In Figure 5, the transconductance stage consists of two NMOS transistors biased in the common-source configuration, and the mixing quad consists of four transistors, which function as RF switches. The load in Figure 5 consists of two resistors between the mixing quad and the voltage supply, but the load can contain inductive and capacitive elements as well. When the Gilbert cell mixer is implemented for down-conversion, the RF input signal is applied differentially to the

transconductance stage, while the LO signal is applied differentially to the mixing quad. The output is taken differentially between the mixing quad and the load.

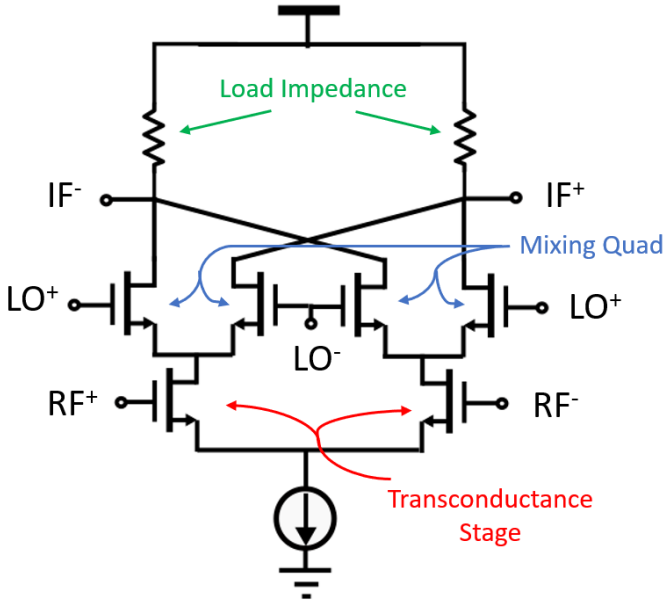

Figure 5. Simplified schematic of Gilbert cell mixer implemented for down-conversion.

The Gilbert cell mixer operates similarly to a standard common-source or common-emitter differential amplifier, but it provides a time-varying gain to the input RF signal instead of a constant gain [13]. This is because the oscillation of the LO signal causes each of the transistors in the mixing quad to alternate between a conducting (ON) state and a non-conducting (OFF) state at the LO frequency [13]. This causes the impedance presented to each branch of the transconductance stage to oscillate at the LO frequency. The gain of a common-source or common-emitter differential amplifier is directly proportional to the impedance presented to the output of the transconductance stage, so the gain provided to an input RF signal in a Gilbert cell mixer oscillates at the LO frequency.

The time-varying gain of the Gilbert cell transconductance stage produces an output waveform proportional to the product of the LO and RF waveforms [13]. The two most dominant frequency components in this output waveform are the sum of the RF and LO frequencies and the difference between the RF and LO frequencies [13]. The smaller of these two frequency components corresponds to the desired IF signal, so applying a low-pass filter at the mixer output allows the IF signal to be recovered. This is consistent with the operating principle of a down-conversion mixer shown in Figure 2. The theoretical conversion gain of a Gilbert cell mixer is given by Equation (2.5), where g_m is the transconductance of the transistors in the transconductance stage and R_L is the load resistance [13].

$$CG = \frac{2}{\pi} g_m R_L \qquad (2.5)$$

The Gilbert cell mixer topology enables a compact IC layout, good common-mode noise rejection, high isolation between ports, and strong rejection of undesired harmonics at the output, making it a popular circuit topology for frequency conversion [12], [13], [14]. Despite its advantages, however, the Gilbert cell introduces a trade-off between linearity and DC power consumption. For a mixer to exhibit high linearity, it should tolerate large signals at its input and output nodes without signal distortion or gain compression. One mechanism for signal distortion is when the output voltage clips against the supply voltage. As can be seen in Figure 6, if the voltage at one of the output nodes rises above its DC level by more than $\frac{I_{bias}R_L}{2}$, it will clip against the supply voltage.

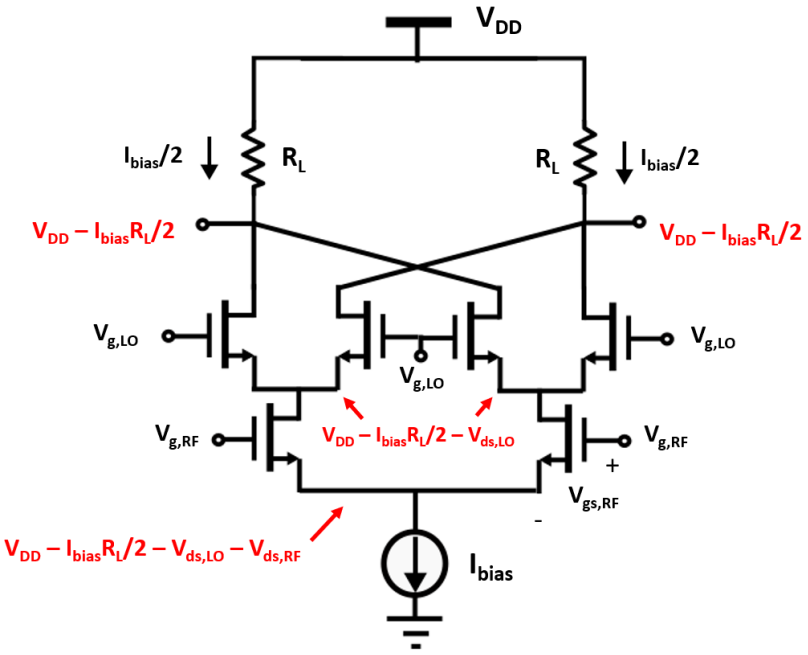

Figure 6. DC operating point of a Gilbert cell mixer.

Gain compression can occur if the input or output signal becomes large enough that it causes the transistors in the transconductance stage to periodically leave the saturation region and enter the triode region or cutoff region, as the gain supplied by the transistors will degrade in these regions of operation due to a reduced g_m. There are two ways this could occur. First, if the input signal is large enough to cause $V_{gs,RF}$ to periodically drop below the transistor's threshold voltage, the transistor will periodically enter the cutoff region, causing gain compression. Second, during a large swing in the output signal, the current in one of the branches of the Gilbert cell may become large enough to reduce $V_{ds,RF}$ to a value below $V_{gs,RF} - V_t$, where V_t is the threshold voltage. This would cause the transistors in the transconductance stage to periodically enter the triode region, leading to gain compression.

Taking these considerations into account, increasing the linearity of a Gilbert cell amounts to optimizing its DC bias point such that the input and output nodes have as much

voltage headroom as possible for signal oscillation. This involves simultaneously ensuring that the DC value of $V_{ds,RF}$ is large relative to $V_{gs,RF} - V_t$ and that $\frac{I_{bias}R_L}{2}$ is large enough to enable appreciable output voltage swing. If it is desired to keep the conversion gain of the Gilbert cell constant, R_L should be held constant, meaning that the only way to increase both $V_{ds,RF}$ and $\frac{I_{bias}R_L}{2}$ is to increase both the supply voltage and the bias current. This results in increased DC power consumption, illustrating the trade-off between linearity and DC power consumption for a standard Gilbert cell mixer. This thesis proposes a mixer design that overcomes this trade-off while maintaining the other performance advantages of the Gilbert cell mixer.

Chapter 3

Proposed Design

3.1 Design Overview and Block Diagram

To combat the trade-off between linearity and DC power consumption in the Gilbert cell mixer, this work proposes an alternative circuit topology whose block diagram is depicted in Figure 7. The circuit consists of a passive mixer based on high-linearity RF switches followed by a transimpedance amplifier (TIA) with resistive feedback.

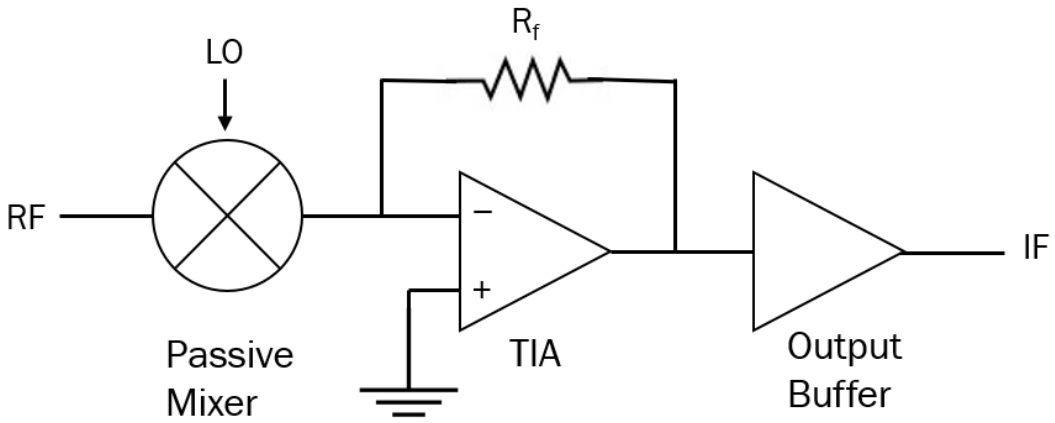

Figure 7. Block diagram of proposed mixer topology.

The passive mixer operates similarly to the mixing quad of the Gilbert cell, but it is not preceded by a transconductance stage. Like the mixing quad of the Gilbert cell, the passive mixer consists of a network of RF switches that oscillate between a conducting state and a non-conducting state at the LO frequency. This presents a time-varying impedance to the RF input port, producing a signal at the IF output with the frequency content of the product of the RF and LO waveforms, allowing the desired IF signal to be extracted. Unlike the Gilbert cell, the passive

mixer exhibits conversion loss instead of conversion gain, as the RF signal is subjected to resistive losses in the switching transistors without first being amplified by a transconductance stage.

To offset the conversion loss of the passive mixer, a differential TIA with feedback resistance is placed at the mixer output. Because the passive mixer consists of switches, signals travel through it in the form of currents. The TIA converts these currents at the mixer output to a useful voltage from which the IF signal can be recovered. Due to its feedback resistance, the TIA presents a smaller input impedance than a typical transconductance stage in a differential amplifier or a Gilbert cell. This simplifies broadband interstage matching between the mixer and the TIA.

The topology proposed in this work offers two primary advantages over the Gilbert cell. First, the new topology exhibits much higher linearity than a standard Gilbert cell for a given DC power consumption. The maximum allowable voltage swing at the input of the passive mixer is not limited by DC biasing constraints, so it can be exposed to much higher input power than the transconductance stage of a Gilbert cell [9], [15]. Also, the conversion loss of the passive mixer relaxes the linearity requirement for the TIA. Second, the passive mixer exhibits a smaller input impedance than the Gilbert cell at mmWave frequencies, making it feasible to achieve strong reactive input matching over a large RF bandwidth. Reactive input matching is demonstrated for the passive mixer in Chapter 4.

3.2 Passive Mixer

The passive mixer implemented in this work adopts a design based on high-linearity CMOS RF switches. The mixer is implemented in a differential topology to improve port-to-port isolation and noise performance, so the input RF signal is applied differentially across two paths connected in parallel. A Cadence Virtuoso schematic of one of these paths is shown in Figure 8. Each path consists of an NMOS transistor and a PMOS transistor connected in parallel. The source and drain of each of these transistors are biased at 0.6 V, corresponding to half the supply voltage for which the transistors are rated (1.2 V). The LO signal is applied to the gates of the transistors in the form of two square waves 180° out of phase with each other, each with a minimum value of 0 V. This biasing and LO distribution scheme serves several purposes. First, it ensures that both transistors oscillate between a conducting and non-conducting state in phase with each other. This enables them to turn on and off at the same time, allowing them to work together as a single switching device. Second, it simplifies the design of LO generation circuitry, as negative voltages are not required. Finally, it significantly reduces LO leakage at the output port. This is because the two transistors receive the LO signal 180° out of phase with each other, so any LO frequency components produced at the sources or drains of the transistors cancel out.

The transistors in the passive mixer are sized to ensure both high linearity and minimal conversion loss. A high width-to-length ratio is desired for each of the MOSFETs to ensure low channel resistance and the ability to handle large currents [16]. This minimizes resistive losses incurred in the transistors, improving conversion loss and linearity [16]. If the transistors are too large, however, parasitic gate capacitance and reduced switching speed can degrade the passive mixer's performance [9], [15]. Linearity and conversion loss simulations were conducted to determine the optimal size for each transistor. The dimensions of each transistor type in the

schematic, along with other passive component values, are given in Table 1. The NMOS and PMOS transistors are sized slightly differently so that both transistor types have similar gate capacitance and threshold voltage magnitude. This was done to ensure each complementary pair switches on and off as simultaneously as possible to reduce distortion.

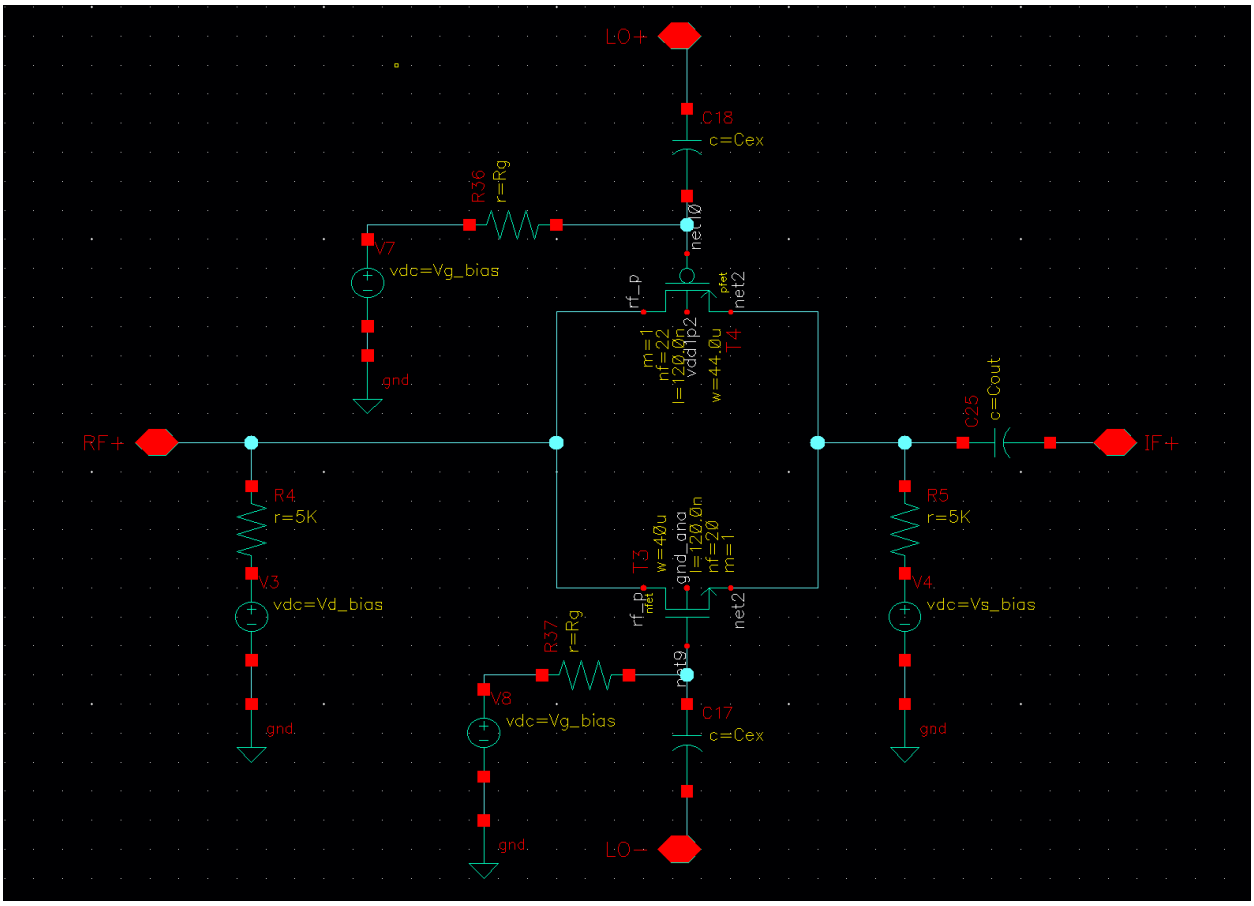

Figure 8. Passive mixer schematic.

An external capacitor (C_{ex}) is placed at the gate node of each transistor in the passive mixer to enable high linearity over large LO and RF bandwidths. The voltage present at the gate of an RF switch can be modeled by a transfer function that depends on the applied RF and LO voltages, the gate capacitance of the switching transistor, and the external impedance placed at the gate node [9], [15]. Using a capacitor for the external impedance makes this transfer function

frequency-independent, ensuring non-degrading performance over much larger LO and RF frequency ranges [9].

Table 1. Passive mixer component parameters.

Parameter	*Value*
PMOS Transistor W/L	44 µm / 120 nm
NMOS Transistor W/L	40 µm / 120 nm
C_{ex}	250 fF
C_{out}	10 pF
R_g	1 kΩ

3.3 Transimpedance Amplifier

The transimpedance amplifier interfaced with the output of the passive mixer takes the form of a cascoded differential common-emitter amplifier with resistive feedback. The schematic of the TIA is shown in Figure 8. The TIA employs a cascode stage to improve bandwidth and input-output isolation [17]. The TIA is loaded with a PMOS current source, presenting a large resistance to give the TIA a large open-loop gain. The current source load also presents a small parasitic capacitance, which helps to attenuate frequency components that are much larger than the IF frequency. The TIA uses a supply voltage of 2.1 V and draws about 5 mA of current, consuming about 10.5 mW of power.

The gain of the TIA is tunable based on the choice of feedback resistor R_f. Because the open-loop gain of the TIA is large, it can be modeled as an operational amplifier (op-amp) with a

differential output, as shown in Figure 9. In the figure, a differential current I is applied across the input terminals of the op-amp, producing an output voltage V_o. Kirchhoff's current and voltage laws reveal the relation $\frac{V_o}{I} = 2R_f$, which implies that increasing R_f increases the gain of the TIA. The transistor dimensions and passive component values in the TIA are given in Table 2.

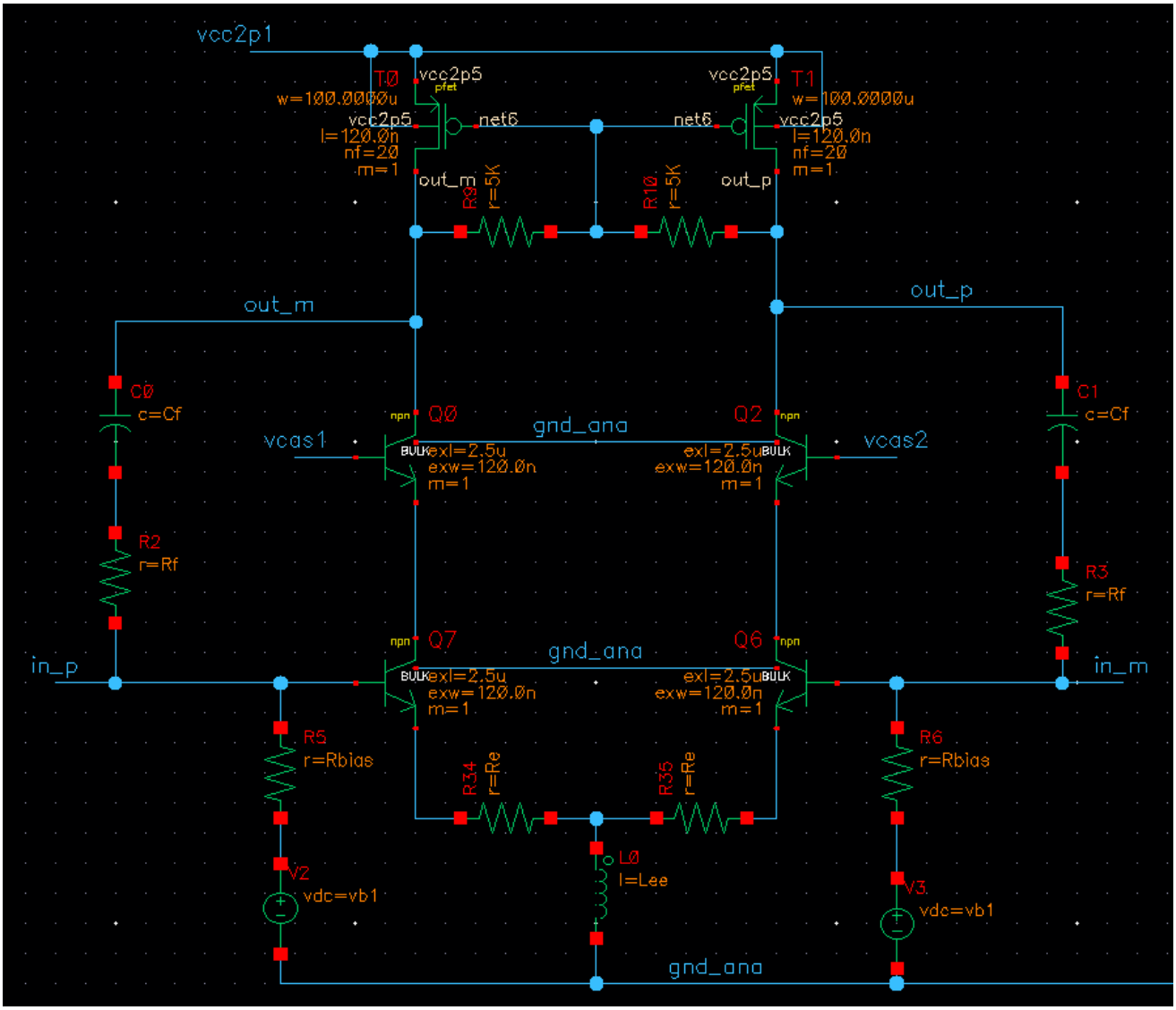

Figure 9. Transimpedance amplifier schematic.

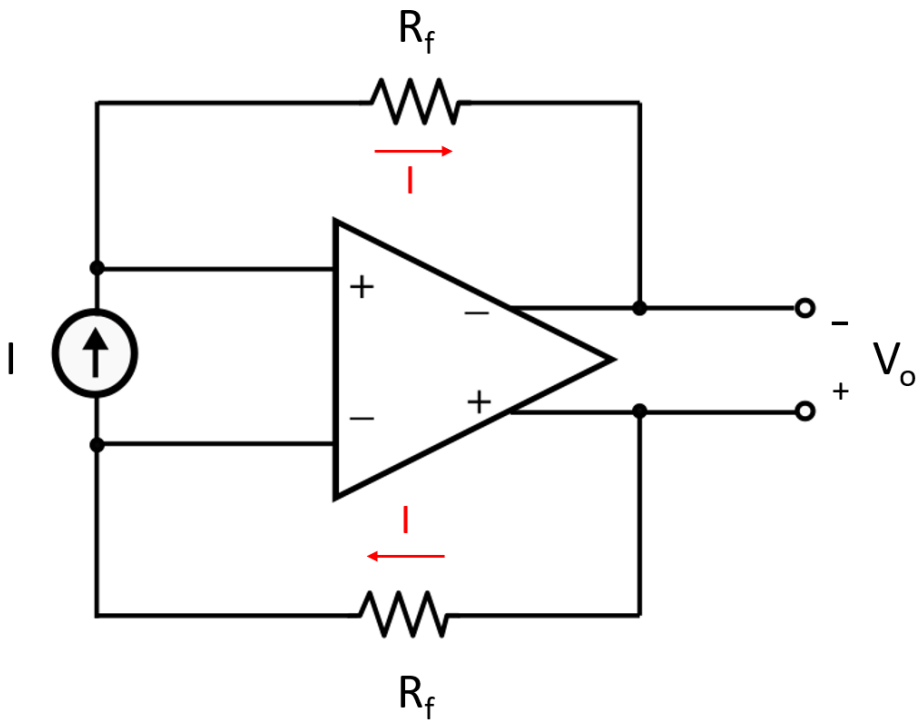

Figure 10. Model for differential transimpedance amplifier with feedback resistance.

Table 2. Transimpedance amplifier component parameters.

Parameter	*Value*
PMOS Transistor W/L	100 µm / 120 nm
SiGe HBT Emitter L/W	2.5 µm / 120 nm
R_f	250 Ω
R_e	10 Ω
R_{bias}	5 kΩ
C_f	10 pF
L_{ee}	5 nH

3.4 Output Buffer

For the mixer to drive a 50-Ω load, the TIA output must be interfaced to an output buffer capable of producing appreciable output power. The schematic for such a buffer is shown in Figure 10. The buffer adopts a differential common-emitter topology with an inductive load and both resistance and inductive emitter degeneration. The buffer is biased so that its input can be coupled directly to the TIA output without the need for DC-level shifting. The output buffer uses a 2.1 V supply voltage and draws about 15 mA of current, consuming about 31.5 mW of power. Transistor dimensions and passive component values are given in Table 3.

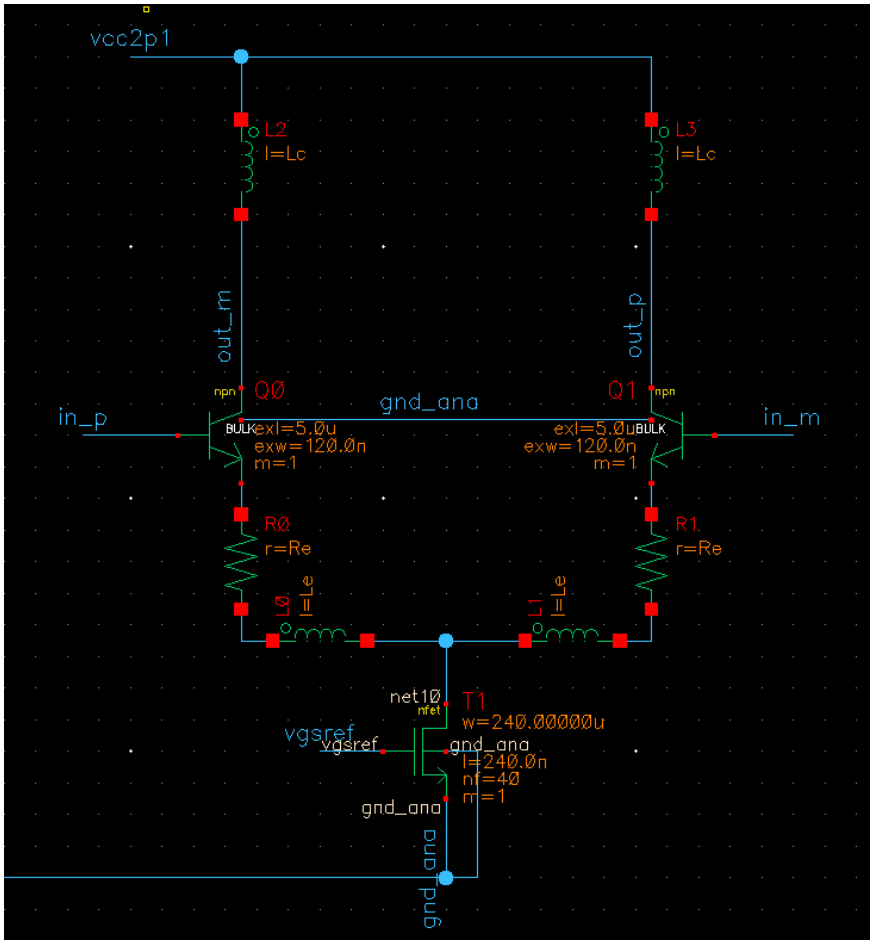

Figure 11. Mixer output buffer schematic.

Table 3. Mixer output buffer component parameters.

Parameter	*Value*
NMOS Transistor W/L	240 µm / 120 nm
R_e	20 Ω
L_c	2.8 nH
L_e	1.8 nH

Chapter 4

Simulation Results

4.1 Simulation Overview

To characterize the performance of this work's proposed mixer topology, several simulations were run using the Cadence SpectreRF engine. Among the performance metrics measured were conversion gain, RF and IF bandwidth, IP1dB, OP1dB, and noise figure. To determine whether the proposed mixer offers any significant performance advantages over a standard Gilbert cell mixer, a reference Gilbert mixer was designed and subjected to the same simulations as the proposed topology. It should be noted that in all simulations for both mixer designs, ideal models were used for passive circuit components, such as resistors and capacitors. Replacing these ideal components with more realistic passive component models provided by the GlobalFoundries 8XP PDK would almost certainly lead to performance degradation in both designs. The nature of this degradation will be explored in future work.

4.2 Reference Gilbert Cell Design

The schematic of the reference Gilbert cell mixer used for comparison is shown in Figure 12. Both the mixing quad and the transconductance stage consist entirely of SiGe HBTs due to their high gain and good high-frequency performance [10]. The mixer is loaded with resistors to ensure a high conversion gain and large IF bandwidth. A tuning capacitor appears between the output nodes to attenuate high-frequency harmonics. The reference Gilbert cell mixer is biased with the same supply voltage and DC current as the proposed topology to ensure both designs

consume the same DC power. Component parameters for the reference Gilbert cell mixer are displayed in Table 4.

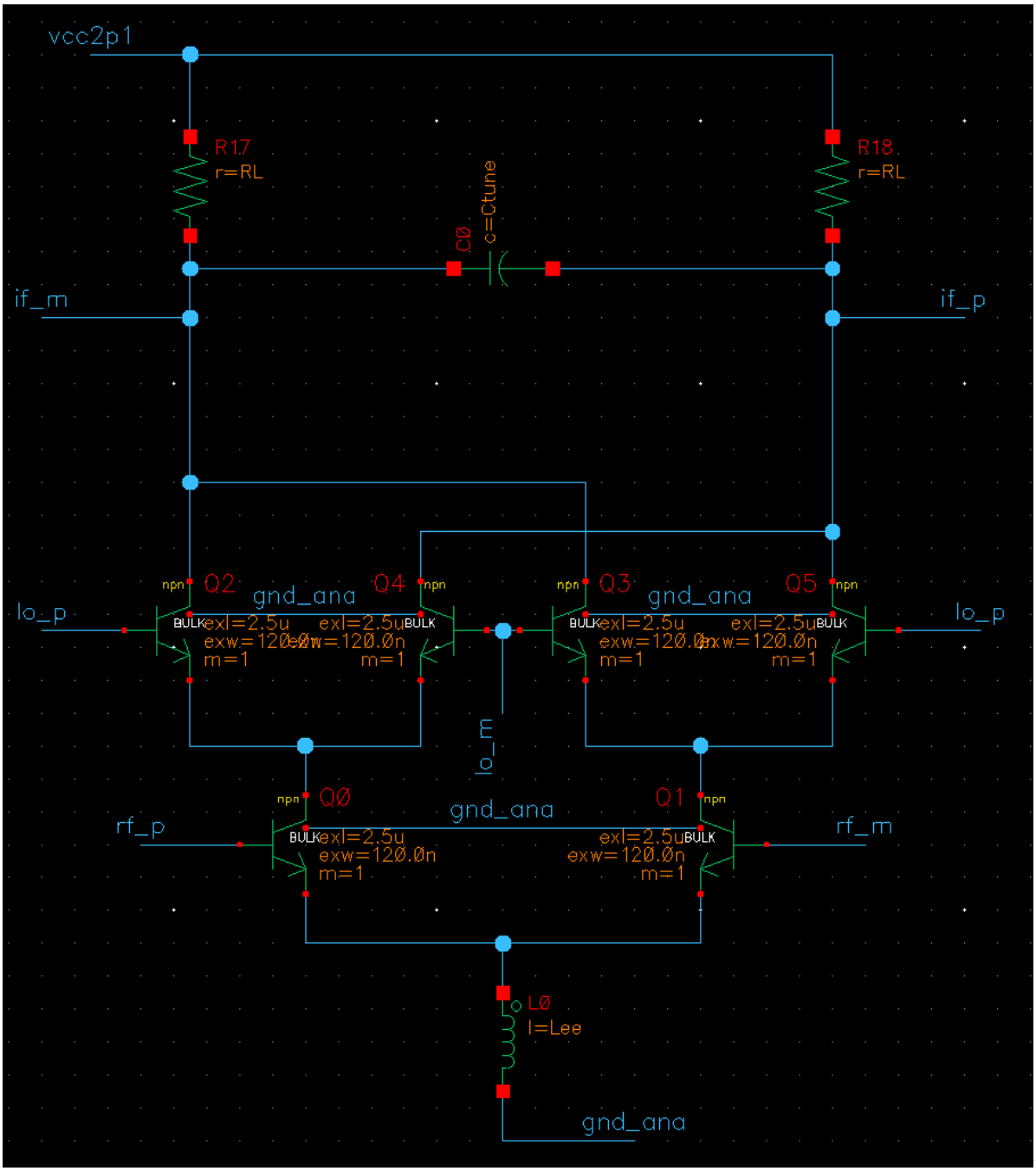

Figure 12. Reference Gilbert cell mixer schematic.

Table 4. Reference Gilbert cell mixer component parameters.

Parameter	*Value*
SiGe HBT Emitter L/W	2.5 µm / 120 nm
R_L	250 Ω
C_{tune}	30 fF
L_{ee}	540 pH

4.3 Mixer Simulation Test Bench

A Cadence Virtuoso schematic of the test bench used to evaluate the performance of this work's proposed mixer design is shown in Figure 13. In the schematic, the input RF signal is applied to the mixer via PORT0, while the LO signal is applied via PORT2 and PORT3. The IF output is measured in PORT1. A shunt tuning capacitor appears between the output of the mixer and the input of the TIA. This capacitor attenuates high-frequency harmonics at the mixer output, and it improves interstage matching between the mixer and the TIA. The value selected for this capacitor is 350 fF. Additionally, two series inductors appear between PORT0 and the mixer input. These inductors are used to achieve reactive input matching, boosting conversion gain and noise performance. Each inductor has a value of 140 pH. To see the impact of these source inductors, the mixer's S11 is plotted vs. RF frequency at an LO frequency of 25 GHz in Figure 14. With the source inductors, S11 is less than -10 dB over a large RF bandwidth, indicating a strong match. Without the source inductors, S11 never drops below -10 dB.

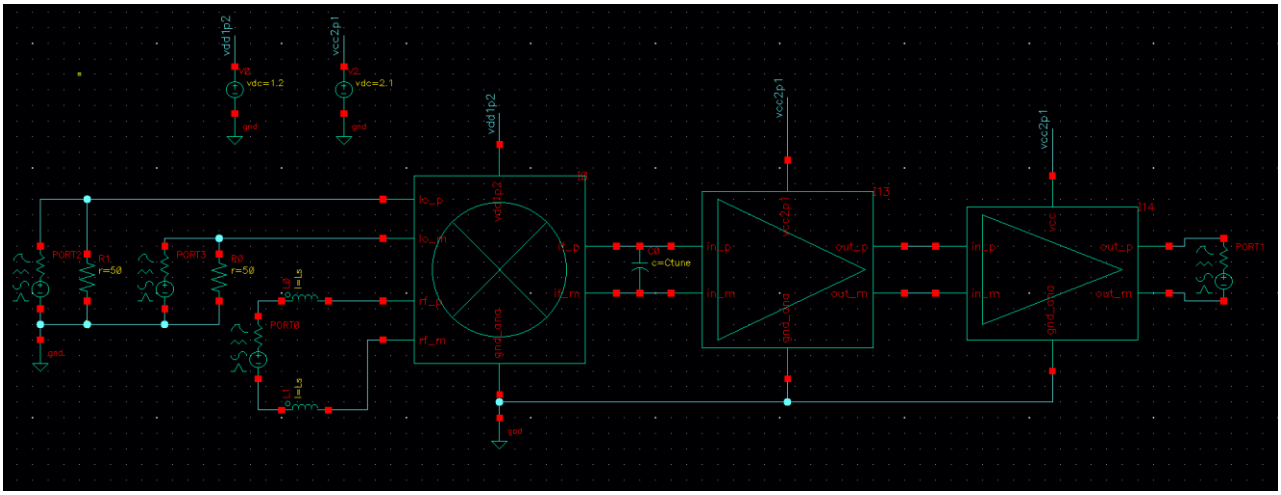

Figure 13. Schematic of test bench for the proposed mixer design.

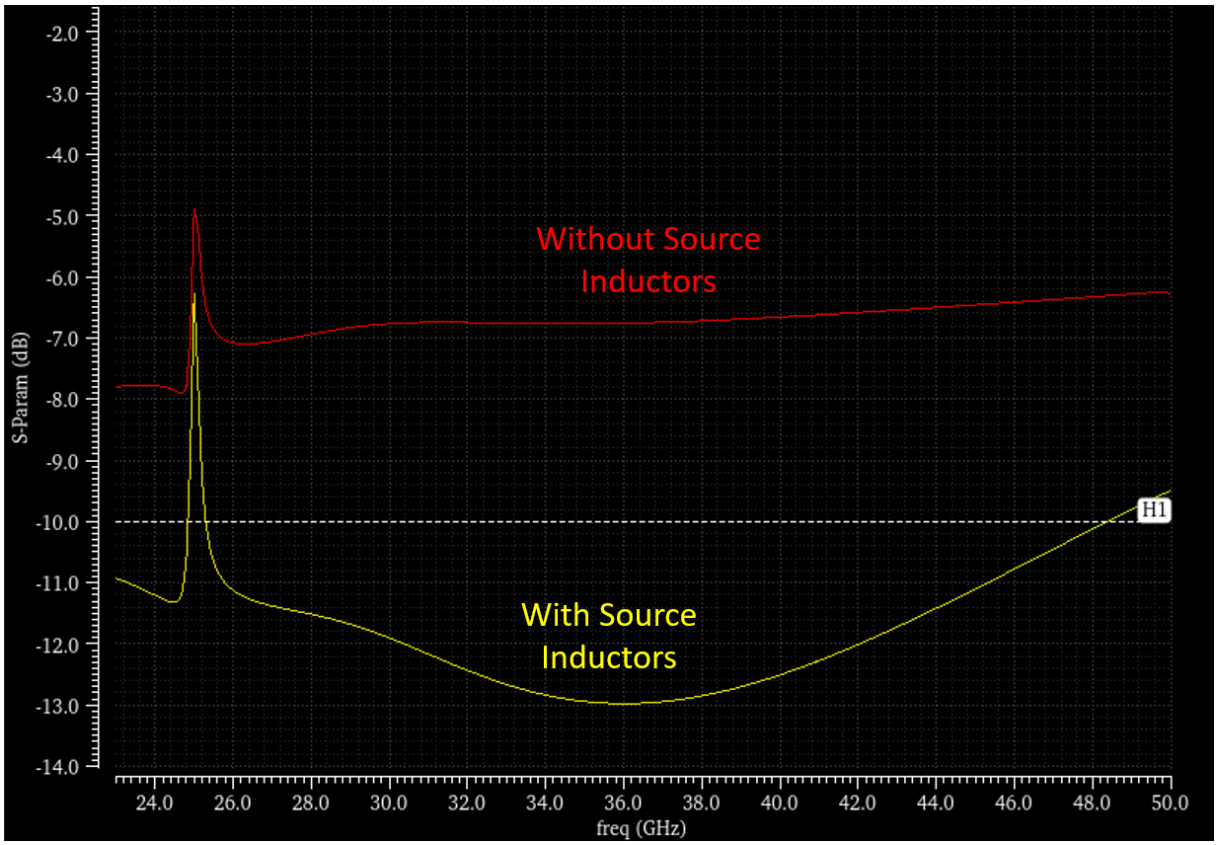

Figure 14. S11 vs. RF frequency at LO frequency of 25 GHz for the proposed mixer design.

The schematic of the test bench used to evaluate the reference Gilbert cell mixer is shown in Figure 15. The input RF signal is applied to the mixer via PORT0, while the LO signal is applied via PORT3. The IF output is measured in PORT1. To enable fair comparison, the same output buffer used in the proposed mixer design is implemented at the output of the Gilbert cell. To achieve broadband matching, shunt resistors are placed between the RF port and the mixer input as well as between the LO port and the LO input. This broadband matching is illustrated in Figure 16, which depicts the mixer's S11 vs. RF frequency at an LO frequency of 25 GHz. S11 is less than -10 dB over an enormous RF bandwidth. It should be noted that resistive matching is generally undesirable because it dissipates power and slightly degrades the mixer's noise figure.

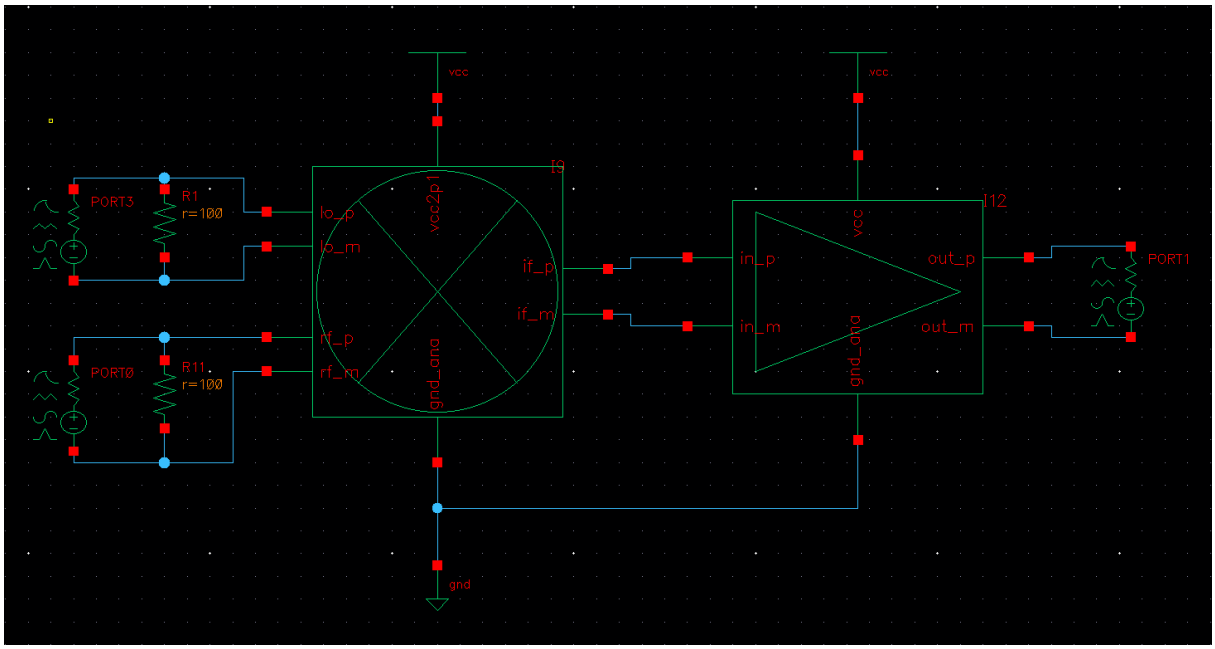

Figure 15. Schematic of test bench for the reference Gilbert cell mixer.

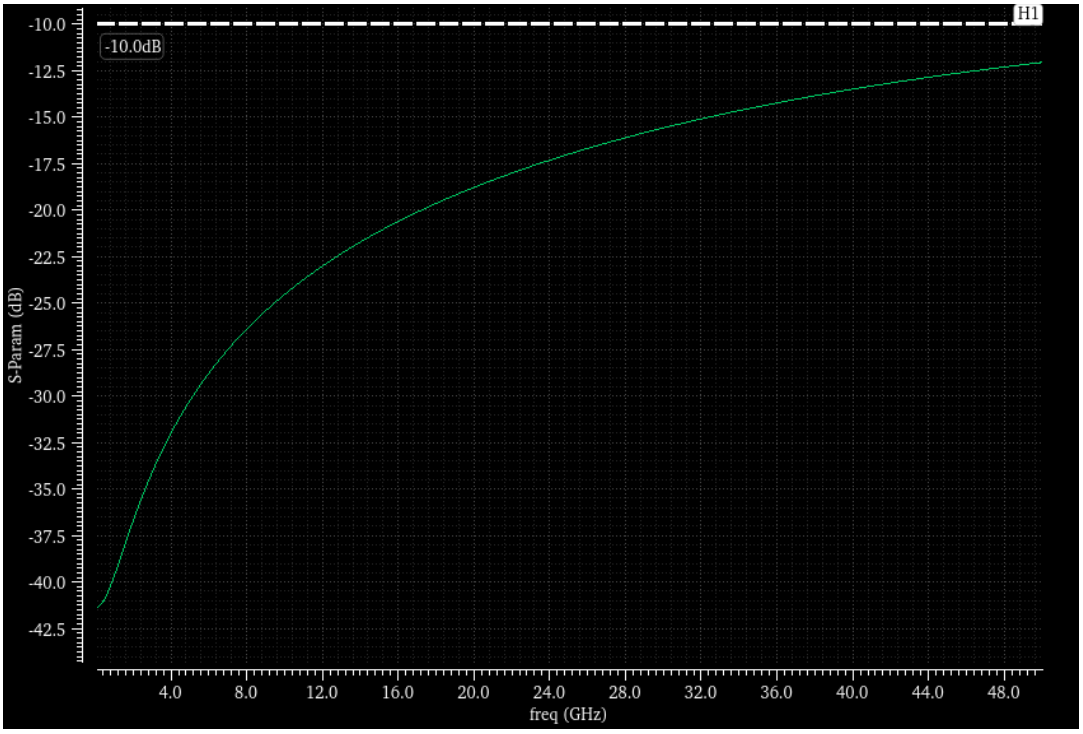

Figure 16. S11 vs. RF frequency at LO frequency of 25 GHz for the reference Gilbert cell mixer.

4.4 Conversion Gain and Bandwidth

At an LO frequency of 25 GHz, the voltage conversion gain of each mixer design was measured for input RF frequencies ranging from 26 GHz to 32 GHz, corresponding to IF frequencies ranging from 1 GHz to 7 GHz. The proposed mixer design exhibited a peak voltage conversion gain of 0.77 dB at an IF frequency of 2.56 GHz. The 3-dB bandwidth of this conversion gain was measured to range from 1.11 GHz to 5.25 GHz. The voltage conversion gain of the proposed mixer is plotted against the IF frequency in Figure 17. Meanwhile, the reference Gilbert cell mixer exhibited a peak voltage conversion gain of 14.8 dB at an IF frequency of 2.32 GHz. The corresponding 3-dB bandwidth was measured to range from 1.01 GHz to 5.06 GHz. The voltage conversion gain of the reference Gilbert cell mixer is plotted against IF frequency in Figure 18.

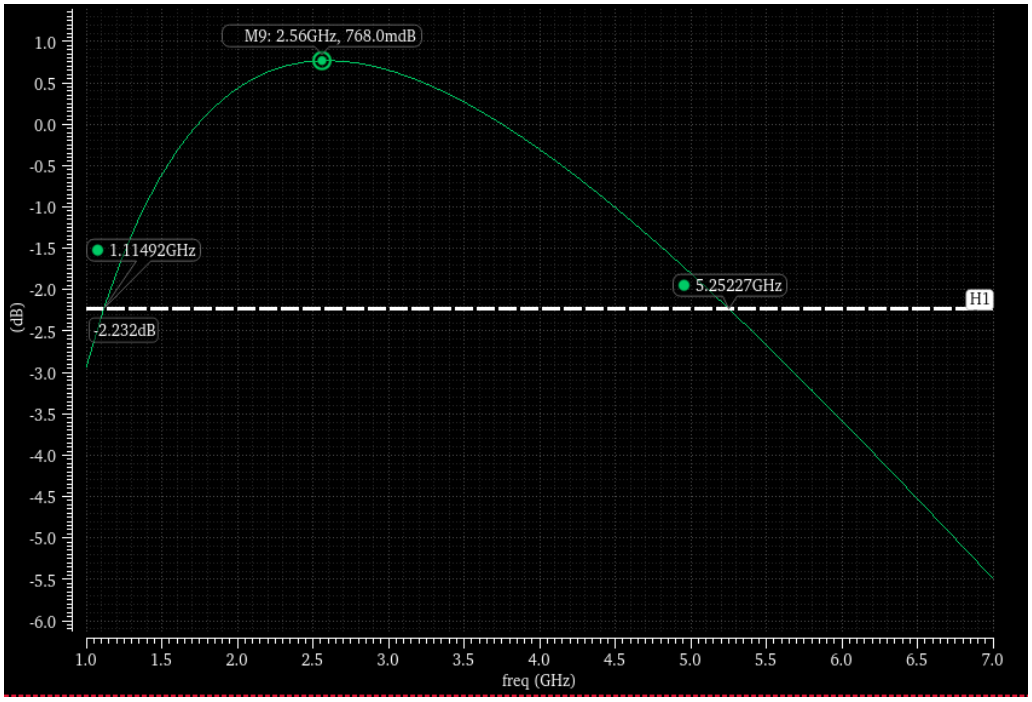

Figure 17. Voltage conversion gain of the proposed mixer design vs. IF frequency.

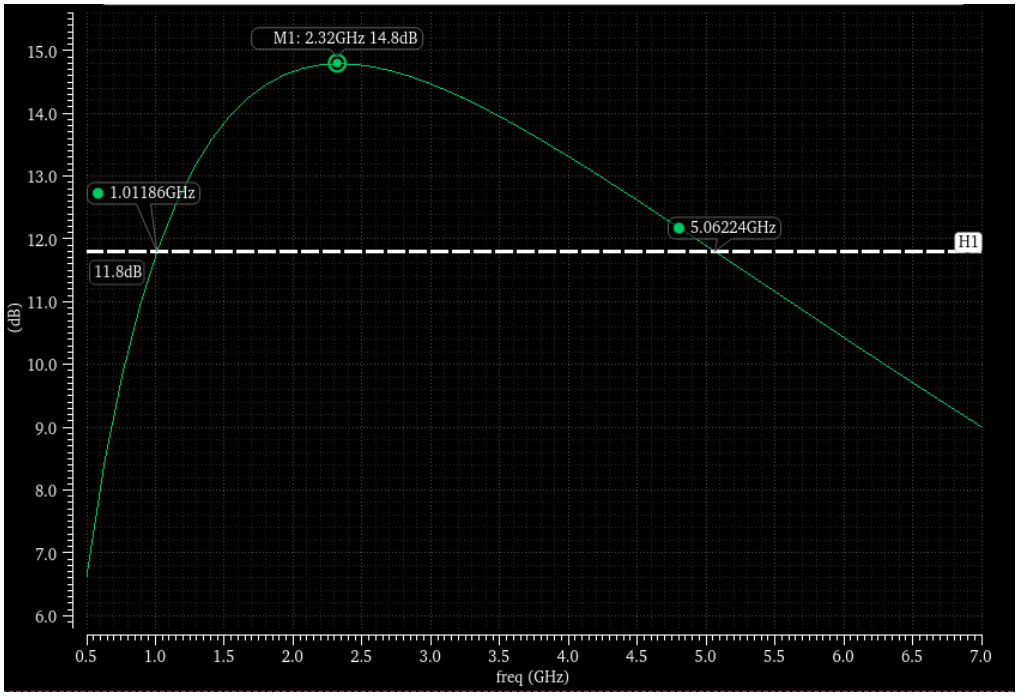

Figure 18. Voltage conversion gain of the reference Gilbert cell mixer vs. IF frequency.

After determining the IF bandwidth of each mixer design at an LO frequency of 25 GHz, the RF bandwidth of each design was characterized. To do this, the power conversion gain of each design was measured at input RF frequencies ranging from 24 GHz to 50 GHz. For each measurement, the LO frequency was chosen such that the IF frequency at the output would be 3 GHz. The resulting conversion gain measures for both designs are plotted in Figure 19. Both designs exhibited comparable conversion gain roll-off with increasing RF frequency. Additionally, the total conversion gain degradation over the entire RF bandwidth was less than 3 dB for both designs. This means that both designs have an RF bandwidth that extends beyond the target bandwidth of 24 GHz to 50 GHz.

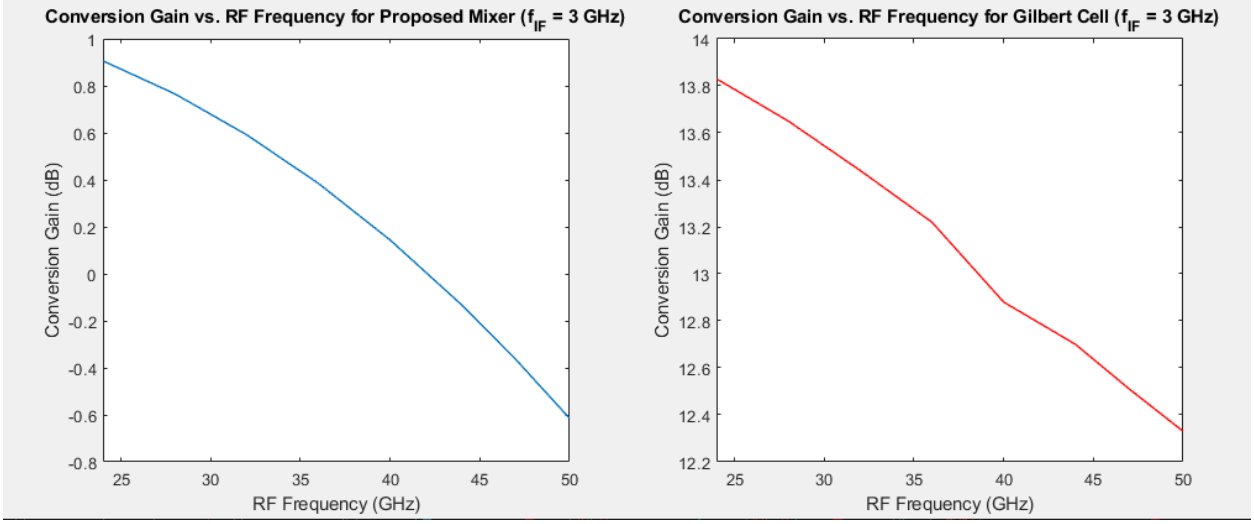

Figure 19. Power conversion gain vs. RF frequency for both mixer designs.

4.5 Linearity

At an LO frequency of 25 GHz, the linearity of each mixer design was measured for an input RF frequency of 28 GHz, corresponding to an IF frequency of 3 GHz. Under these conditions, the proposed mixer topology exhibited a power conversion gain of 0.80 dBm and an IP1dB of 0.44 dBm, shown in Figure 20. The proposed mixer also exhibited an OP1dB of about

0.23 dBm, shown in Figure 21. The reference Gilbert cell mixer exhibited a power conversion gain of 14.0 dB, an IP1dB of -12.81 dBm, and an OP1dB of 0.18 dBm. These results are plotted in Figure 22 and Figure 23.

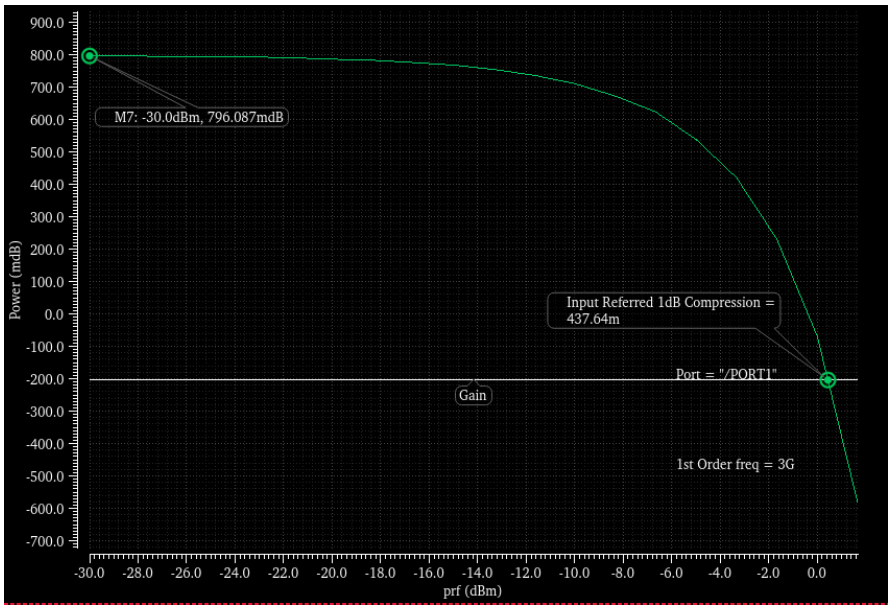

Figure 20. Conversion gain of the proposed mixer design vs. input RF power.

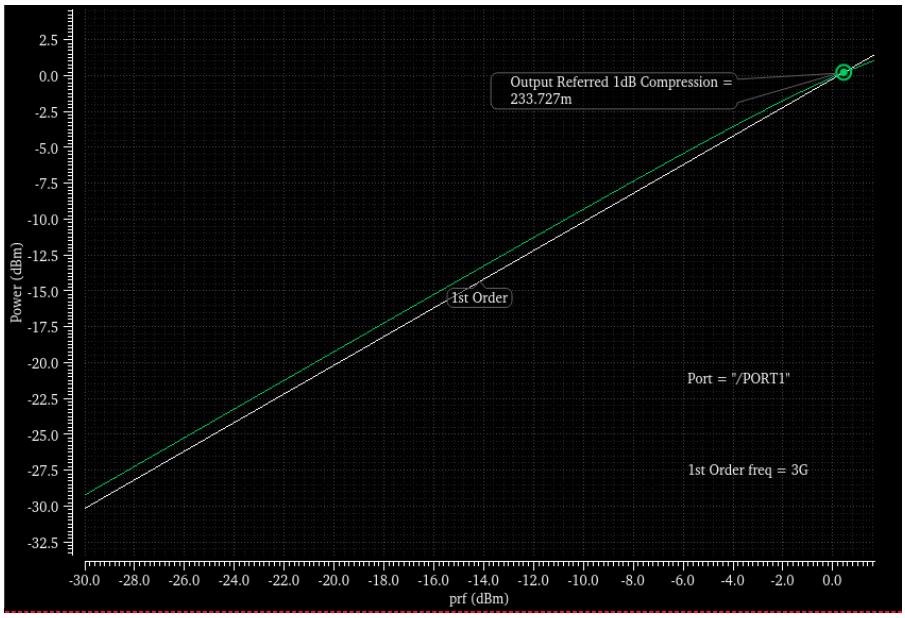

Figure 21. Output power of the proposed mixer design vs. input RF power.

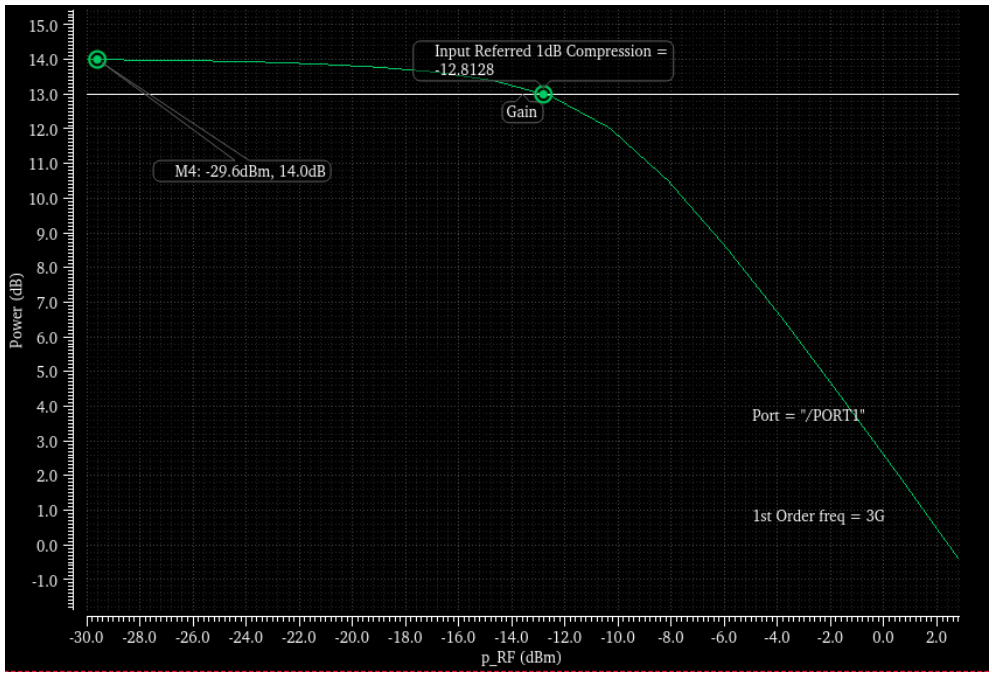

Figure 22. Power conversion gain of the reference Gilbert cell mixer vs. input RF power.

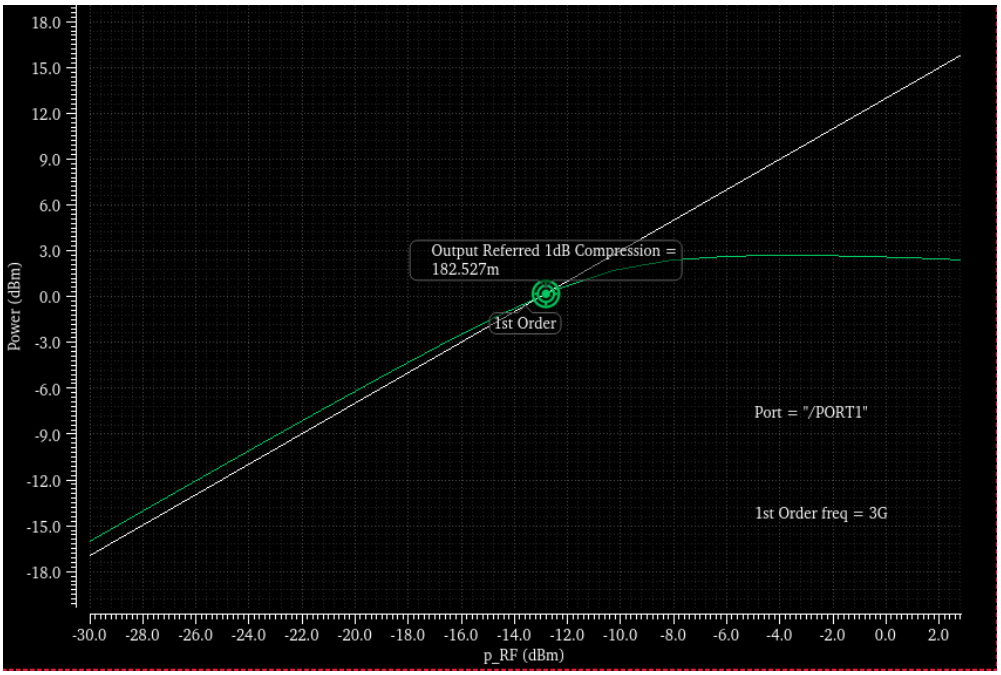

Figure 23. Output power of the reference Gilbert cell mixer vs. input RF power.

4.6 Noise Figure

At an LO frequency of 25 GHz, the noise figure of each mixer design was measured for input RF frequencies spanning 25.5 GHz to 32 GHz, corresponding to IF frequencies ranging from 500 MHz to 7 GHz. The noise figure of the proposed mixer ranged from 15.91 dB to 20.78 dB over its IF bandwidth. The average value of the noise figure over this range was 18.22 dB. The noise figure of the proposed mixer is plotted against the IF frequency in Figure 24. The noise figure of the reference Gilbert cell mixer ranged from 12.12 dB to 12.2 dB over its IF bandwidth. The average value of the noise figure over this range was 12.15 dB. The noise figure of the reference Gilbert cell mixer is plotted against the IF frequency in Figure 25.

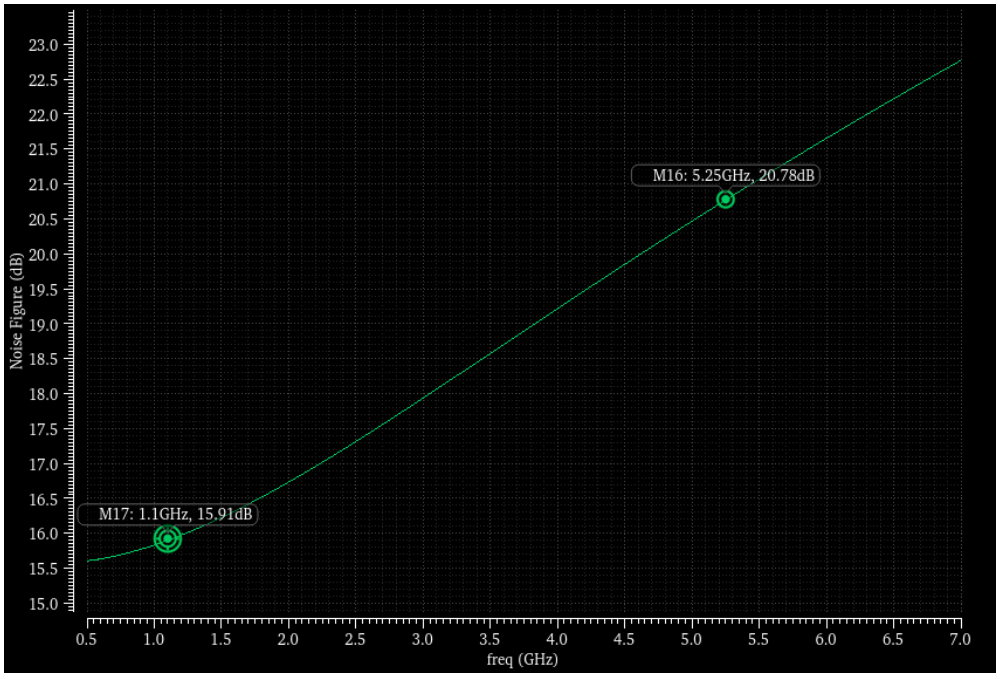

Figure 24. Noise figure of the proposed mixer vs. IF frequency.

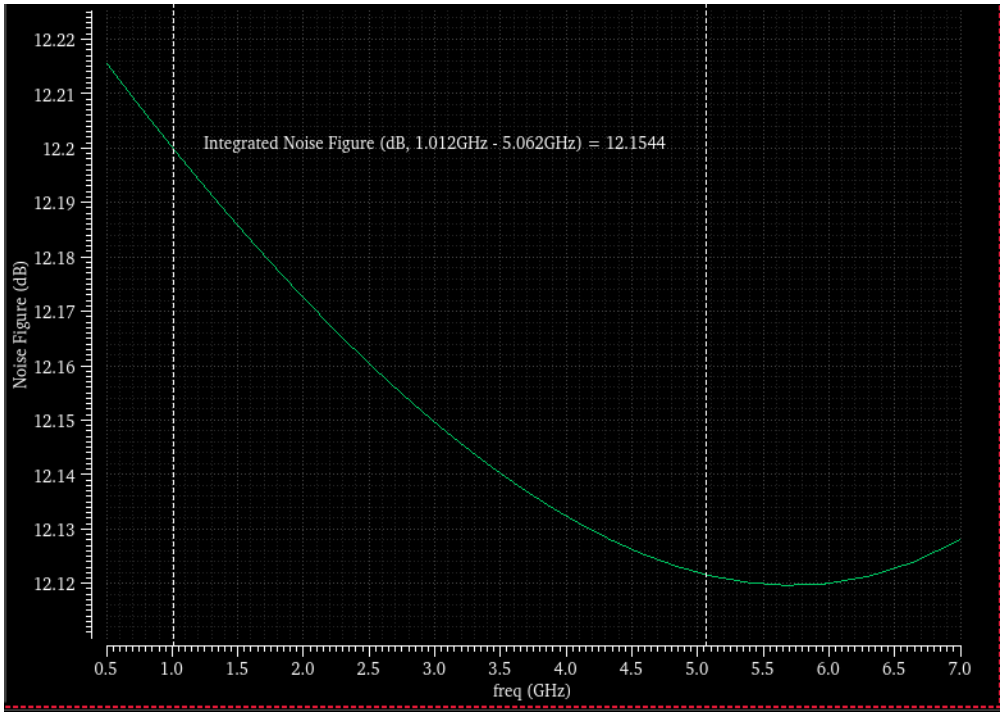

Figure 25. Noise figure of the reference Gilbert cell mixer vs. IF frequency.

4.7 Consideration of Gilbert Cell Mixer with an Attenuator at the Input

Comparing the simulation results between the proposed mixer design and the reference Gilbert cell, it is clear that while the proposed design exhibits a larger IP1dB than the Gilbert cell, the Gilbert cell offers much higher conversion gain and better noise performance. This introduces the possibility that simply interfacing an attenuator to the input port of the Gilbert cell could increase the mixer's IP1dB while maintaining positive conversion gain and good noise performance. To test this, a 13-dB resistive attenuator was designed and placed at the Gilbert cell input port, as shown in Figure 26. The gain of the attenuator is plotted vs. RF frequency in Figure 27

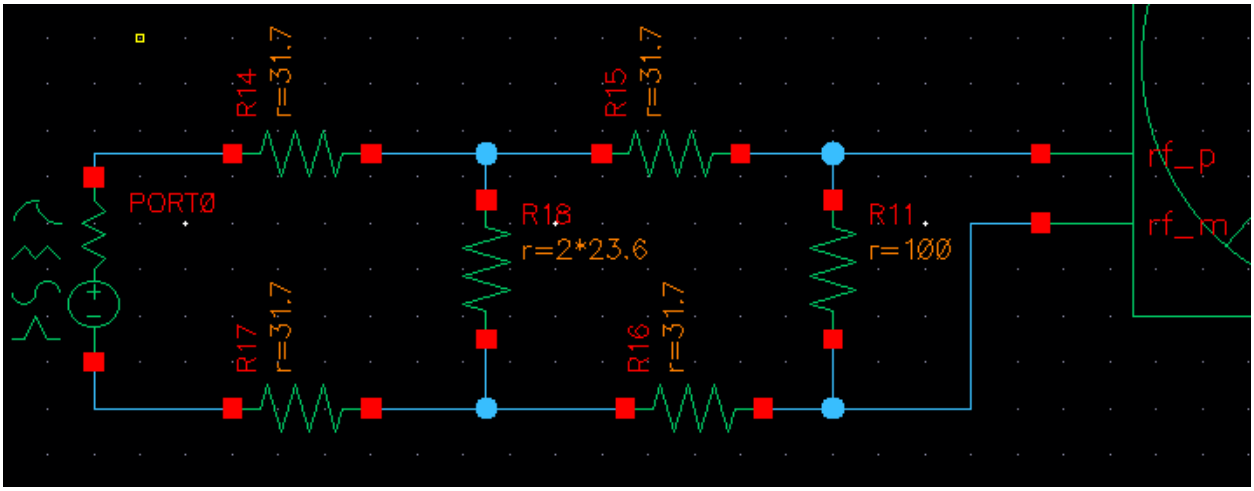

Figure 26. Schematic of 13-dB attenuator placed at Gilbert cell input port.

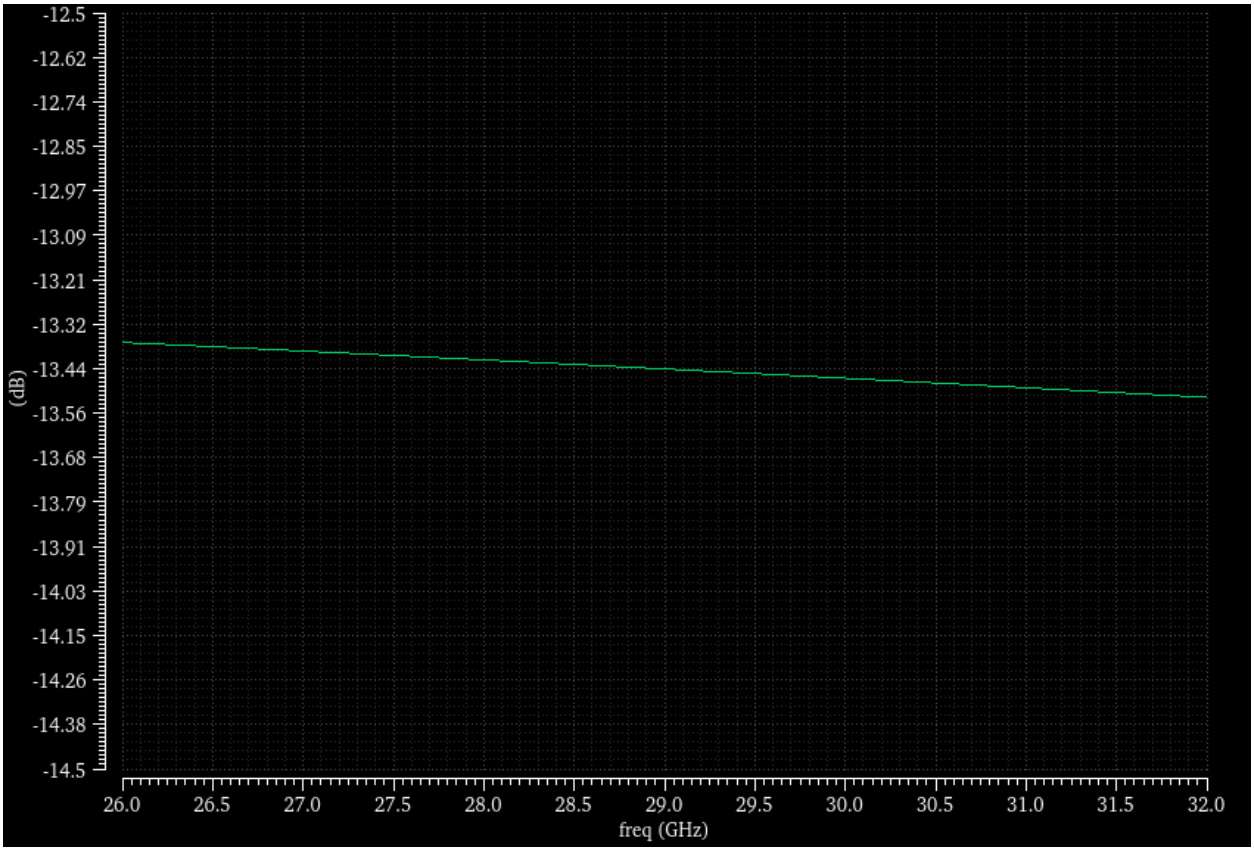

Figure 27. Gain of 13-dB attenuator vs. RF frequency.

With the attenuator interfaced to its input port, the Gilbert cell mixer exhibited a conversion gain of 1.02 dB, an IP1dB of 0.05 dBm, and an OP1dB of 0.07 dBm, as shown in Figure 28 and Figure 29. This contrasts with the 14.0 dB conversion gain and IP1dB of -12.81 dBm achieved without the attenuator present. The improved linearity afforded by the attenuator comes at the expense of noise performance, however. With the attenuator present, the Gilbert cell exhibits an average noise figure of 25.16 dB over its IF bandwidth, as shown in Figure 30.

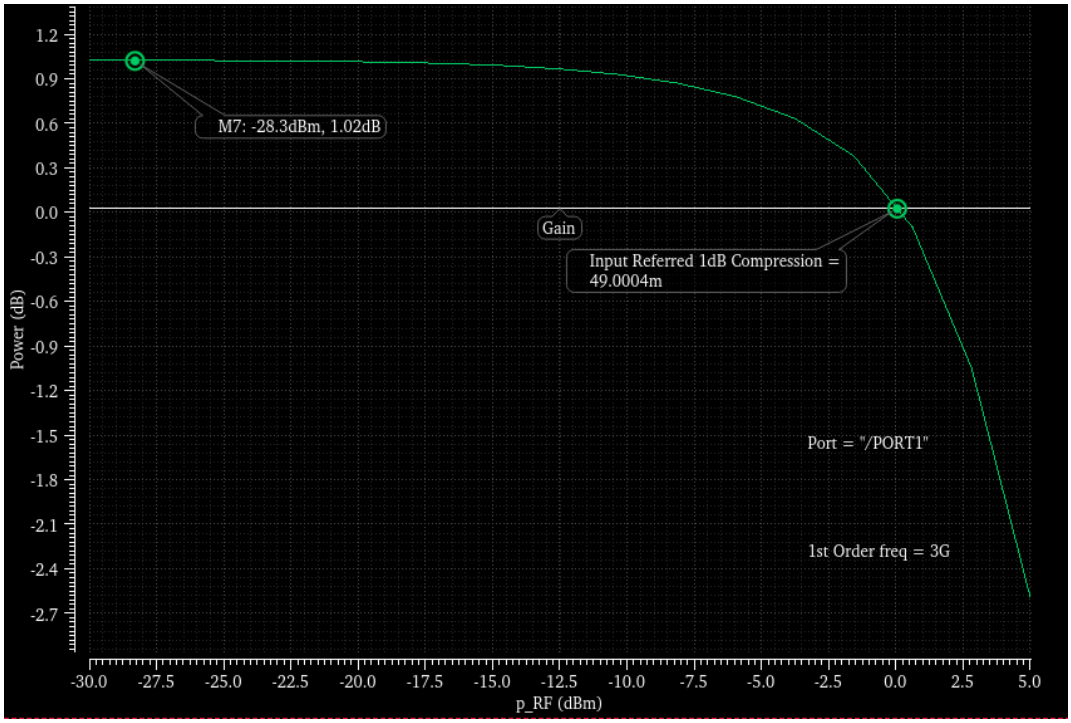

Figure 28. Power conversion gain of the reference Gilbert cell mixer with input attenuator vs. input RF power.

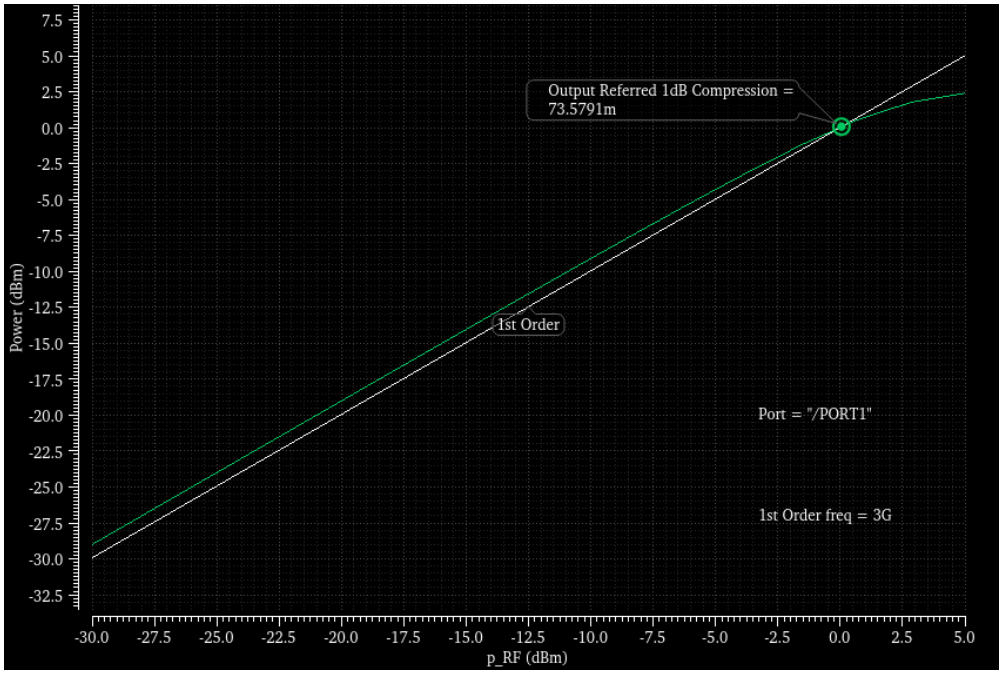

Figure 29. Output power of the reference Gilbert cell mixer with input attenuator vs. input RF power.

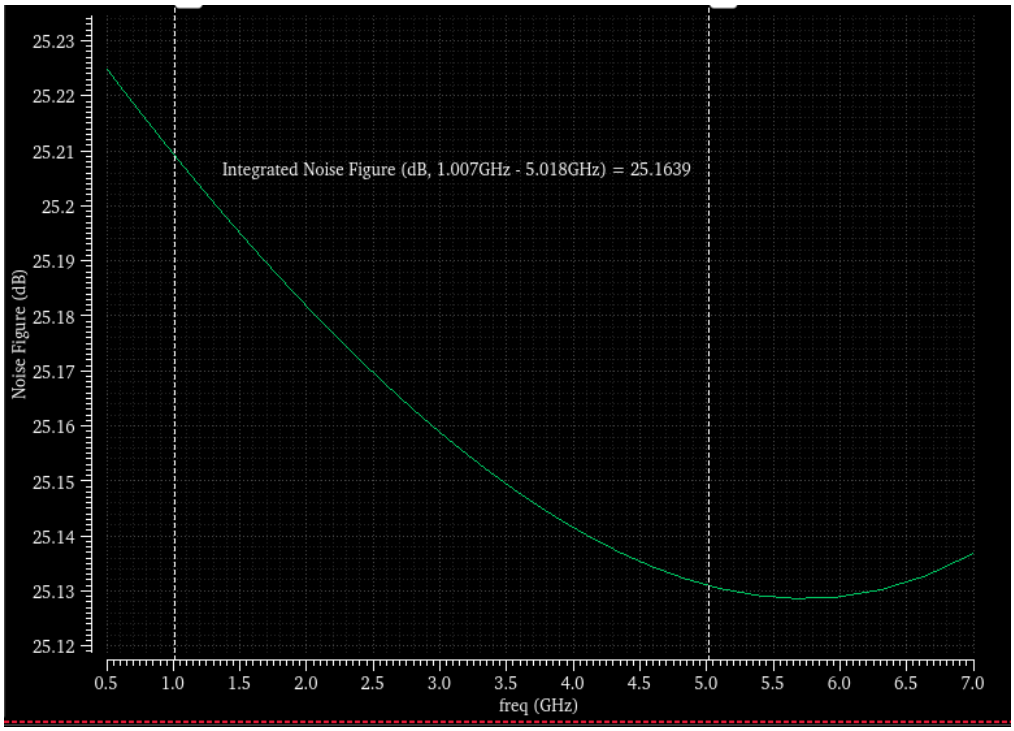

Figure 30. Noise figure of reference Gilbert cell mixer with an attenuator at its input port.

The noise figure of a passive attenuator is approximately equal to the loss it imparts [18]. The result obtained in Figure [blank] can be predicted via the Friis formula for noise, which yields the total noise factor for a system consisting of any number of cascaded stages [19]. Applying the Friis formula to the Gilbert cell mixer with an input attenuator yields Equation (4.1), in which F_{mixer} is the noise factor of the Gilbert cell mixer, F_{atten} is the noise factor of the attenuator, F_{total} is the total noise factor, and G_{atten} is the linear power gain of the attenuator.

$$F_{total} = F_{atten} + \frac{F_{mixer} - 1}{G_{atten}} \qquad (4.1)$$

Taking the gain of the attenuator to be -13 dB, the noise figure of the attenuator to be 13 dB, and the noise figure of the mixer to be 12 dB, the calculation of the total noise figure NF_{total} proceeds as shown in Equation (4.2).

$$NF_{total} = 10\log\left(10^{\frac{13}{10}} + \frac{10^{\frac{12}{10}} - 1}{10^{-\frac{13}{10}}}\right) = 25\ dB \qquad (4.2)$$

This result is consistent with Figure 30, and it shows that the noise figure of the Gilbert cell mixer with an input attenuator strongly depends on the attenuator's gain. Higher attenuator gain results in a lower system noise figure. Thus, a possible way to improve the Gilbert cell's linearity without excessive noise figure degradation is to design the mixer to have a smaller conversion gain, as this could ensure that less attenuation is required at the input to ensure an IP1dB of around 0 dBm.

To test the effect of decreasing the Gilbert cell's gain, its linearity was simulated (without an attenuator) using load resistance values of 50 Ω, 150 Ω, and 250 Ω, corresponding to three different conversion gain values. The resulting plots are shown in Figure 31. Figure 31indicates that decreasing the Gilbert cell's load resistance results in decreased conversion gain. This

decreased conversion gain does not change the mixer's IP1dB very significantly, however. This means that to increase the mixer's IP1dB to above 0 dBm, a 13-dB attenuator would be required at the mixer input in all three cases. This result indicates that the mixer design proposed in this work offers a combination of linearity and noise performance that the reference Gilbert cell mixer cannot achieve, even with an attenuator at its input.

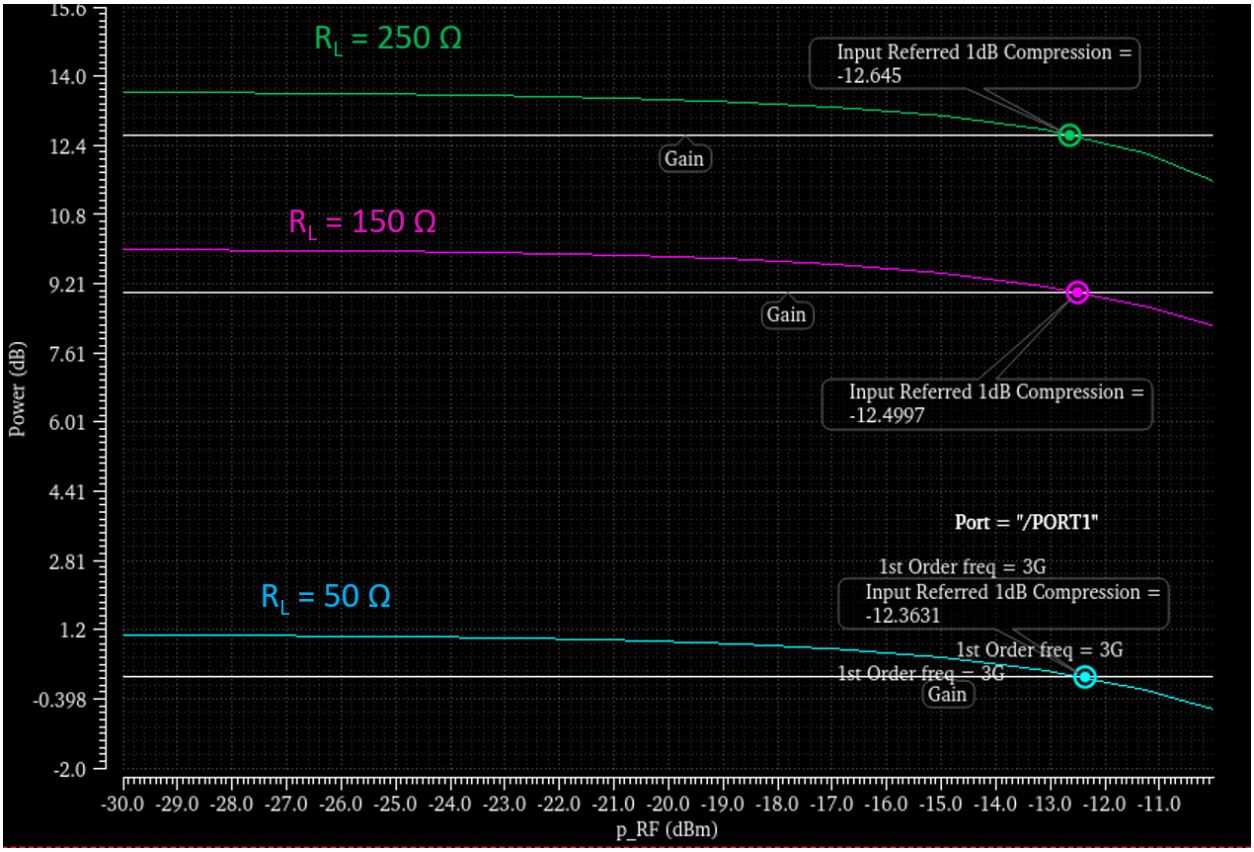

Figure 31. Conversion gain and IP1dB of Gilbert cell mixer using different load resistance values.

Chapter 5

Summary with Comparison Table

5.1 Summary

This thesis presents a novel mmWave down-conversion mixer topology intended to operate in nearly all 5G FR2 bands. The proposed mixer consists of a passive mixer composed of high-linearity CMOS RF switches followed by a TIA, and it is designed for highly linear operation, exhibiting positive conversion gain, IP1dB, and OP1dB. The mixer design proposed in this work overcomes the trade-off between linearity and DC power consumption exhibited by the traditional Gilbert cell mixer, enabling highly linear operation while maintaining acceptable noise performance and minimizing DC power consumption.

5.2 Comparison Table

A performance comparison among this work's proposed mixer design, the reference Gilbert cell mixer, and the reference Gilbert cell mixer with an input attenuator is shown in Table 5. In the table, an IF frequency of 3 GHz was used when obtaining each performance metric.

Table 5. Comparison table of different mixer topologies at an IF frequency of 3 GHz.

Performance Metric	*Proposed Mixer Topology*	*Reference Gilbert Cell*	*Reference Gilbert Cell with 13-dB Input Attenuator*
DC Power Consumption (mW)	42	42	42
Conversion Gain (dB)	0.80	14.0	1.02
IF Bandwidth (GHz)	4.14	4.05	4.01
RF Bandwidth (GHz)	> 26	> 26	> 26
IP1dB (dBm)	0.44	-12.81	0.05
OP1dB (dBm)	0.23	0.18	0.07
Noise Figure (dB)	18.22	12.15	25.16

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ACADEMIC VITA

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Education

The Pennsylvania State University, University Park, PA 2020-2023

- Electrical Engineering Major
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High-Speed Integrated Circuits Lab Undergraduate Researcher 2022-Present

- Conducting integrated circuit design for ultra-wideband millimeter-wave mixers.

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- Published an IEEE paper describing and evaluating the application.

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- Regularly competing at elite-level national competitions.

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- Python
- LabVIEW
- C/C#
- Keysight ADS
- MS Office Suite

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Eta Kappa Nu Member	2021-Present
Tau Beta Pi Member	2021-Present
IEEE MASS 2022 REUNS Workshop Best Poster Award	2022
Academic All Big Ten Team	2022, 2023
College Gymnastics Association First-Team All-America Scholar Athlete	2021-2023

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1. M. Artlip, J. Chen and B. Li, "Virtual Reality-Based Gymnastics Visualization Using Real-Time Motion Capture Suit," 2022 IEEE 19th International Conference on Mobile Ad Hoc and Smart Systems (MASS), Denver, CO, USA, 2022, pp. 728-729, doi: 10.1109/MASS56207.2022.00112.

Other Activities

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- Socialized with and performed gymnastics for children and families suffering from pediatric cancer as part of the Penn State THON Athlete Hour.
- Prepared and performed a dance routine with Penn State men’s gymnastics team members for children and families affected by pediatric cancer as part of Penn State THON Pep Rally.